

An online laboratory notebook

since 2011

Posts published on March 9, 2025, by Owen Medeiros from qnn.mit.edu/wordpress. Printed on March 9, 2025

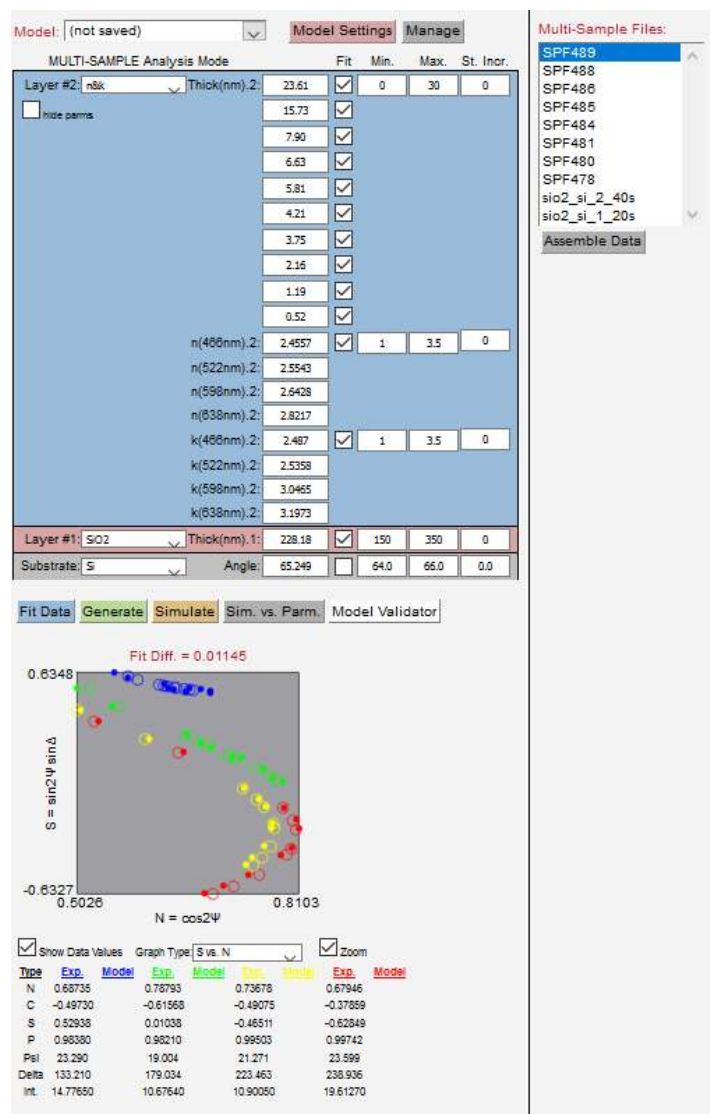
Determining Thickness of NbN Films Using Ellipsometry

June 8, 2018

Categories: NbN deposition

The FS-1 ellipsometer has a Multi-Sample Analysis Mode which combines data from 10 samples and fits a model to the measured Psi and Delta values.

This method works for films deposited under the same conditions (same n&k) with varying thicknesses (deposition times: 20s, 40s, 60s, 100s, 120s, 160s, 180s, 200s, 400s, 600s).



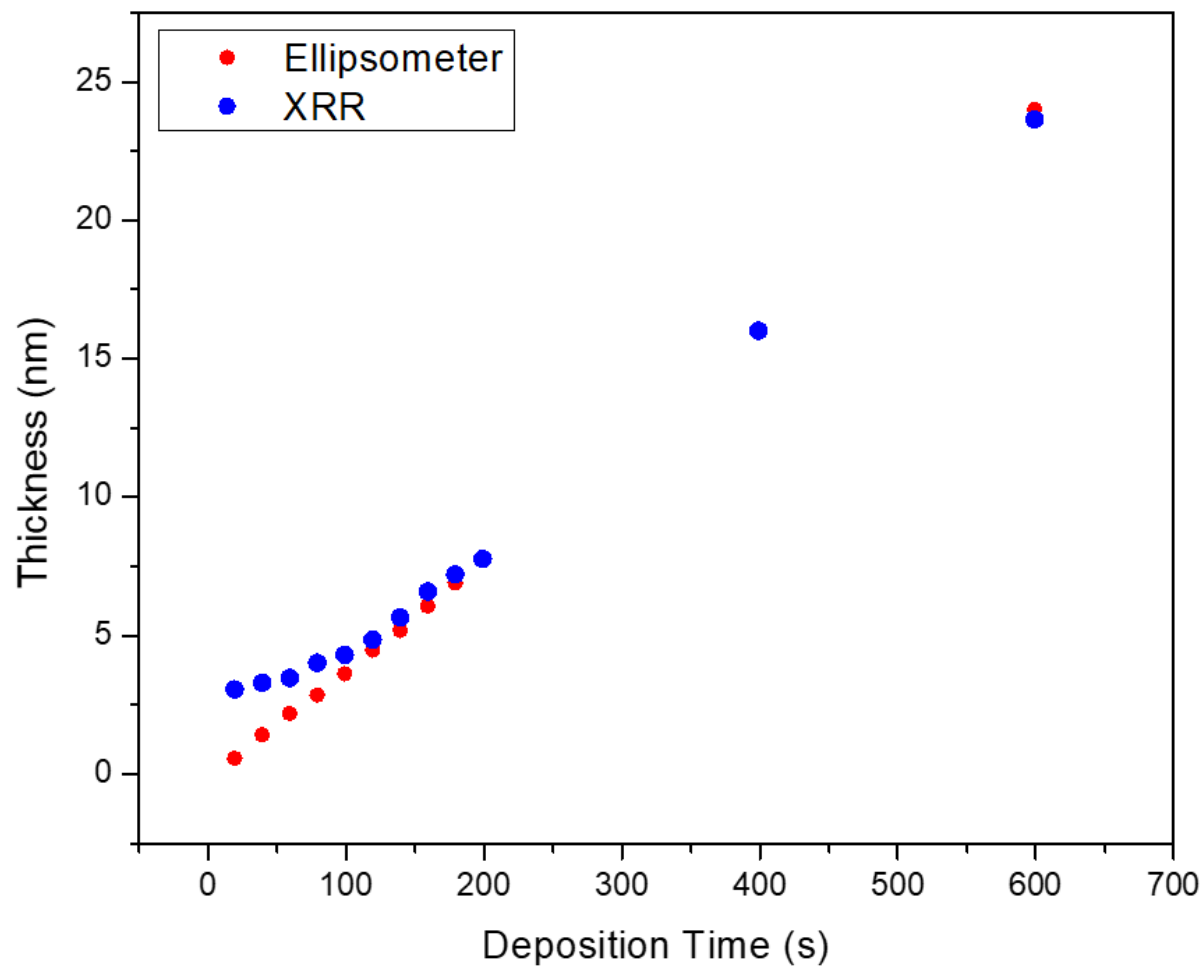
1.145% fit difference is very good. Notice the figure is zoomed in. Normal bounds are

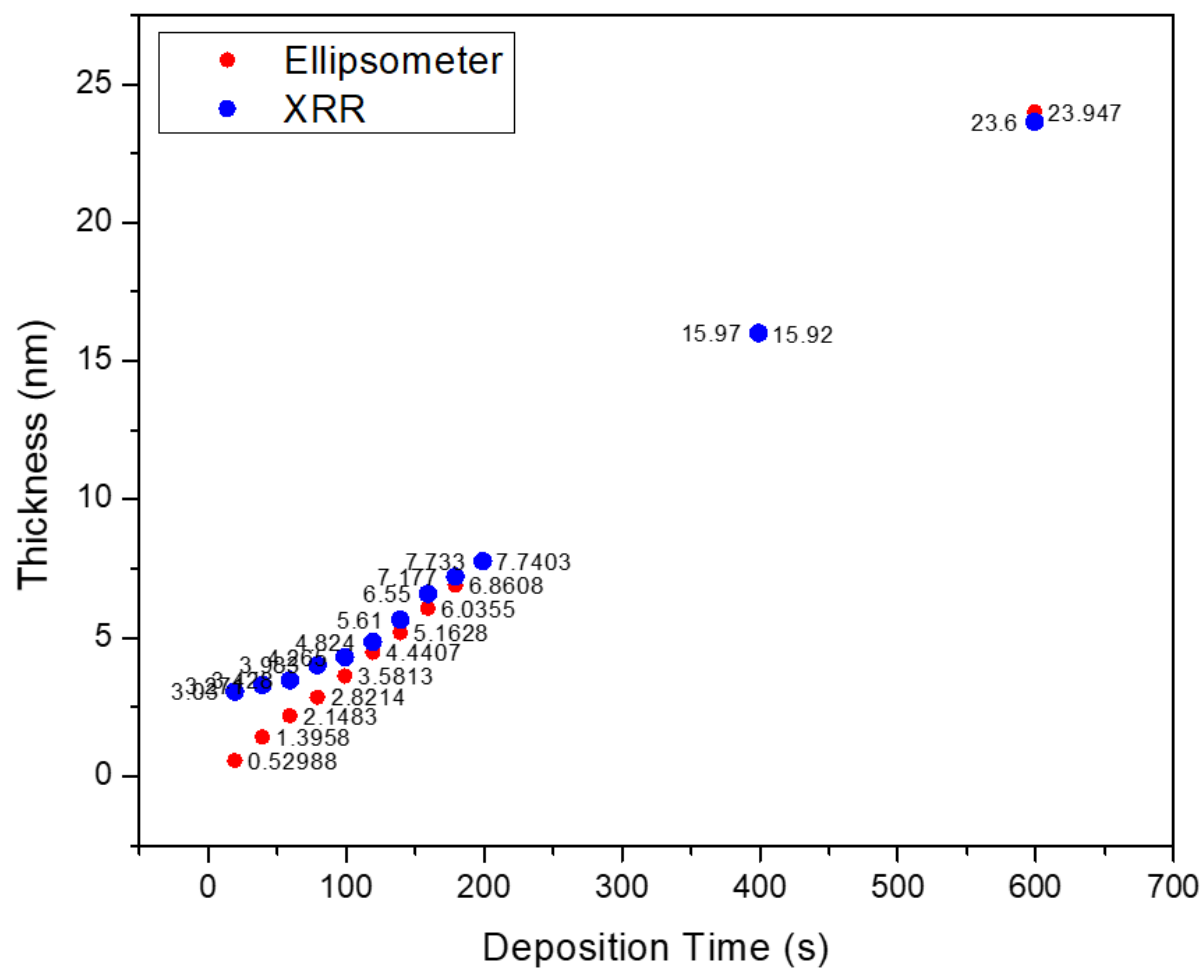
The n&k layer "can specify the index of refraction n and extinction coefficient k at each of the 4 FS-1 measurement wavelengths. This is often used for measuring and saving the optical constants of absorbing (e.g., metal) substrates." In this model, I fit all 10 thicknesses and the n&k for NbN as well as the thickness of SiO2.

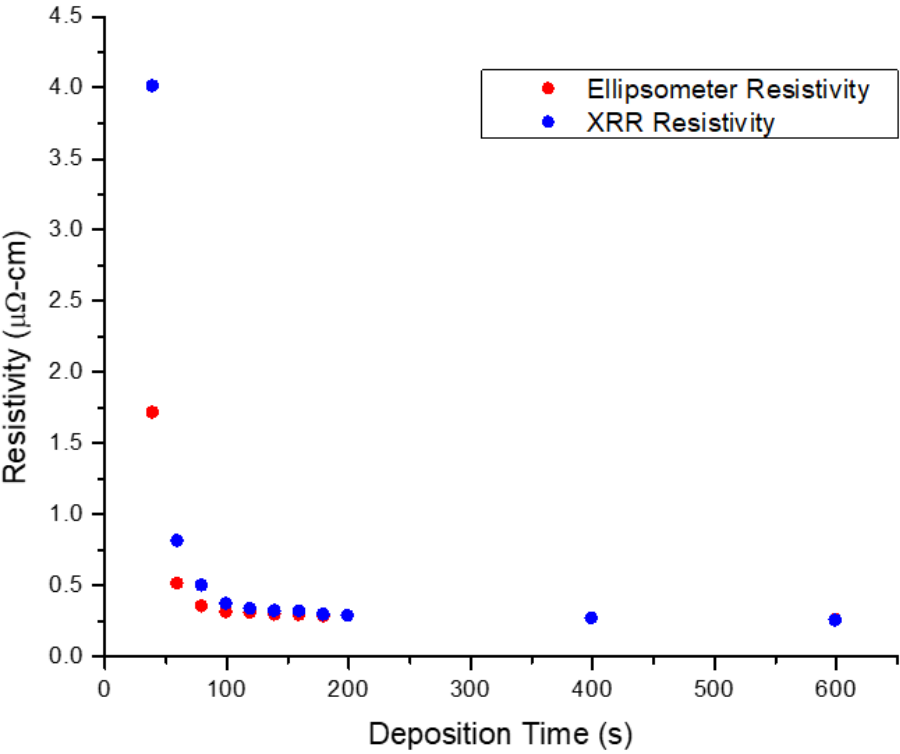
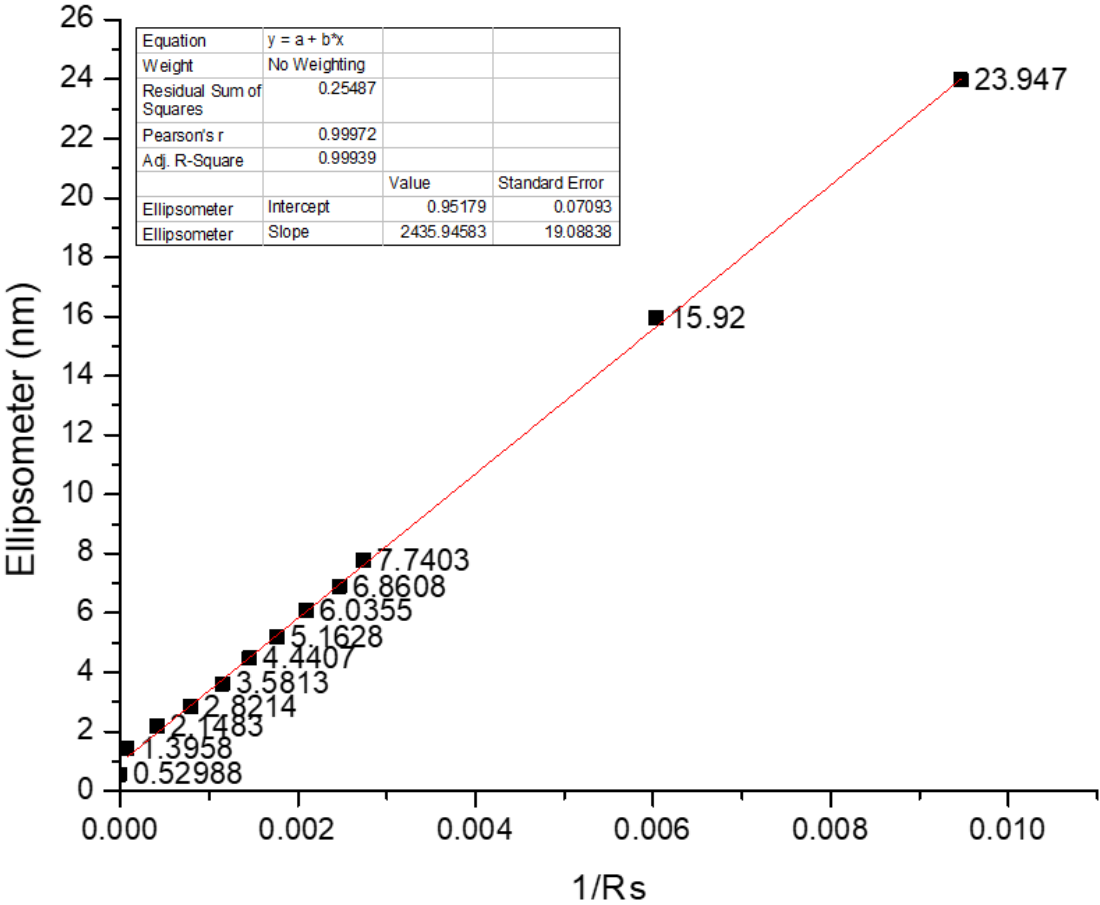
I chose to fit the silicon dioxide layer because each sample should have a similar thickness, this is similar to measuring each SiO2 thickness before deposition then averaging. The Nb2O5 layer is not present because the FS-1 is not able to fit

more than one layer using the multi-sample analysis mode. I could include it but that would assume every film to have the same amount of oxide.

Results from XRR so far:







Tracking oxide formation using ellipsometry

June 12, 2018

Categories: NbN deposition

To see what happens to a film over time I deposited a film and tracked any changes on the ellipsometer.

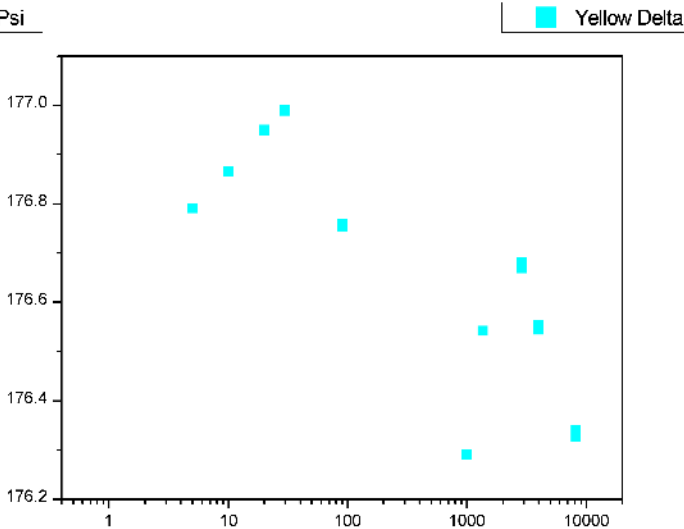
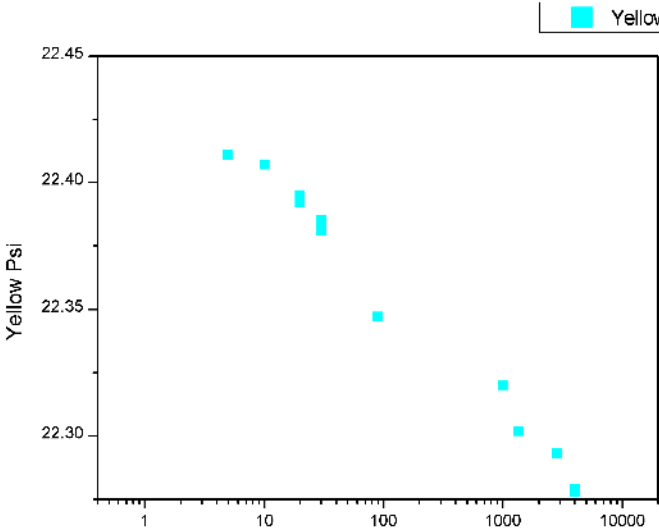
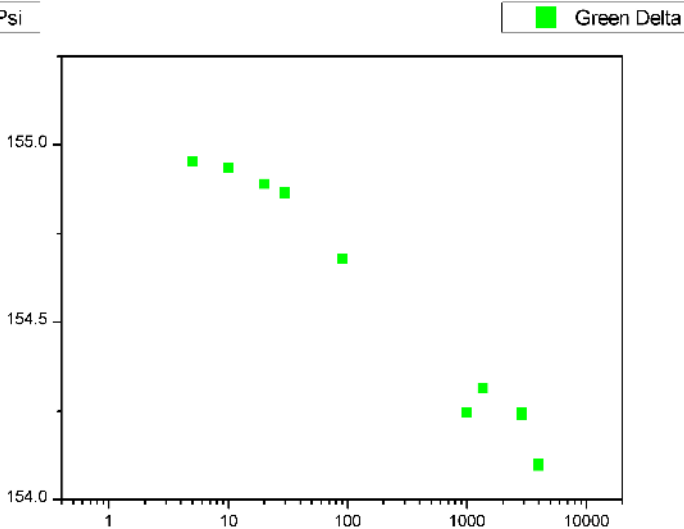
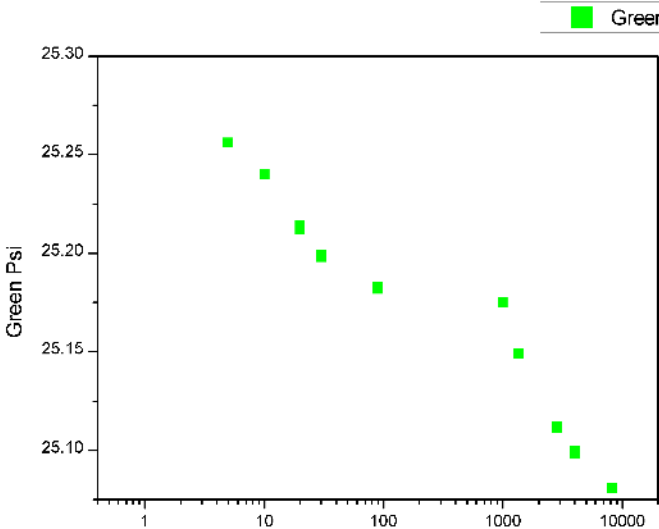
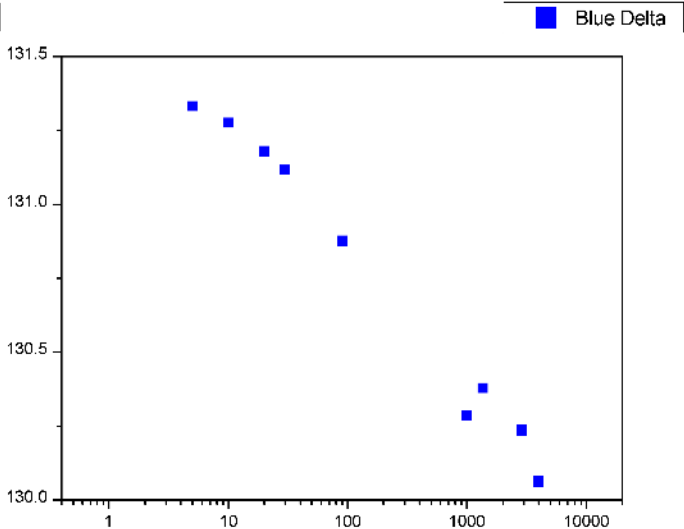
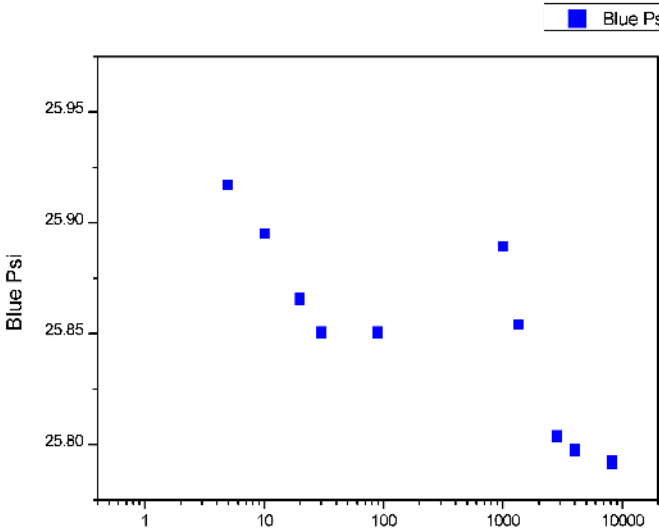
— **SPF528** 200s deposition (prior to target cleaning) standard process control parameters.

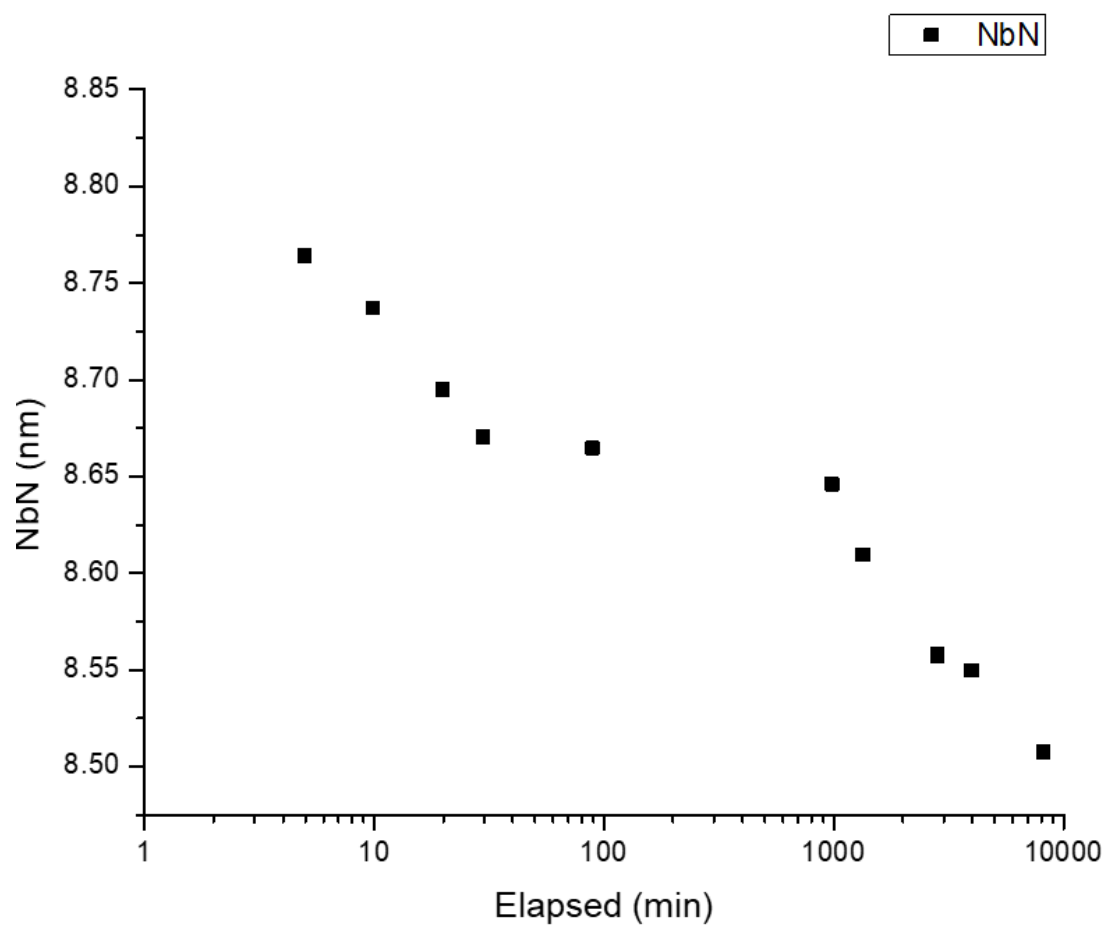
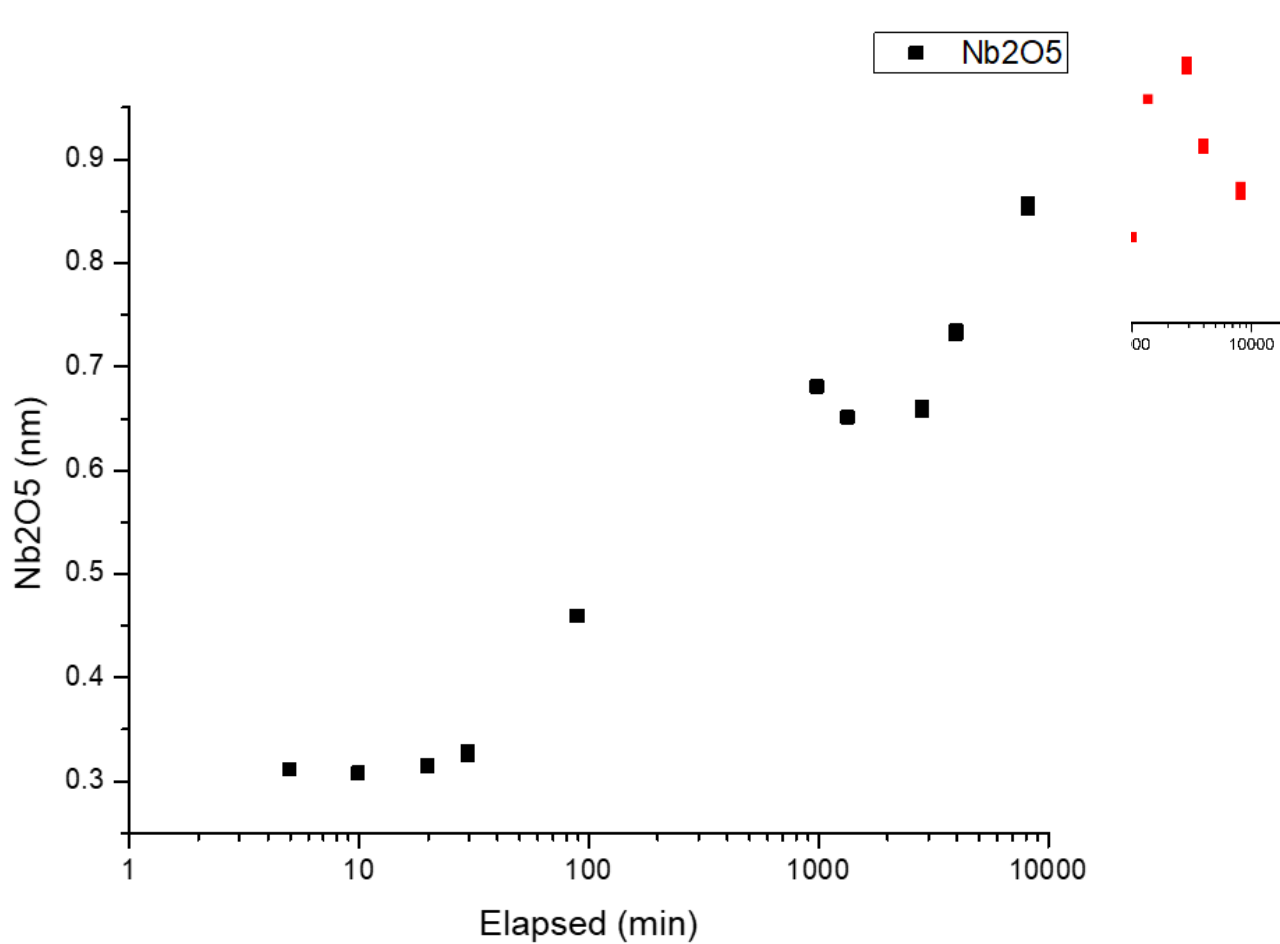
The sample was placed into a vacuum box as soon as the load lock was vented. Then brought to NSL to be measured on ellipsometer.

I made measurements after 0, 5, 10, 20, 30, 90 minutes, then overnight, ... continuously increasing the time between measurements.

The sample was stored in a 4×4 in the NSL (no vacuum).

x axis is elapsed time in minutes.





Effect of glass cover slip on etch rate

June 12, 2018

Categories: NbN deposition

If you've used the Plasma-Therm RIE in the NSL you have probably noticed a pile of glass slides and a note from Jim reminding users to remove the slide after use.

This slide is used to cover an opening where the RIE measures the DC bias, or etch voltage. This, in principle, is supposed to lower the voltage and increase the etch rate.

Process summary

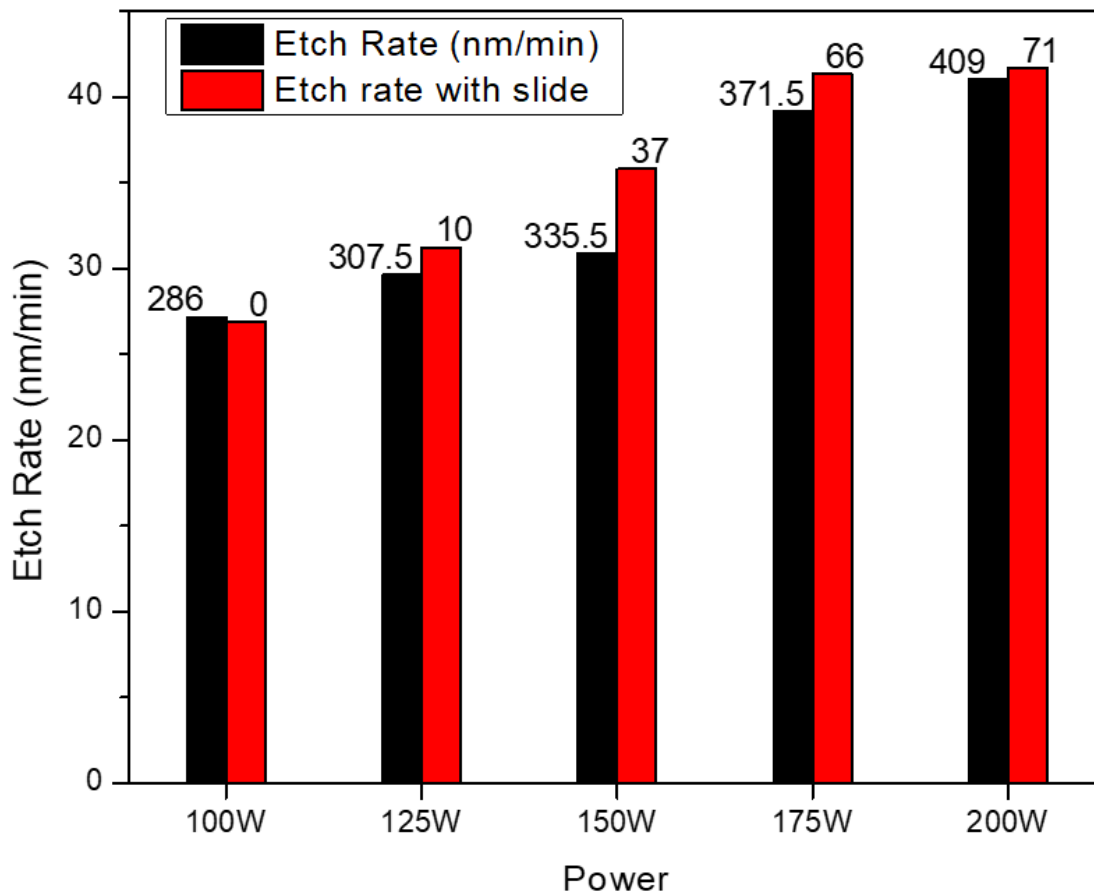
CF4 Etching SiN for 2 minutes.

Power >>100:25:200W

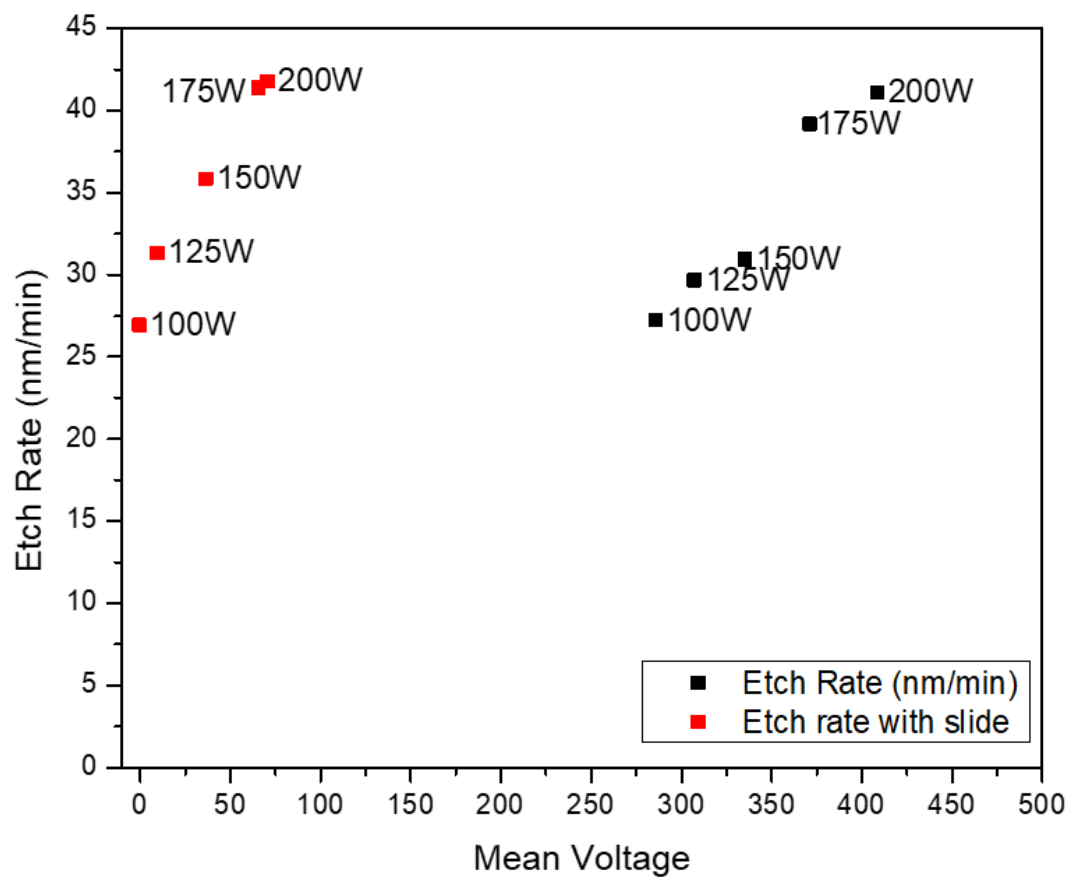
Two etches per power set point, with and without the slide.

Thickness measured on ellipsometer before and after each etch.

Minimum voltage and maximum voltage recorded during etch.



Labels are mean voltage.



Recap of events in RIE process monitoring

June 26, 2018

Categories: Fabrication, NbN deposition

2/20/2018

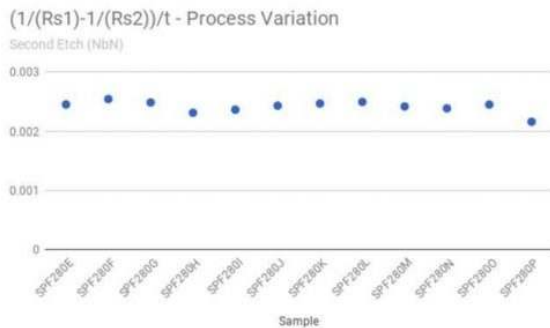
SPF280 1030s deposition – $R_s = 51 \text{ Ohms/sq}$

4/05/2018

1 minute, 50W etch (x2) DC Bias $\sim 174\text{--}180\text{V}$, sample measured on ellipsometer and four-point probe before and after each etch. Once a week.

Two etches were used to compensate for the oxide layer that could affect the sheet resistance. At this time, no ellipsometer model existed, so the etch rate was determined by an assumed resistivity which was calculated using an average of 6 XRR thickness measurements ($\rho \sim 3400$). This value has later been deemed incorrect.

Four samples were etched together, to remove the same amount of material(oxide). Then each sample was etched again individually.

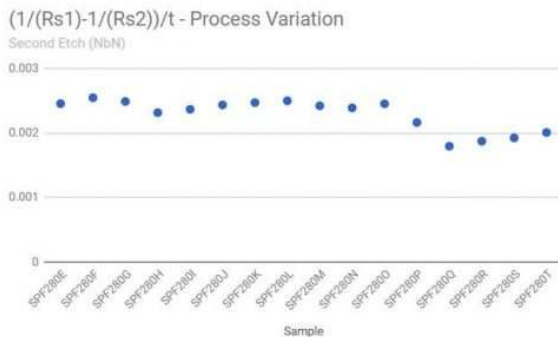


So far so good.

4/12/2018

SPF280K – first instance of voltage $> 180\text{V}$ (191V)

4/26/2018



$\sim 30\%$ drop in etch rate. Current age of NbN: 65 days

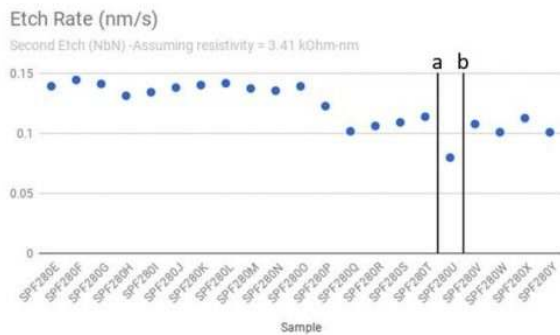
4/30/2018

Switch to daily etching. Samples are still etched twice/measured the same.

5/04/2018

a. Protocol change – daily etch starts

b. Maintenance – The wafer platen was visibly dirty and scratched. Jim installed a new wafer and cleaned the platen cover.



5/10/2018-5/29/2018

High voltage period 200-208V

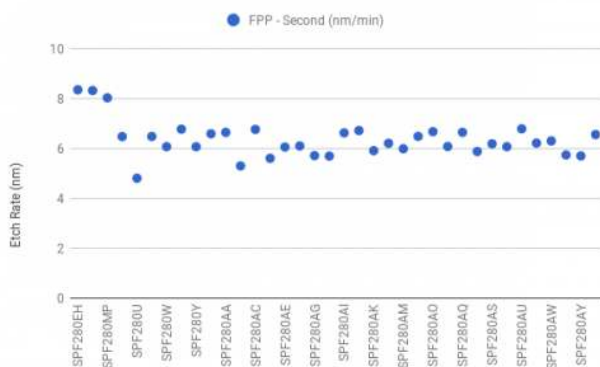
6/12/2018

Jim cleaned chamber. Between AW-AY

6/13/2018

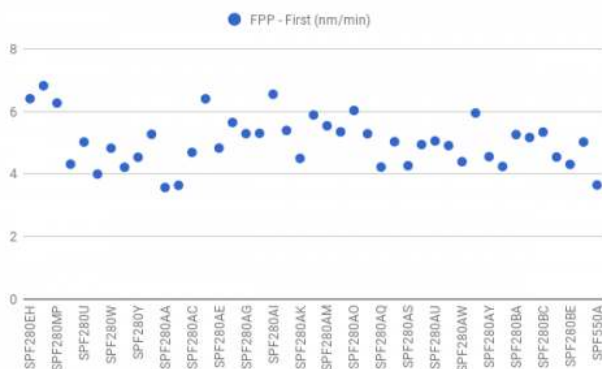
Unit change, nm/min. Etch continues, in line with previous estimates.

First 16 points were condensed into 4 points. The 4 sample process really only provided one data point, the average of each week. Shown as SPF280EH ... MP



6/14/2018

Switched to single etch process. Updated resistivity. First etch is generally (91.6% of the time) SLOWER by an average of 30%. Still within a typical range of 4-6nm per minute. Higher variance.



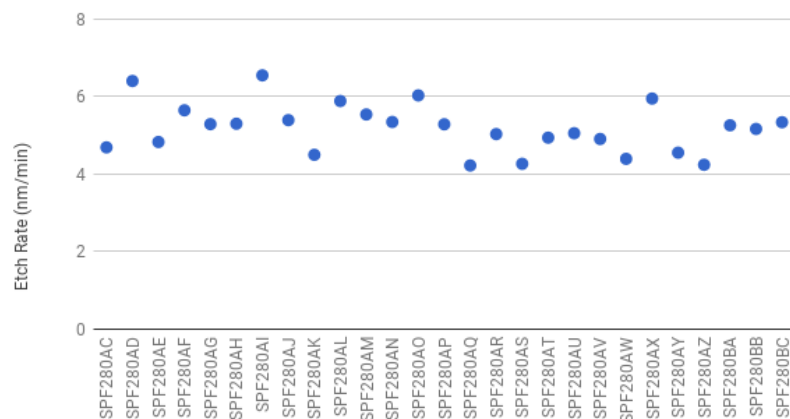
The first four points (average of EH->QT) look less abnormal.

6/15/2018

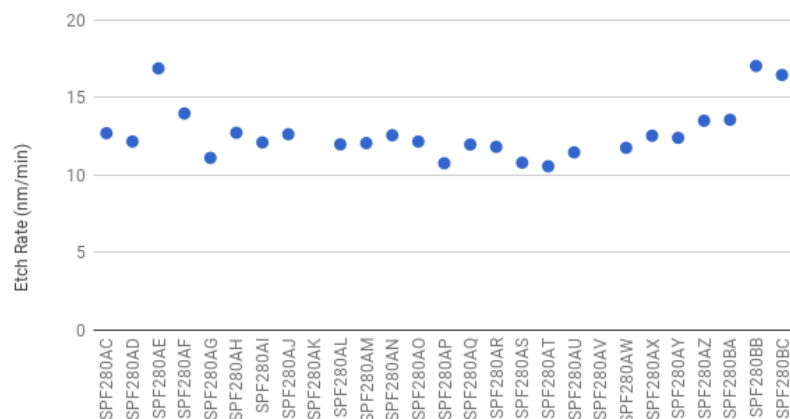
NbN layer model was used to reanalyze *all* ellipsometer data thus far. The second measuring method should tell us more about the problems we are seeing. Is the variance/30% drop due to measuring methods, film properties or process?

Sample range narrowed to AC-BC. Notice that they do not agree. Ellipsometer measurement has been validated using XRR. Maximum Fit Difference is ~2.8%.

FPP



Ellipsometer



Ellipsometer Data Sample

Filename	Fit_Diff	NbN	Nb2O5
20180614_SPF280BA_0	0.0136	55.357	0.711
20180614_SPF280BA_1	0.0201	42.489	0

Etch rate is calculated by finding the difference of the sum of each layer thickness NbN & Nb2O5 between measurements. Measurement seems typical, no oxide after etch. However, etching ~13 nm/min is unlikely.

6/19/2018 – 6/21/2018

Incorrect measurement three days in a row. Sent to Film Sense to diagnose. Fit Diff is normal.

Filename	Fit_Diff	NbN	Nb2O5
20180619_SPF280BD_0	0.0129	122.4	0.84076
20180619_SPF280BD_1	0.027	45.899	0

20180620_SPF280BE_0	0.0128	118.92	0.82744
20180620_SPF280BE_1	0.0307	52.253	0
20180621_SPF280BF_0	0.0129	118.51	0.69289
20180621_SPF280BF_1	0.0303	50.214	0

SPF280BF is the last sample of SPF280.

6/22/2018

New Wafer

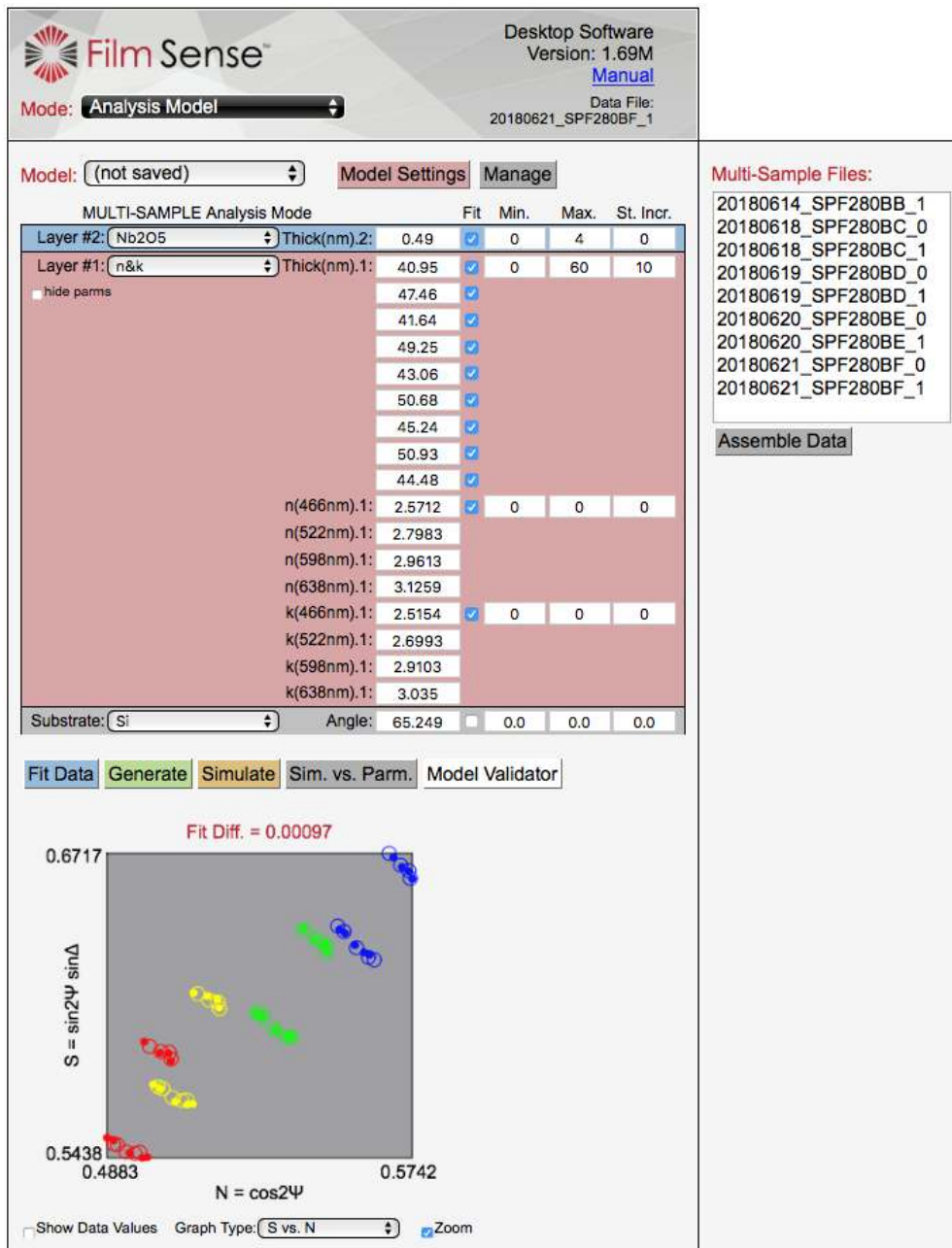
SPF550 1030s deposition – Rs = 47 Ohms/sq (6/20/2018)

Filename	Fit_Diff	NbN	Nb2O5	AlignX	AlignY	AveInt	Etch Rate (nm/min) – Ellipsometer	R1	R2	Etch Rate (nm/min) – FPP
20180622_SPF550A_0	0.0083	40.052	1.9158	0.005	0.006	15.374		12.91	12.8	
20180622_SPF550A_1	0.0073	35.653	1.0246	0.008	0.006	15.517	5.2902	14.08	14.18	6.262270438
20180625_SPF550B_0	0.0081	39.748	2.0883	0.007	0.001	15.346		12.37	12.28	
20180625_SPF550B_1	0.0074	36.158	1.0173	0.004	0.005	15.473	4.661	13.64	13.66	7.026388773

Etch rates are now similar but do not agree (increase/decrease). The ellipsometer no longer measures 0nm oxide after the etch (same model).

6/24/2018

Film-Sense adds a new feature to the software allowing for multiple layers to be fit using the multi-sample analysis thickness measurement. The model is recreated and data reanalyzed.



6/25/2018

The new model showed an average etch rate of 6.232 nm/min while the FPP showed an average of 3.736 nm/min using $\rho = .24935 \mu\Omega\text{-cm}$.

These numbers are closer but they do not show the same trend. Between measurements, the change in etch rate only agrees 48% of the time.

Possibility of changing resistivity

Max Fit Dif: 0.01

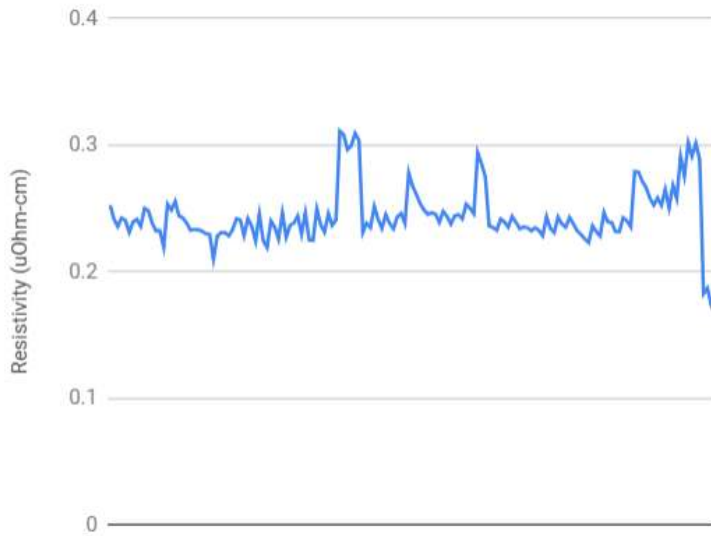
Using the thickness of the just NbN from the ellipsometer, the calculated resistivity decreased by an average of 5.7% after the etch.

There is also a big difference between wafers.

Deposition	Rs Ohm/sq	Resistivity uOhm-cm
SPF280	51	0.2628

SPF550	47	0.1803
--------	----	--------

Resistivity ($\mu\text{Ohm-cm}$)



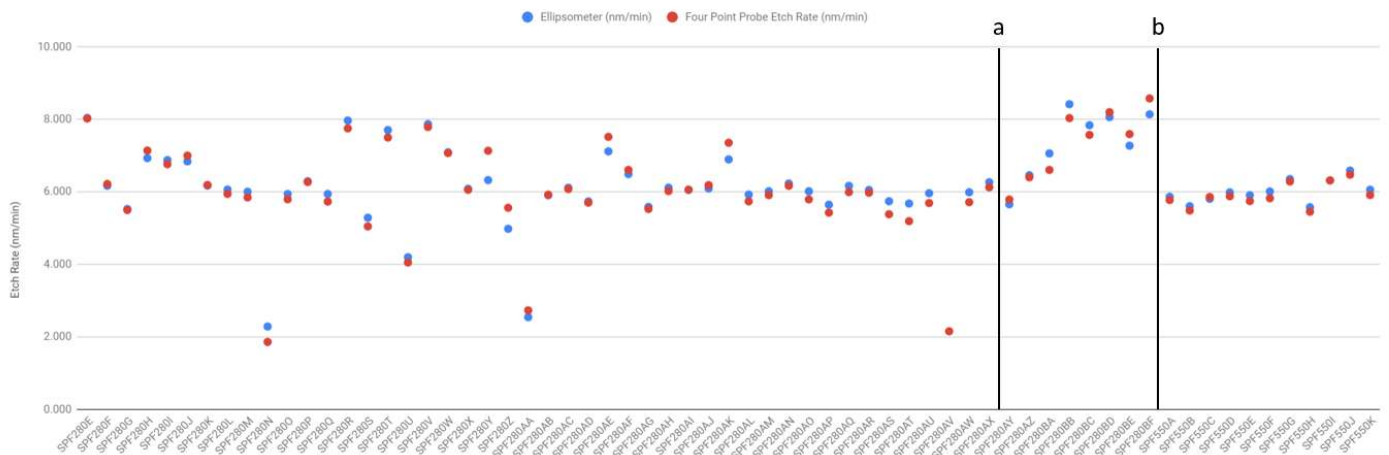
*axis- sample

We are far into the saturated region for resistivity as a function of thickness. Should be constant after $\sim 20\text{nm}$.

6/27/2018

Etch Rate of NbN

CF4 | 10mTorr | 50W | 1 min



a. chamber cleaned

b. **new sample**

The FPP etch rate was calculated using two different resistivities. The first resistivity was calculated using the thickness of NbN while the second resistivity was calculated using the thickness of NbN + Oxide.

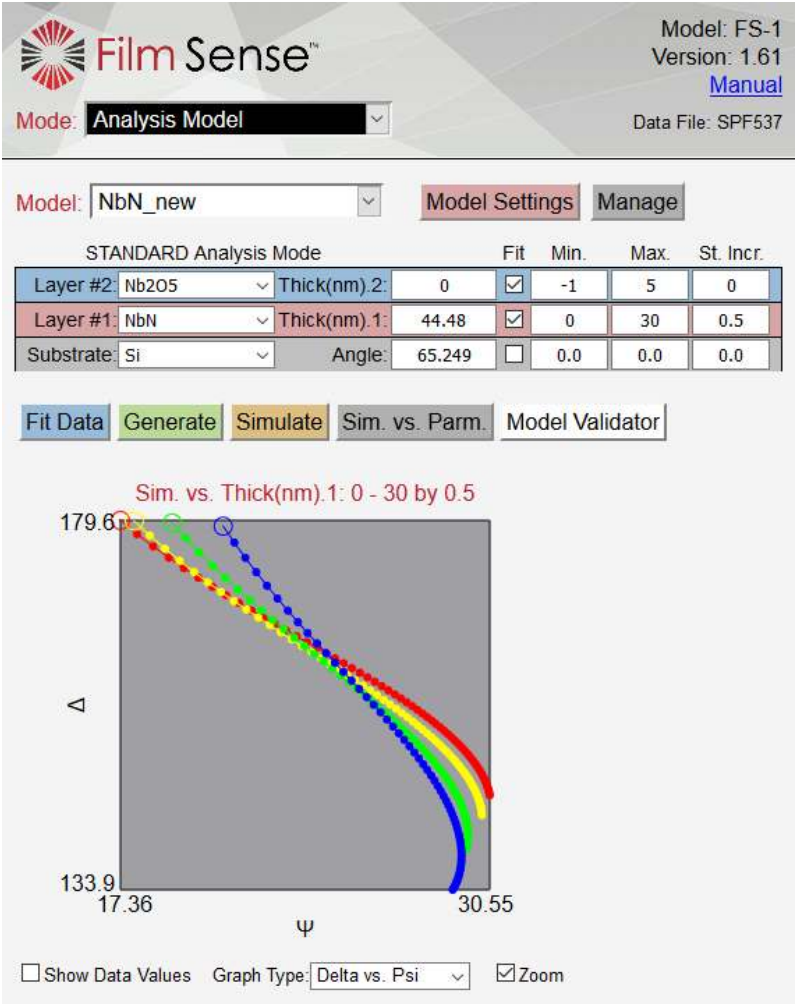
The entire set was shifted by $+2.155\text{nm}$ (the average difference between etch rates).

The resistivity for SPF550 was calculated using NbN+Nb₂O₅.

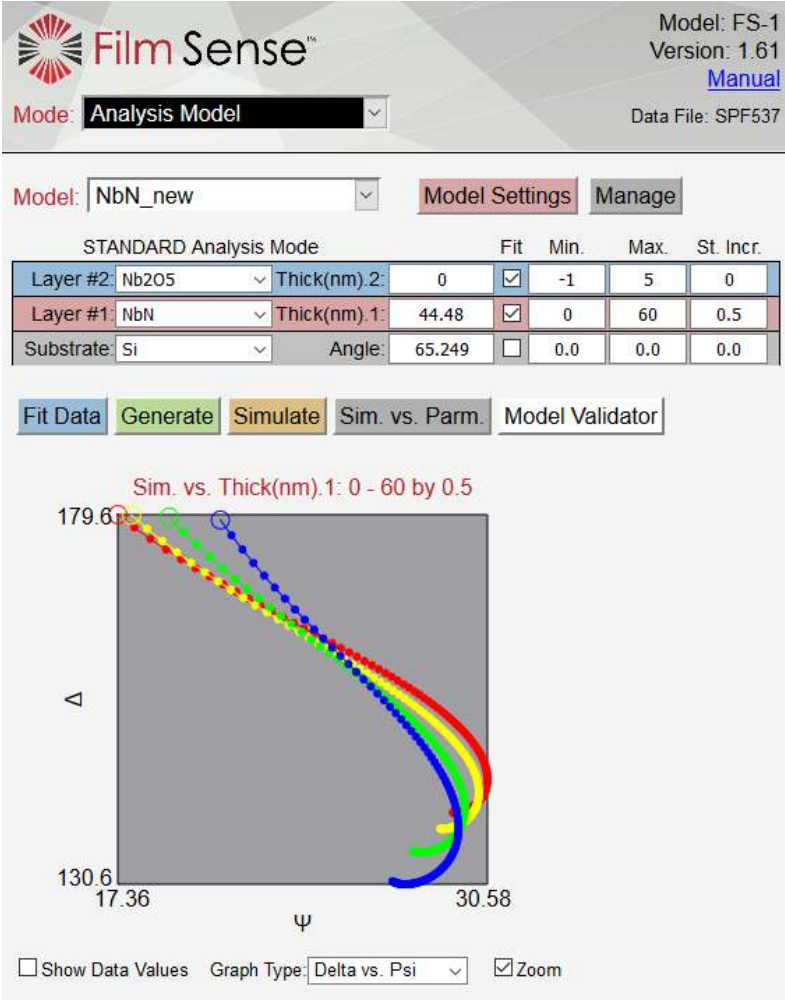
Due to the absorbing nature of NbN the maximum measurable thickness is $\sim 50\text{nm}$.

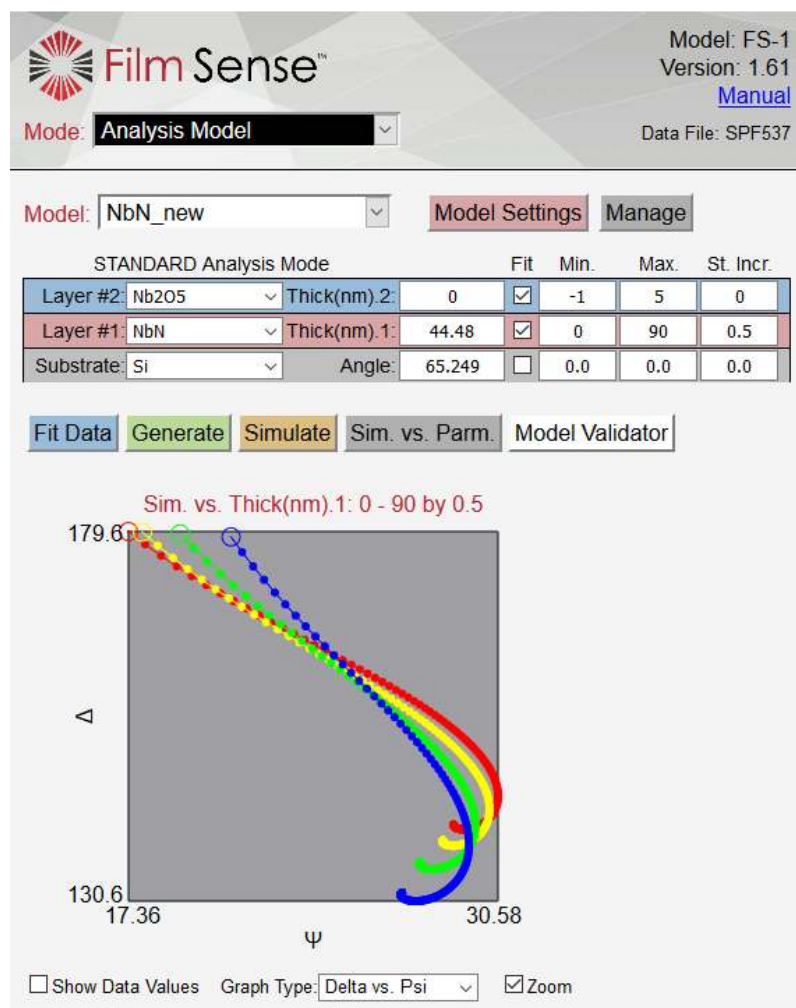
Psi-Delta plots to show absorbing limit.

30nm

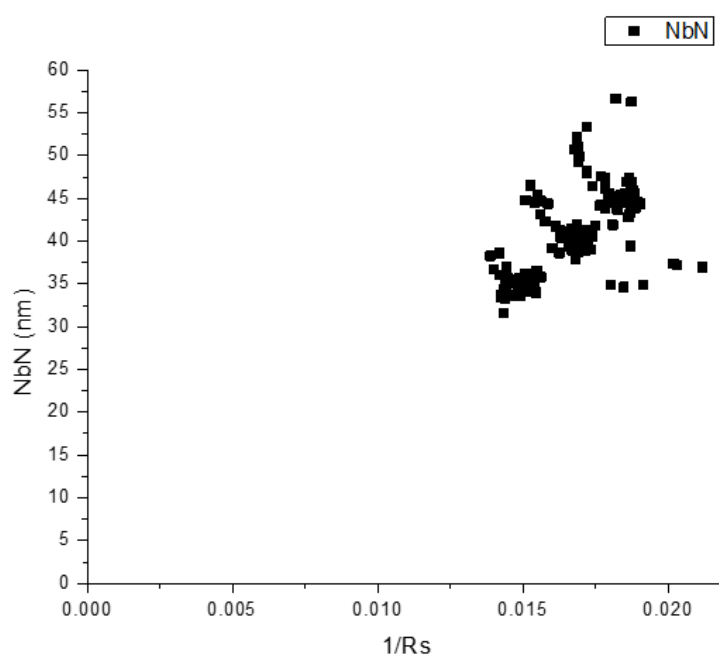


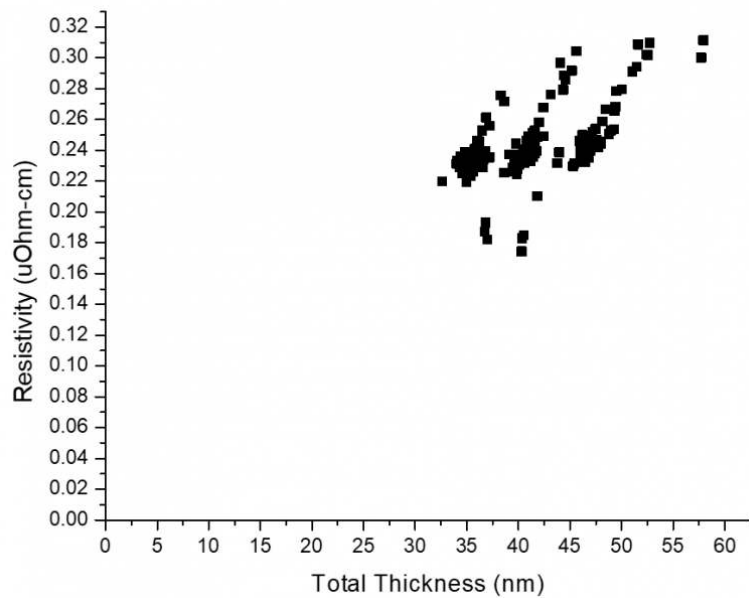
60nm





Thickness vs $1/R_s$ from all measured data.

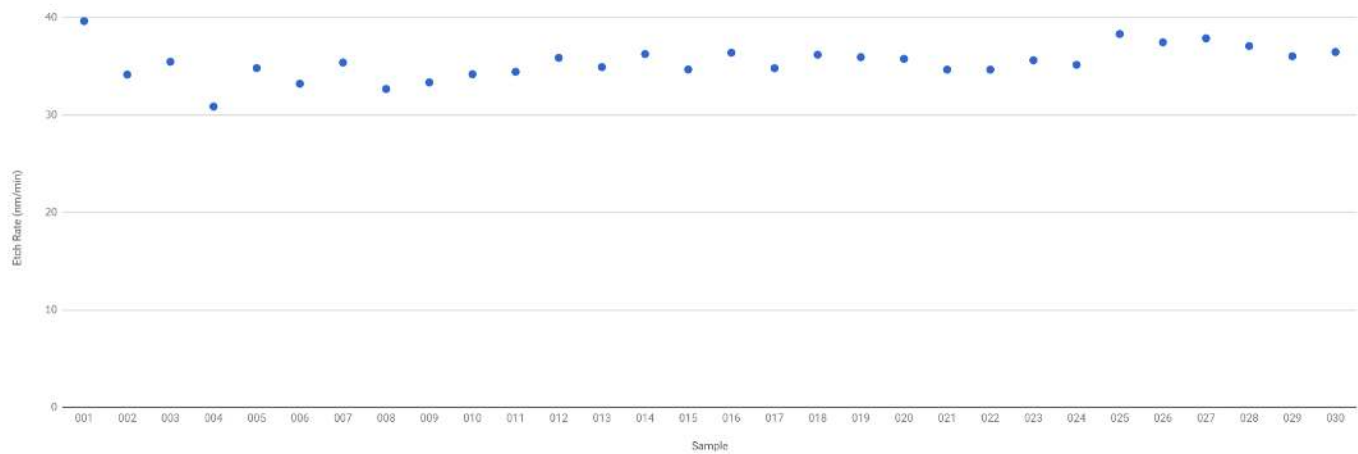




Resistivity on average decreases by 3.4% after etching.

SiN

Etch Rate of SiN
CF4 | 10mTorr | 150W | 2 min



If the etch rate of NbN increases does the etch Rate of SiN increase? – 72.4% of the time.

If the voltage increases from the previous day, does the etch rate increase? – 41.2% (NbN), 48.3% (SiN)

On average, if the voltage is high is the etch rate high? – 58.3% (NbN, SPF550), 75.9% (SiN)

effect of segmented etches

July 2, 2018

Categories: Fabrication

Often, we will break up long etches into shorter etches to avoid burning resist. The following experiment compares a single etch with three combined etches. The total time, the power setpoint, and the material were parameters of interest. All thicknesses were measured on the ellipsometer in the NSL.

NbN (max fit diff: 0.0133)			
	totaltime_power_NumberOfEtches	Etch Rate (nm/min)	Percent Change (%)
Increased Power	3M100W_1	8.6966	
	3M100W_3	10.2329	17.6655
Baseline	3M50W_1	3.2897	
	3M50W_3	3.6067	9.6350
Increased Time	6M50W_1	5.2928	
	6M50W_3	5.4810	3.5574

SiN (max fit diff: 0.0027)			
	totaltime_power_NumberOfEtches	Etch Rate (nm/min)	Percent Change (%)
Increased Power	3M100W_1	24.6633	
	3M100W_3	29.0520	17.7943
Baseline	3M50W_1	13.9067	
	3M50W_3	16.5180	18.7776
Increased Time	6M50W_1	13.4262	
	6M50W_3	14.6765	9.3127

The voltage for the second and third etch did not begin at the typical minimum value. Instead, the latter etches skipped the ramp-up period. A possible explanation for the increased etch rate.

3M50W_3					
1st		2nd		3rd	
Min	Max	Min	Max	Min	Max
162	190	179	196	176	194

NSL four point probe

July 3, 2018
Categories: Fabrication, NbN deposition

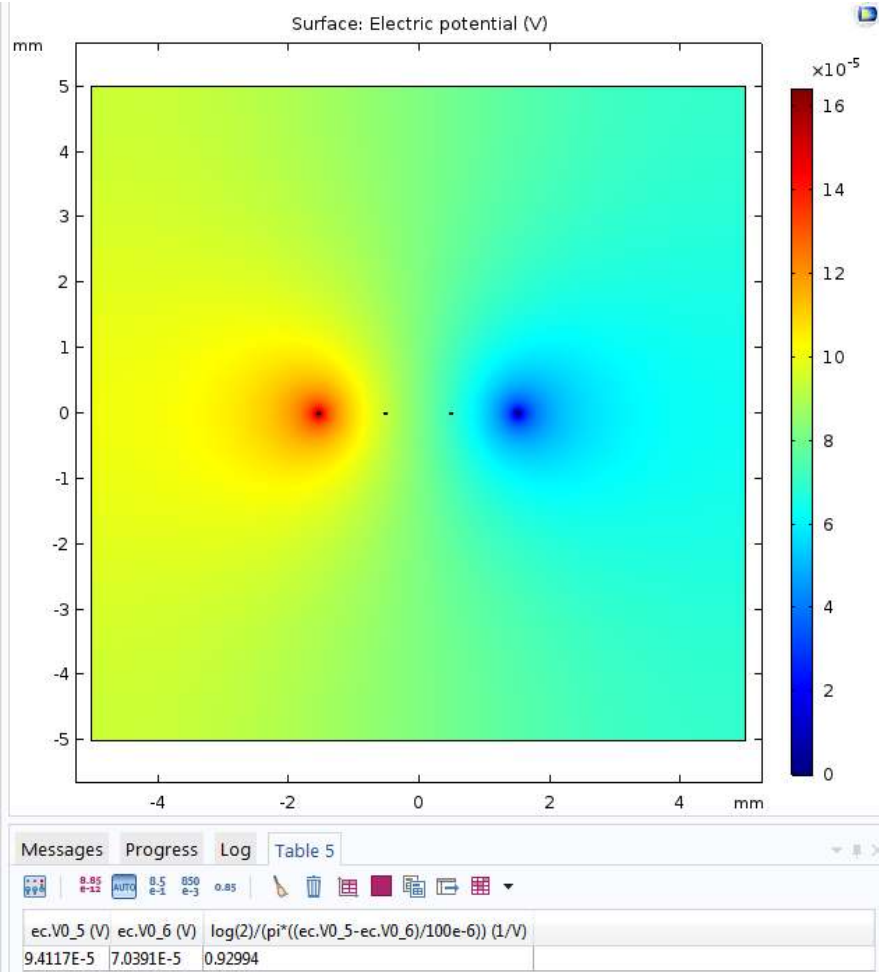
KSR-4 Four Point Probe Stand

- Lever Driven Up/Down
- Square Chuck
- 6" Wafer Carrier
- Z Up/Down 30 mm Travel
- Z Up/Down 20 μm Resolution

SR-H62 Four Point Probe Head

- Individual Spring Probes
- Gold Plated BeCu Tips
- 1000 μm Pin Spacing
- 40.6 μm Pin Diameter

Correction coefficient for 1cm x 1cm sample: 0.92994



Process for determining AJA deposition time

March 14, 2019

Categories: NbN deposition

Intro

The deposition time is most important (and only) user determined parameter when we are performing the standard NbN deposition. We use the sample database get a feel for what length of time would produce the desired parameter, typically sheet resistance or thickness. To be more thorough in our approach I extracted a few key relations between: time, deposition rate and **drops in deposition voltage**, and shared them below.

Procedure

Thickness – Rs

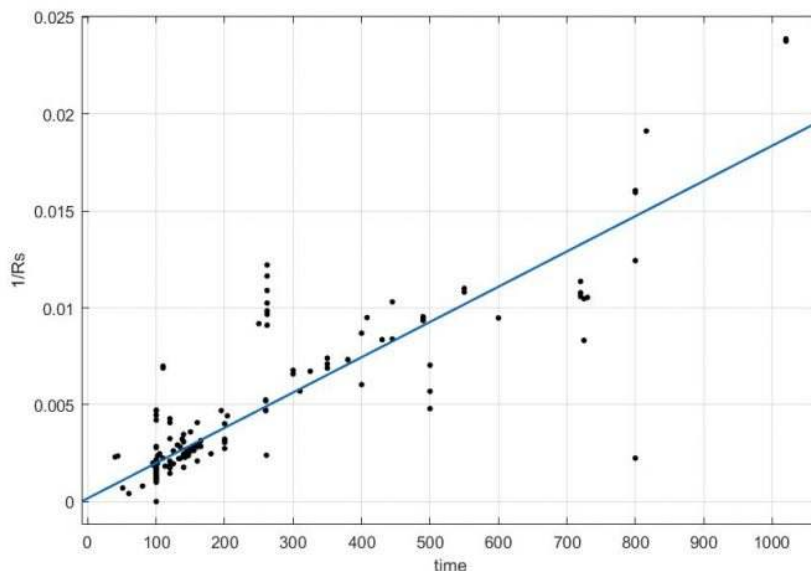
If a similar deposition has not been made use the relation $\rho = R_s * d$ to approximate the sheet resistance using the desired thickness d and an assumption of NbN resistivity ρ .

NbN Resistivity $\rho \sim 2447 \text{ } \Omega\text{-nm}$.

Rs – Deposition time. The graph contains data for NbN on SiO₂ depositions for 2018.

The fit line is the relation:

$$1/R_s = 1.818 \cdot 10^{-5} \cdot \text{time}(\text{seconds})$$



Time Correction

Depending on your accuracy needs it is likely that you will not be successful your first try and will have to adjust the deposition time.

*time=new time

Target Erosion Correction

Iron man tests showed that as the target erodes the voltage drops (usually 1-2V) and the deposition rate decreases. This step is only necessary for highly critical depositions, in general the target erosion is small. Slope is a characteristic of target,

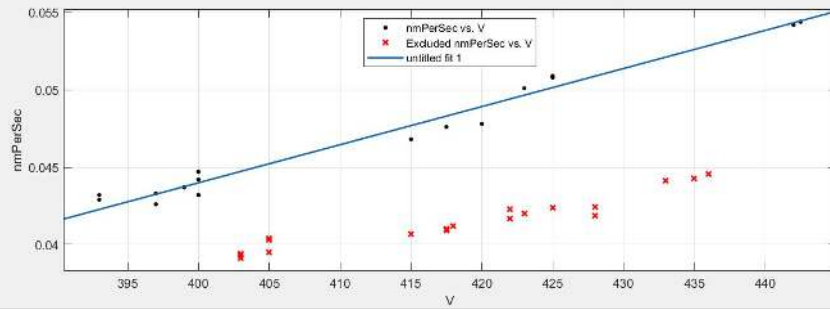
$$\Delta D(\text{nm/s}) = p_1 \Delta V$$

$$p_1 = 2.462 \cdot 10^{-4}$$

Results

Linear model Poly1:
 $f(x) = p1 \cdot x + p2$
 Coefficients (with 95% confidence bounds):
 $p1 = 0.0002462 \ (0.0002241, 0.0002683)$
 $p2 = -0.05448 \ (-0.06359, -0.04537)$

Goodness of fit:
 SSE: 7.795e-06
 R-square: 0.9721
 Adjusted R-square: 0.9703
 RMSE: 0.000698

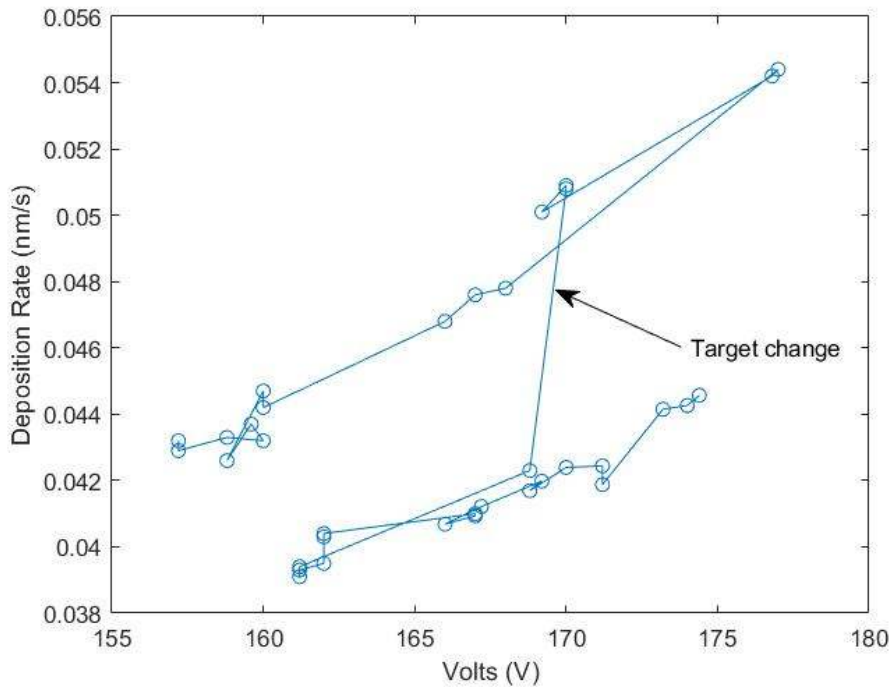
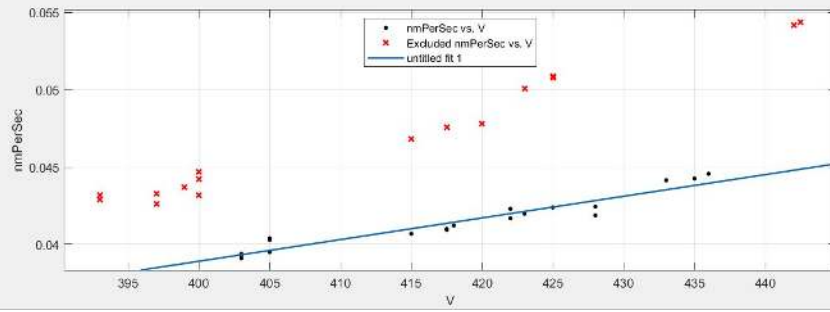


$$p2 = 1.402 \cdot 10^{-4}$$

Results

Linear model Poly1:
 $f(x) = p1 \cdot x + p2$
 Coefficients (with 95% confidence bounds):
 $p1 = 0.0001402 \ (0.0001193, 0.000161)$
 $p2 = -0.01715 \ (-0.02587, -0.00843)$

Goodness of fit:
 SSE: 3.878e-06
 R-square: 0.922
 Adjusted R-square: 0.9175
 RMSE: 0.0004776



Conclusion

This information should aid a new user or new process that requires an uncommon thickness or Rs. All thicknesses were measured on the ellipsometer using NbN_SiO2_test4. The resistivity is an approximation that will increase for thinner films. Resistivity closer to $\sim 2675 \Omega\text{-nm}$ might be more appropriate for $\sim 5\text{nm}$ films.

Termotek chiller

May 23, 2019

Categories: Lab

Ultrafast Lab laser chiller.

Termotek ag P308-15054

Flow meter – 4F23D35

Flow meter reading decays over time (3.4L/min→0) while other flow meters read a steady 4L/min. No sign of damage on flow meter, could be a controller problem. Because of the redundant flow meters, no replacement will be sourced at this time. To prevent alarms from the chiller the minimum flow threshold will be set to zero.









Wire Bonder Tip

July 18, 2019

Categories: nTron

Tried out Andrew's cell phone camera adapter for the microscope. Here are some pictures of the wire bonder tip. Wire bonder wedge

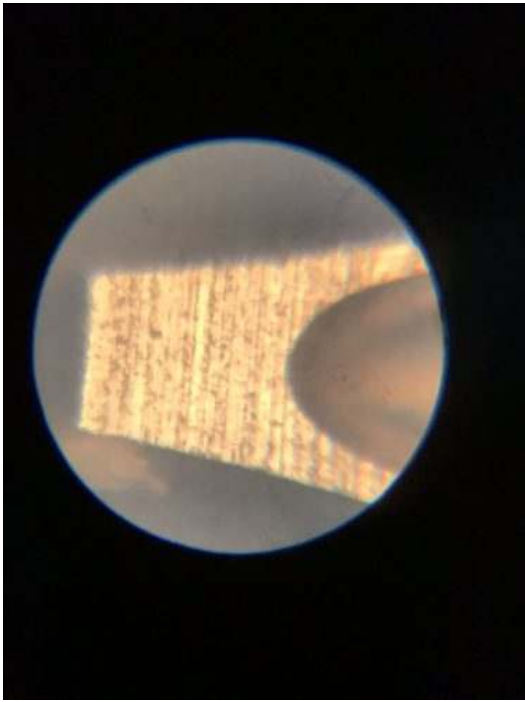
Old Tip



Broken tip



New Tip



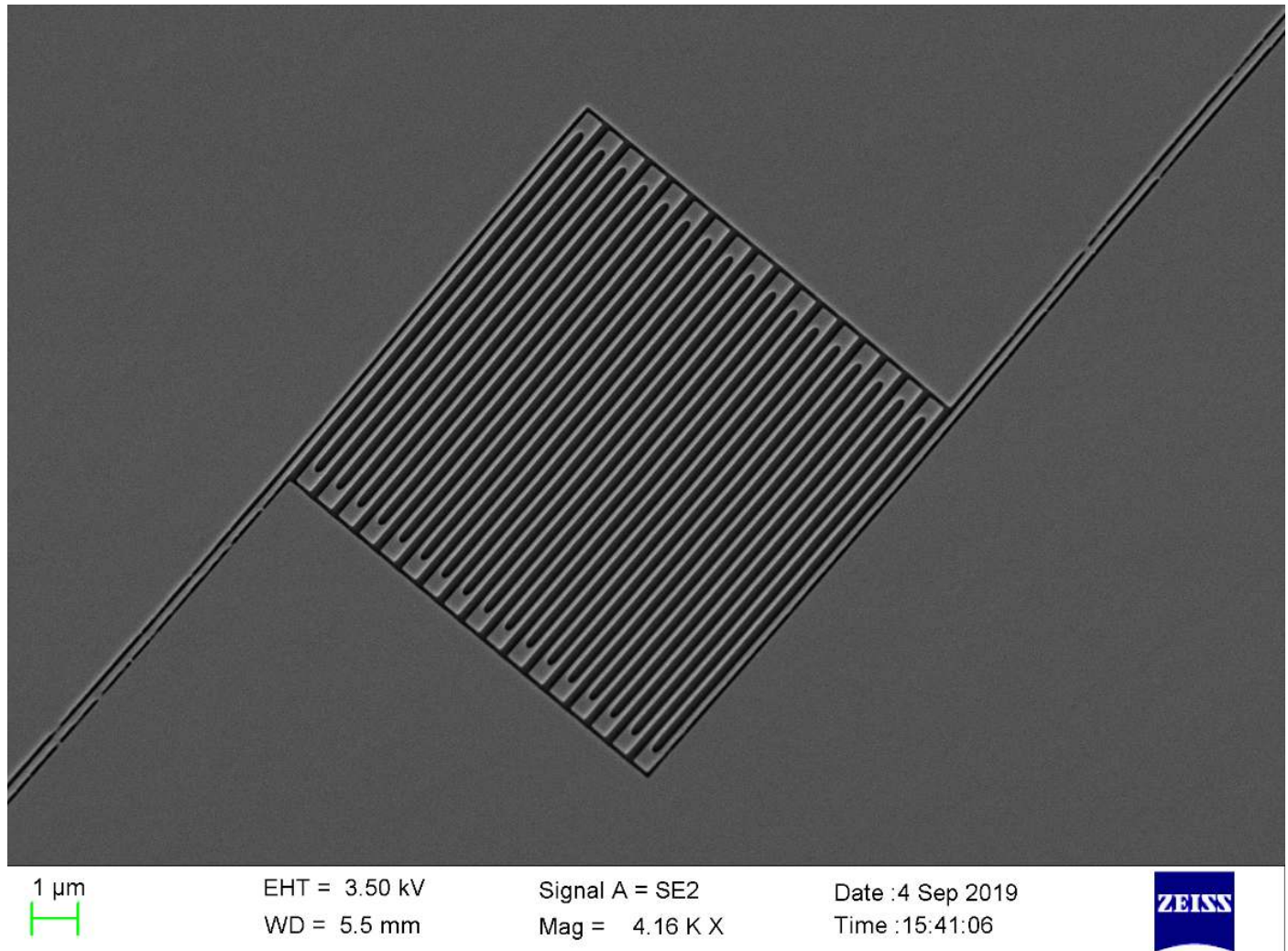
10x10um snspd (standard process)

September 24, 2019

Categories: SNSPD

SPG122 Rs=350ohms/sq

SEM



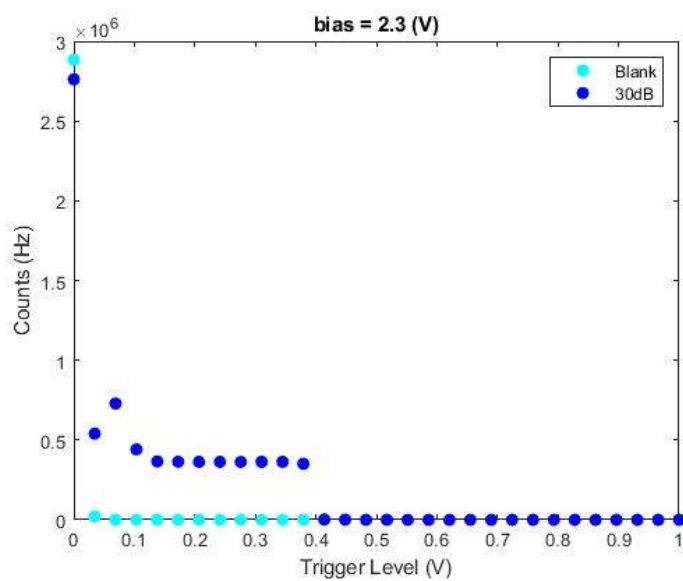
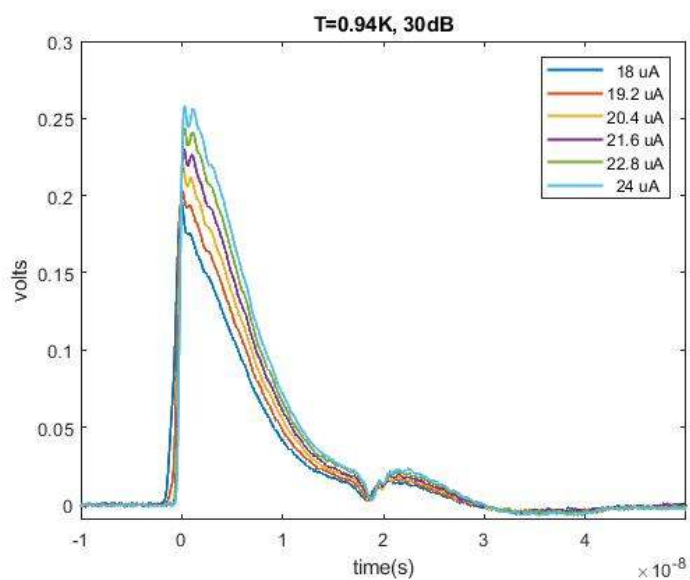
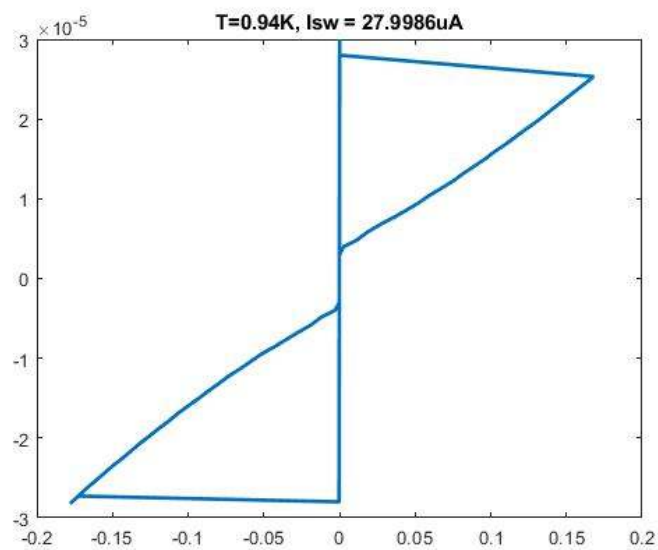
Clearly some shorted points along the taper. Total yield was 3/16.

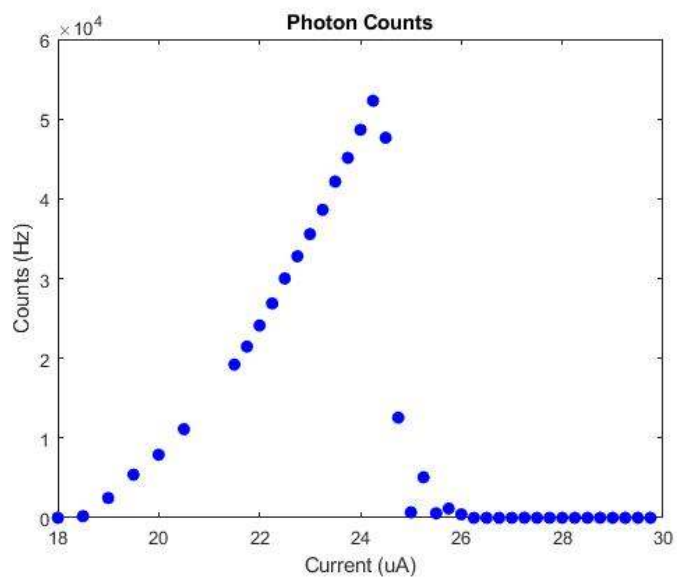
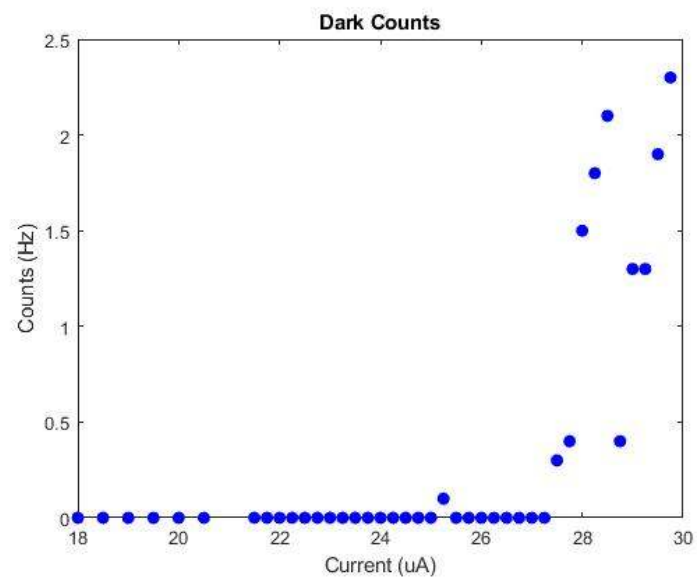
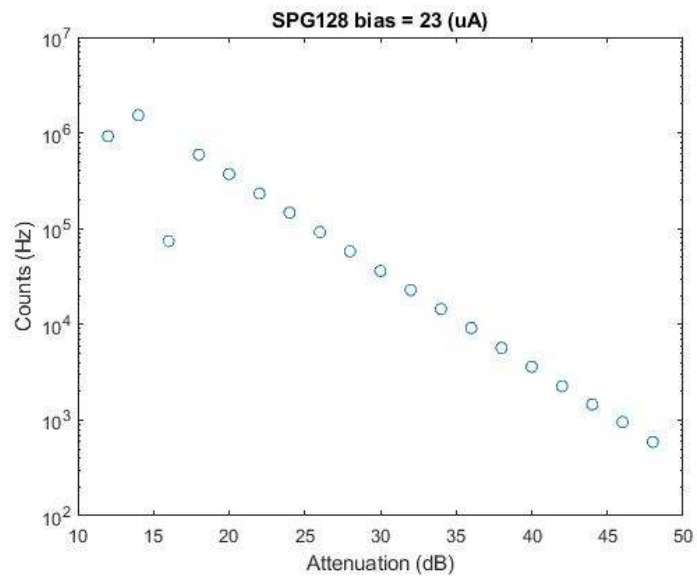
ZEP 5kRPM spin, 500uC/cm²

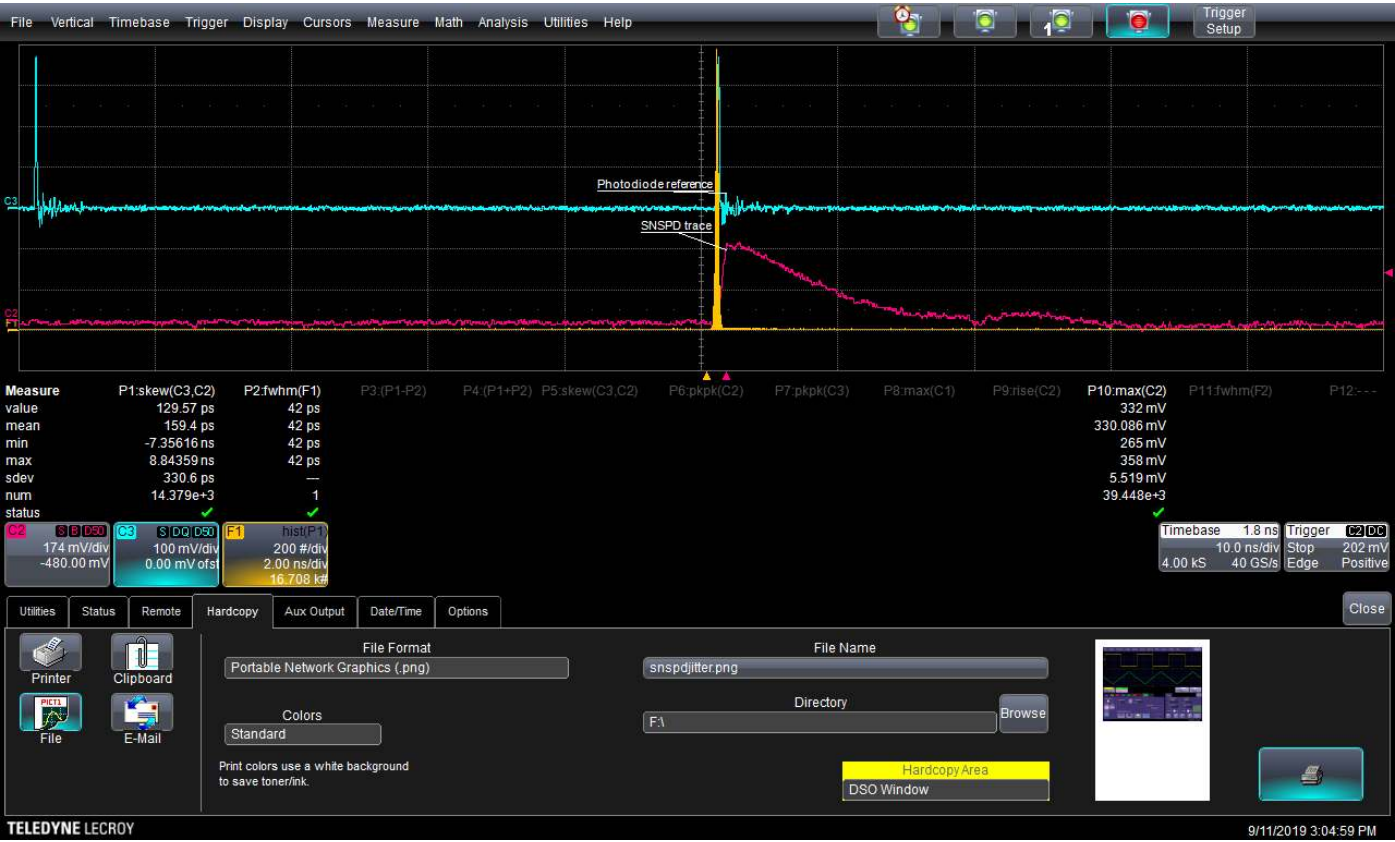
Cold Develop – 90s @ 5°C followed by 30s in IPA

Etch 3min @ 50W, (3*1min)

Strip in NMP overnight







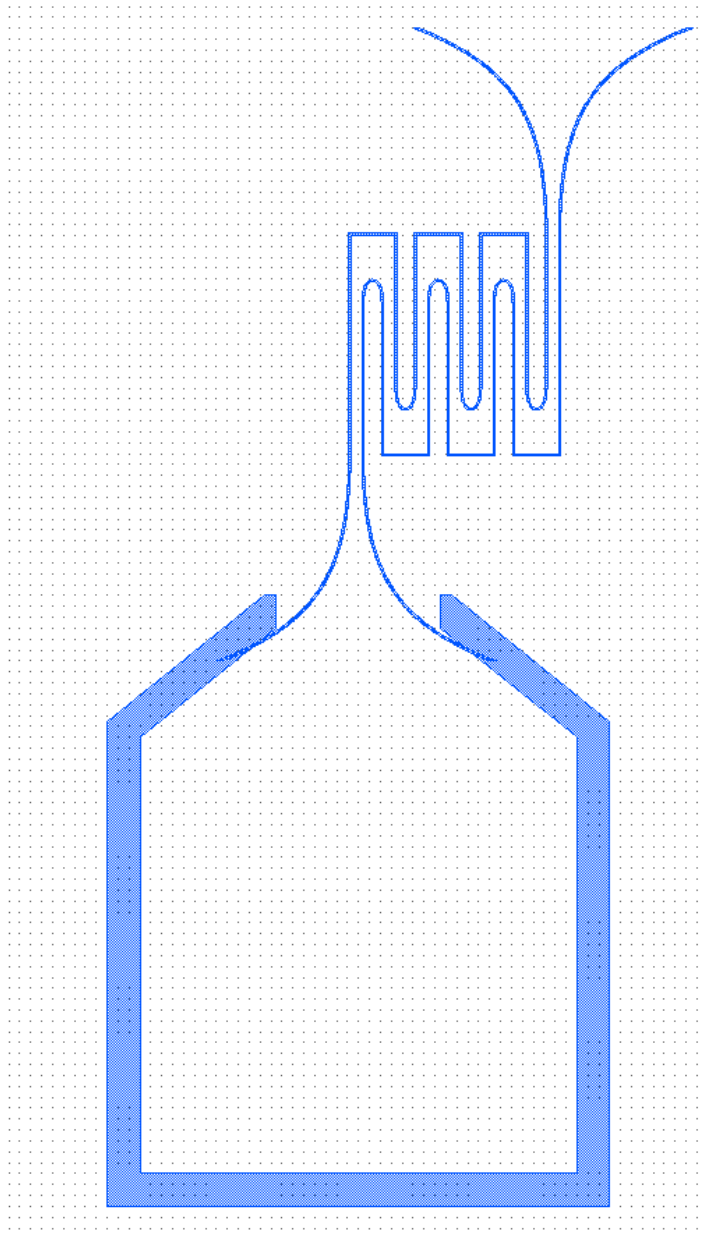
Thin Detector

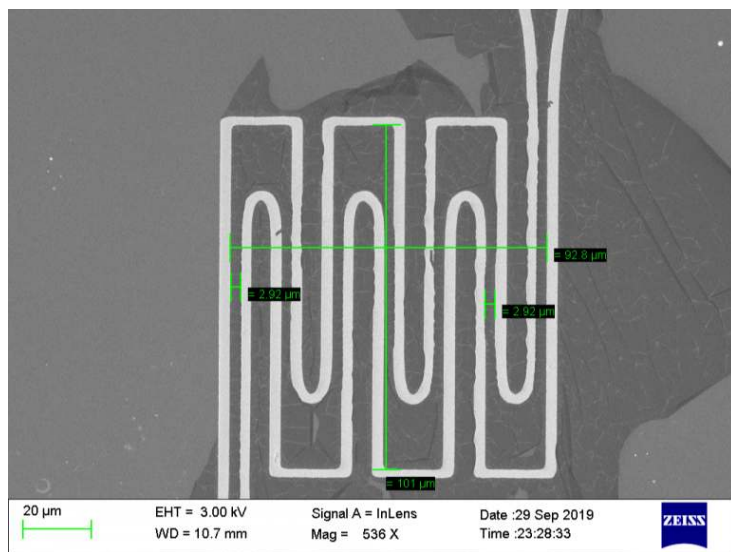
September 24, 2019

Categories: SNSPD

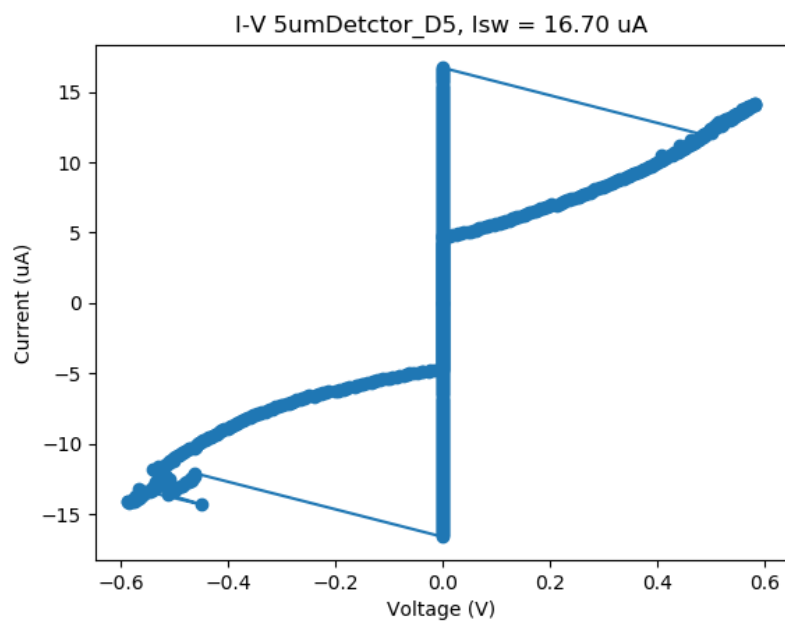
SPG144 2.5nm $T_c=4.5$

3um wire, 15um pitch. 100umx100um

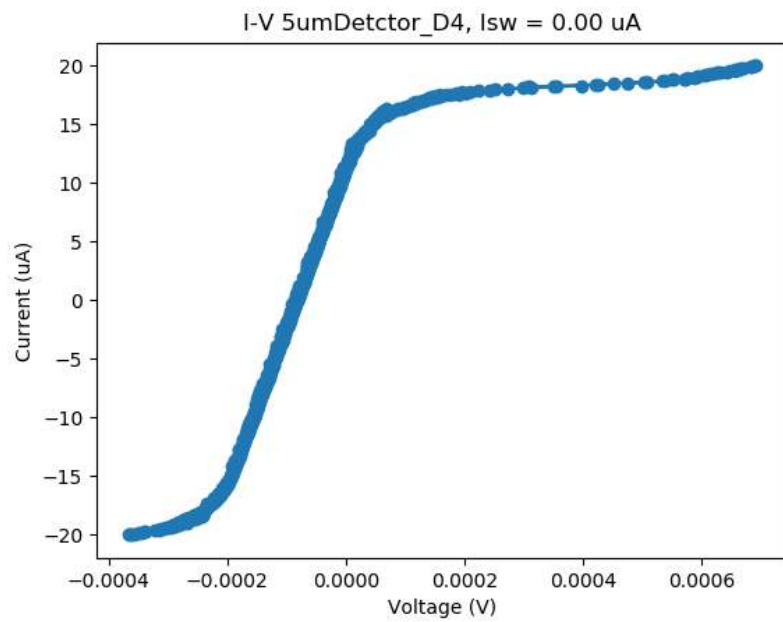




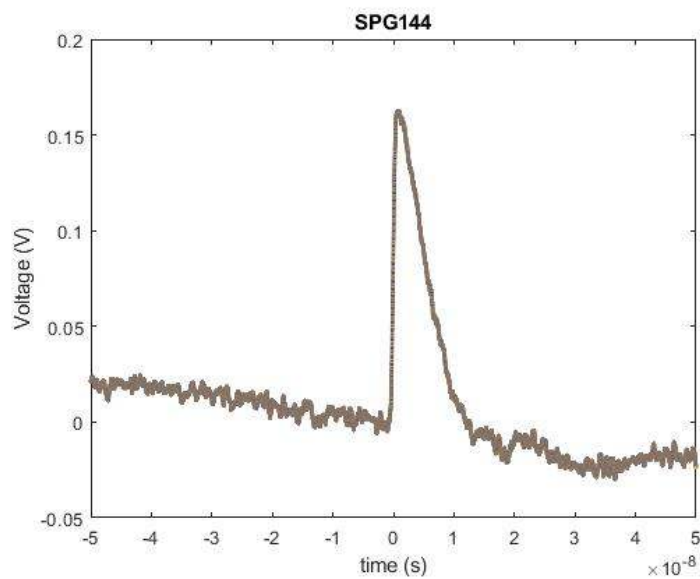
2.9um wire



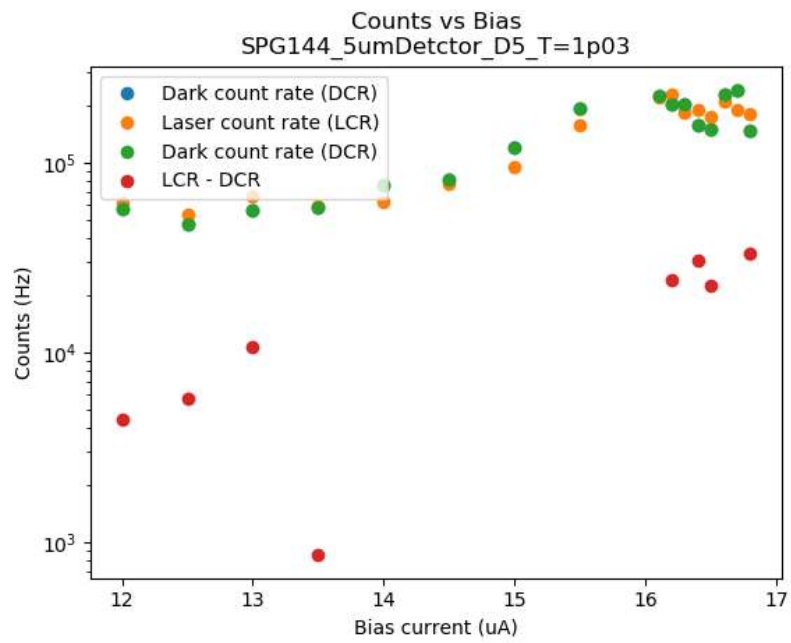
With 500hm shunt



Pulse trace



Only dark counts



Pearl Length

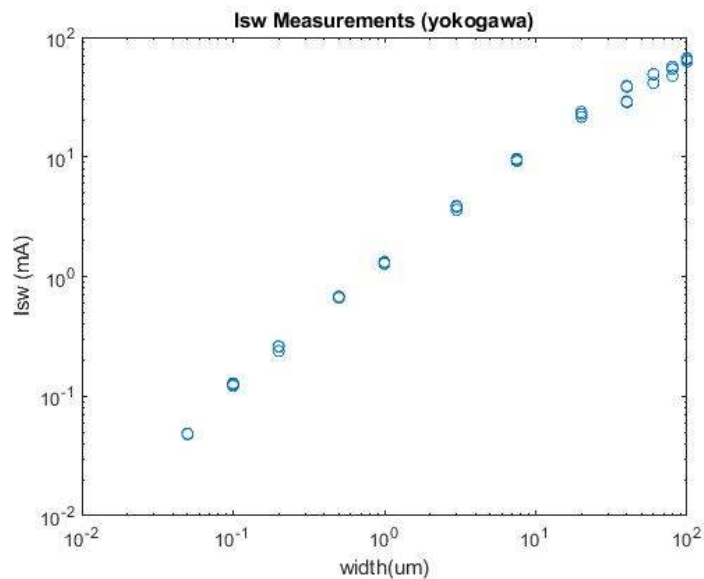
September 25, 2019

Categories: Materials, NbN deposition, Superconductivity

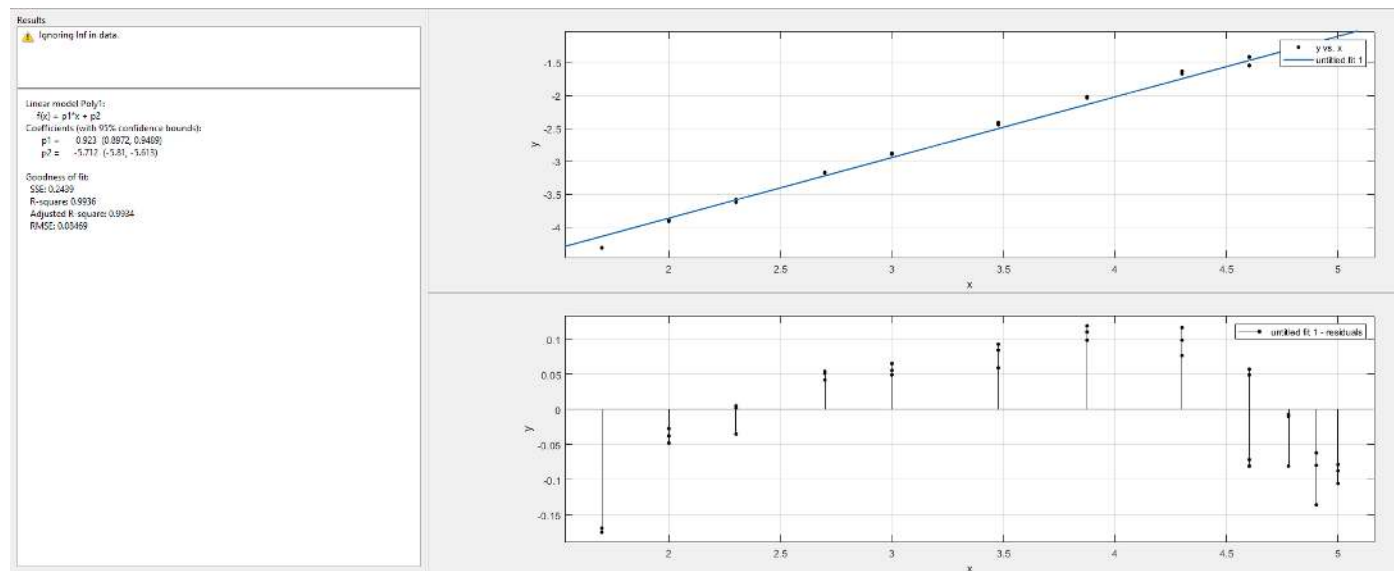
Final measurements

$T_c = 9.77\text{K}$

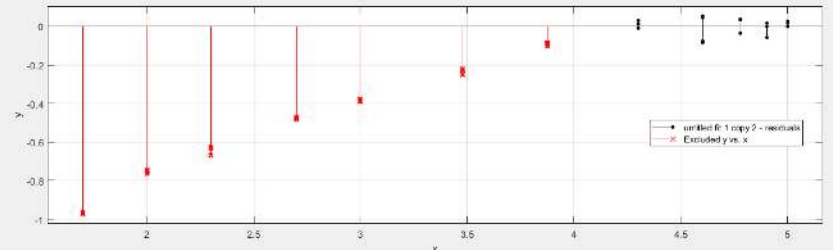
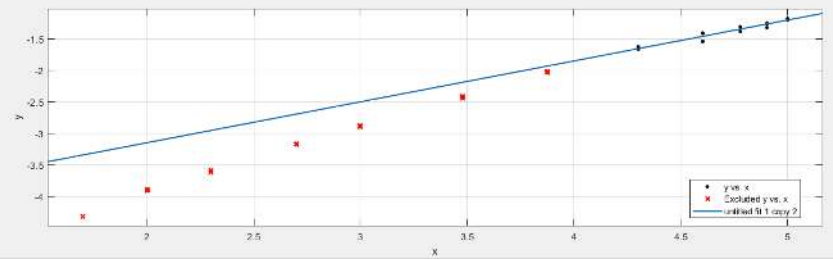
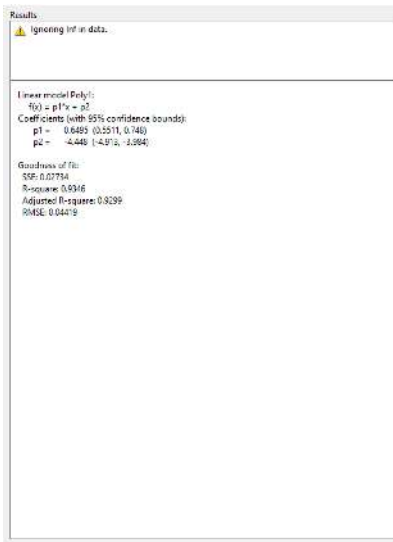
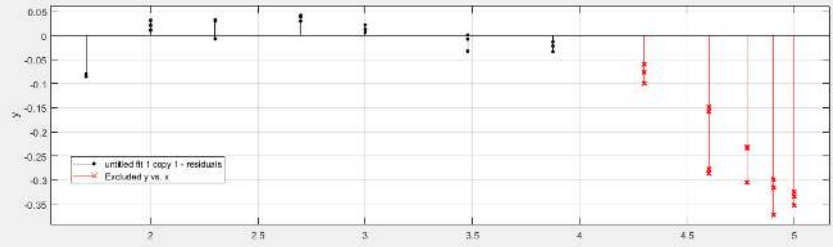
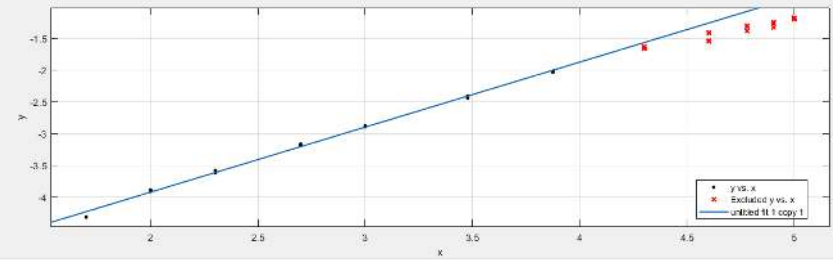
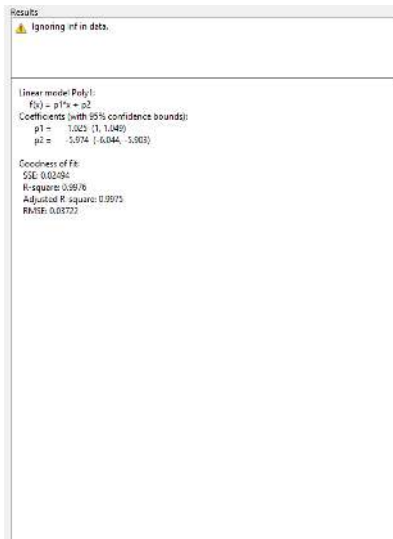
Probe station $T = 4.89\text{K}$ at sample stage.



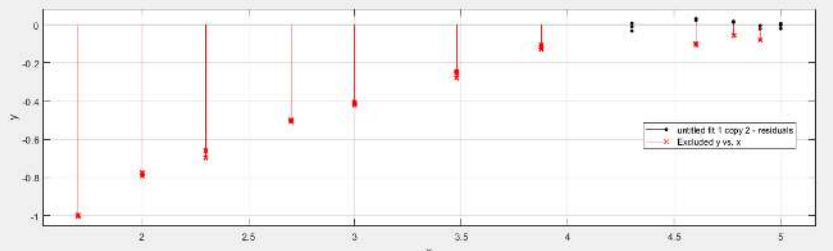
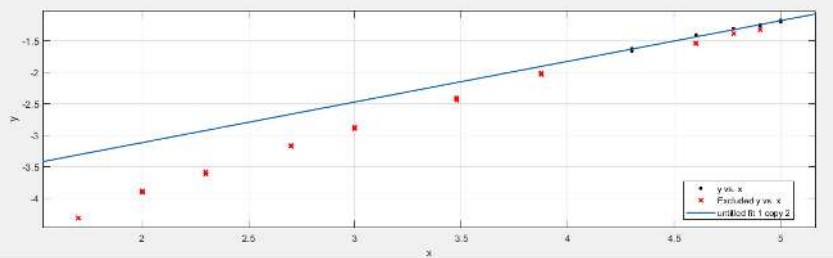
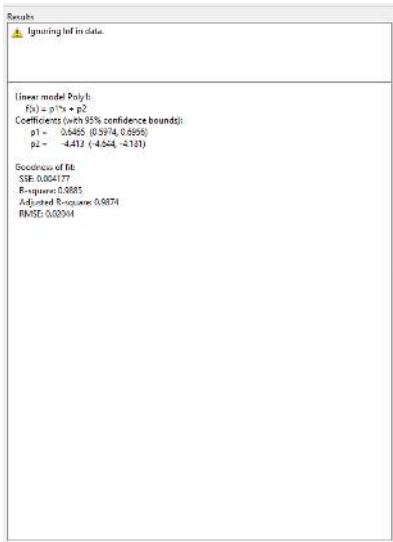
Looks linear. rather a power function.



Clear peak in the residuals around 4. Signaling some saturation. I tried to isolate each region.



The three extra points were excluded due to a change in radiation shield temperature. Possible other points for narrow wires were also at higher temperature (35K vs 26K) but there is little difference.

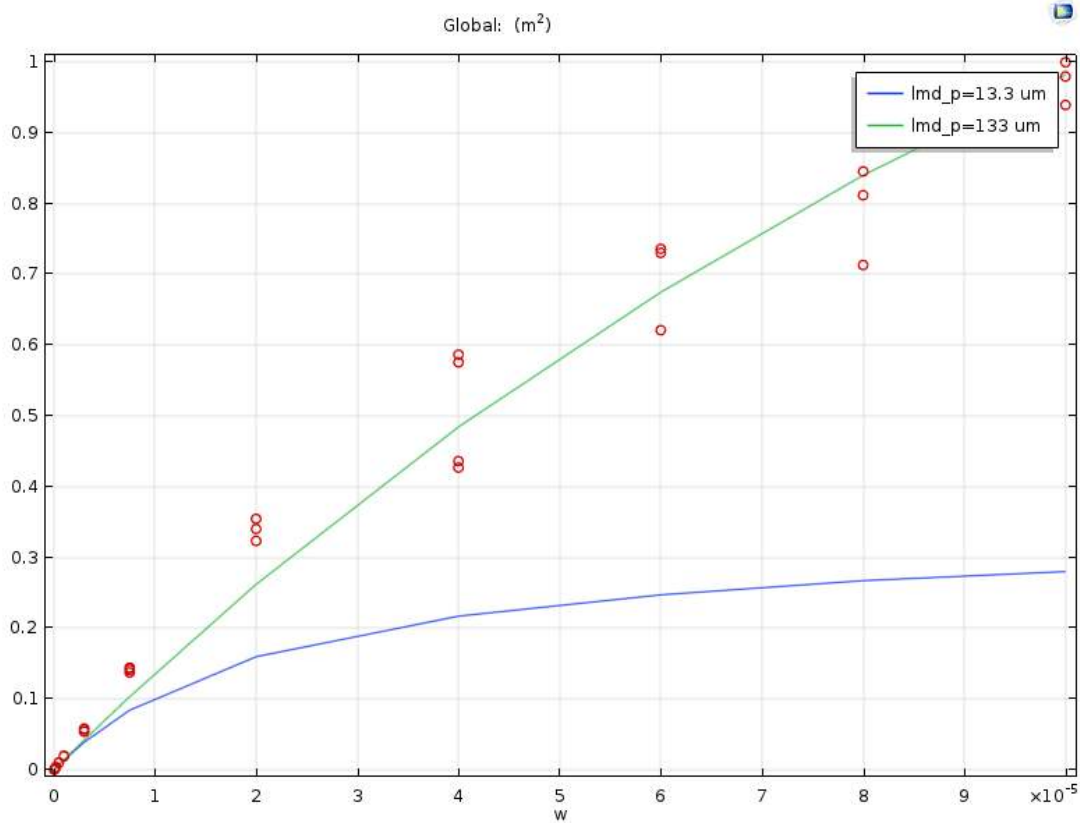


Ok so finding the intersection $x=4.124$. Again this is all Log scale so $10^x = 13.3\mu\text{m}$.

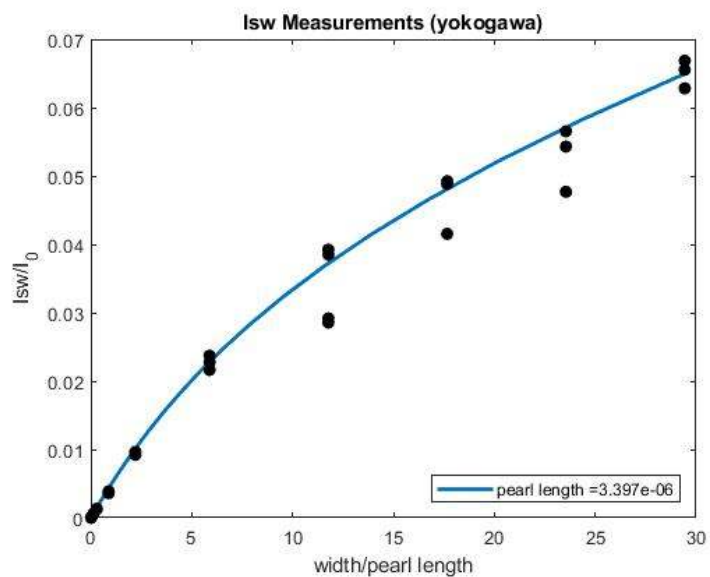
$$\Lambda = 2\lambda^2/d$$

$$\lambda = (\Lambda d/2)^{1/2} = 415.8\text{nm}$$

In COMSOL



Skoltech Model



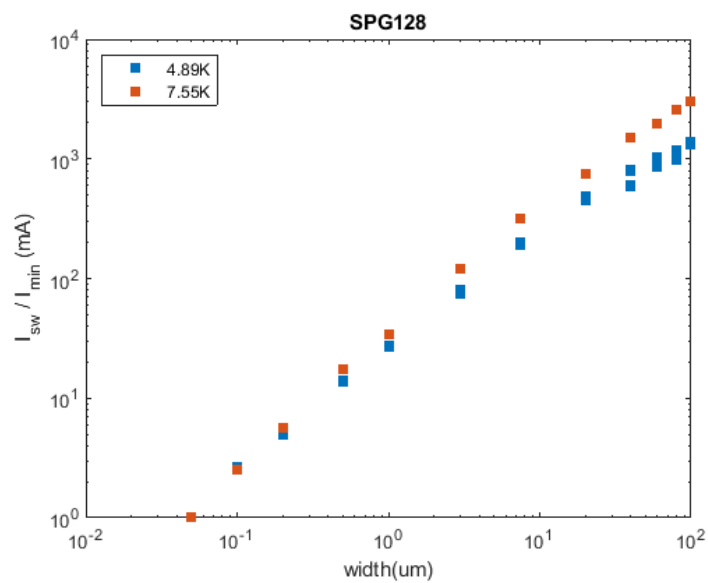
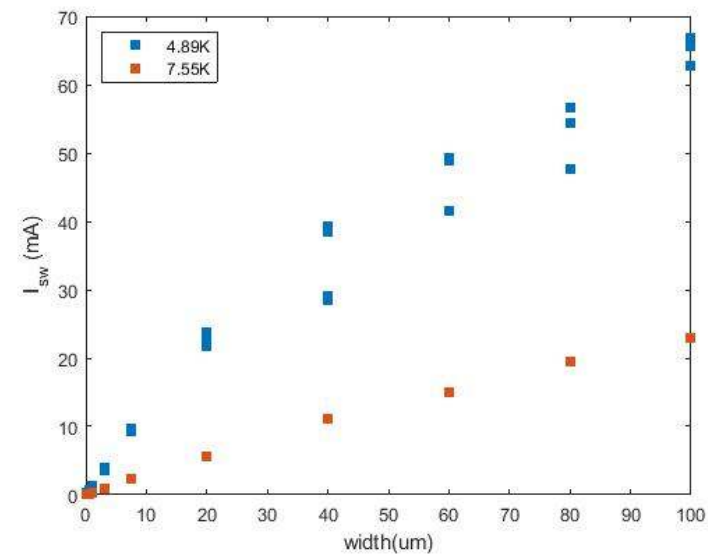
$$I_c/I_0 = x/(1+0.1952x+0.0255x^2)^{(1/4)}$$

$$x = w/\Lambda$$

$$\Lambda = 3.397\mu\text{m}$$

$$I_0 = 5.11\text{mA (fitting parameter)}$$

Temperature dependence



Wanted to include the temperature dependance of the penetration depth, also included dependance on bias current where I assumed $I = I_c$.

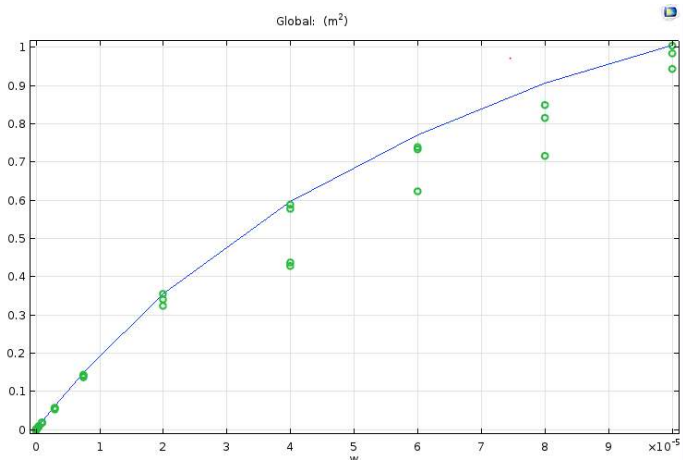
Only good fitting at $T \sim T_c$. where the measurement was taken at 4.89K.

Parameters

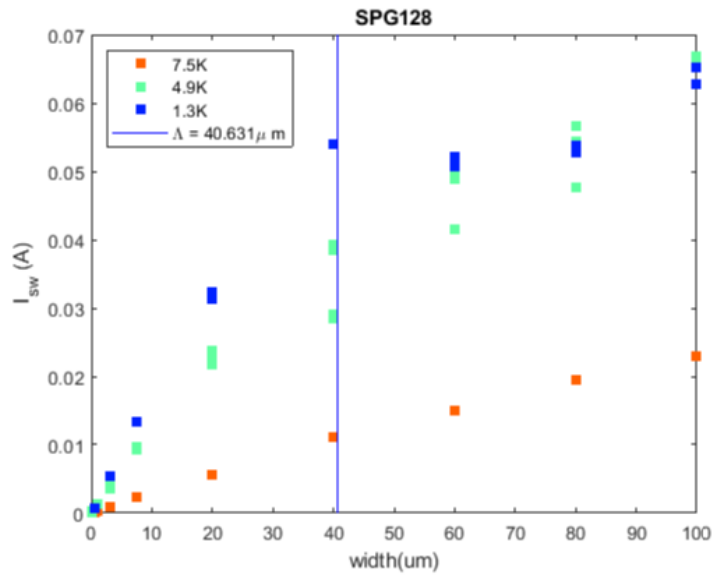
Name	Expression	Value	Description
x_box	500[um]	5E-4 m	
y_box	100[um]	1E-4 m	
w	500[nm]	5E-7 m	
t	26.04[nm]	2.604E-8 m	
T	8.89[K]	8.89 K	
Tc	9.77[K]	9.77 K	
lmd0	5.25097932415628e-07 [m]	5.251E-7 m	
lambda	sqrt(lmd_p*t)	5.885E-7 m	
lmd_p	13.3[um]	1.33E-5 m	
Lk	mu0_const*(lmdT^2)/t	6.4043E-11 H	
lmdT	sqrt((lmd0^2)*((1-(T/Tc)^2)^(-1))*((1+(T/Tc)^(3/2))^(-1/2))*((1-0.31)^(1-1/3)))	1.152E-6 m	

Name:

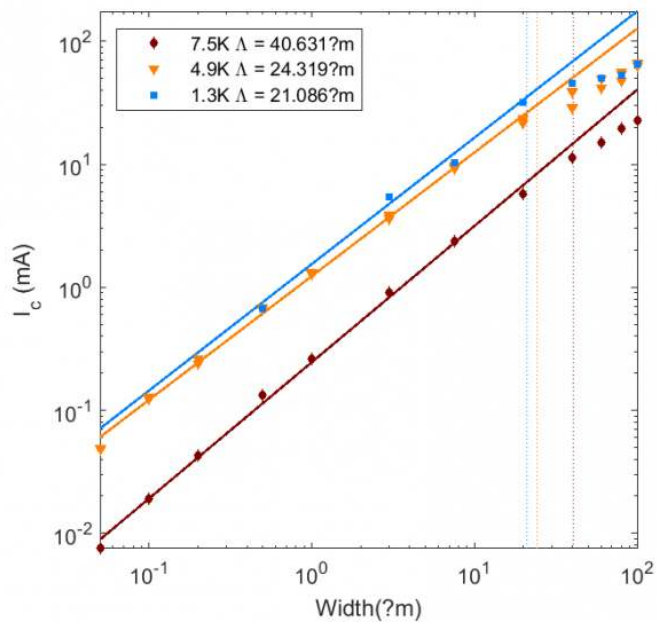
Expression:

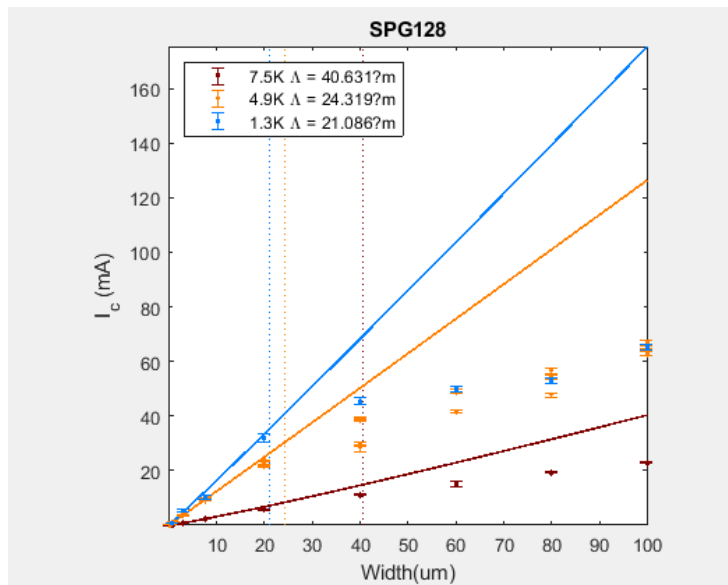


maybe i should focus on $T \rightarrow T_c$ model



Power fit for points less than calculated pearl length. Vertical dotted lines are calculated pearl length.





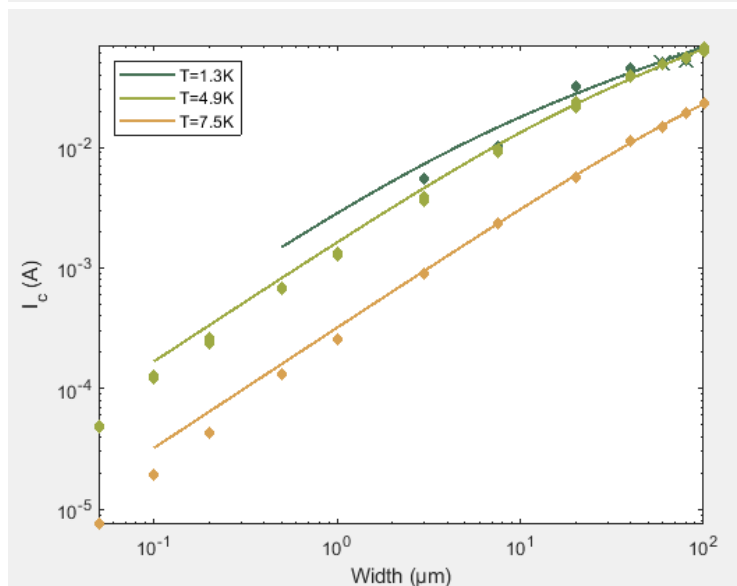
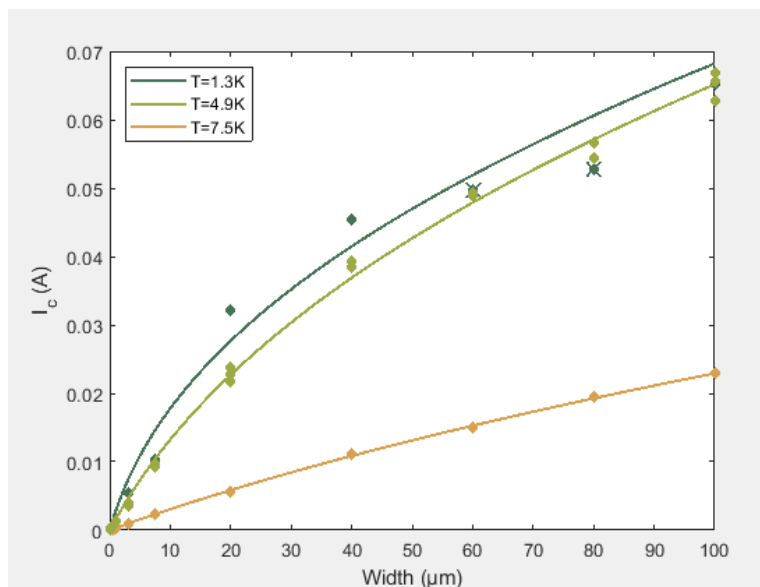
Skoltech Model

$$I(w) = \frac{dwj_c}{[1 + f(1)w/2\pi\Lambda_p + (\beta w/4\pi\Lambda_p)^2]^{1/4}}.$$

Skoltech Fit using following fitting parameters. X points were excluded.

beta(1.3,4.9,7.5K) = (.584,.596,.555)

f(1)((1.3,4.9,7.5K) = (.6925,.698,.6785)



Rsquare = (0.9792, 0.9980, 0.9996)

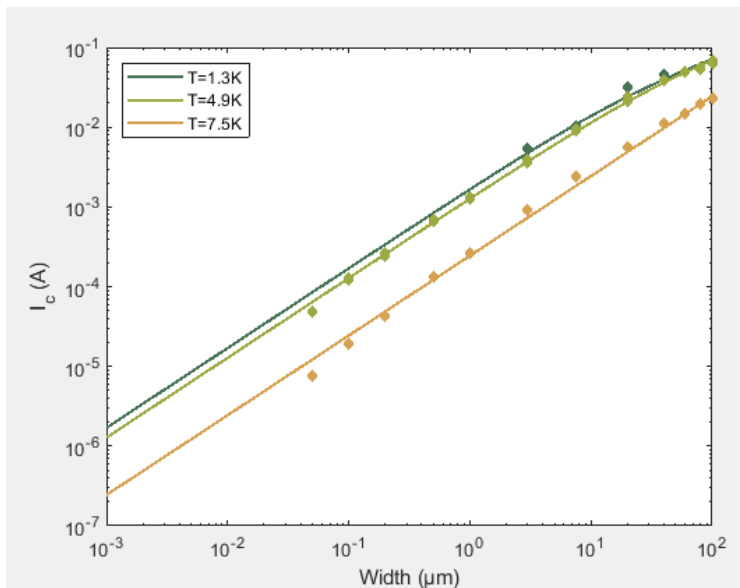
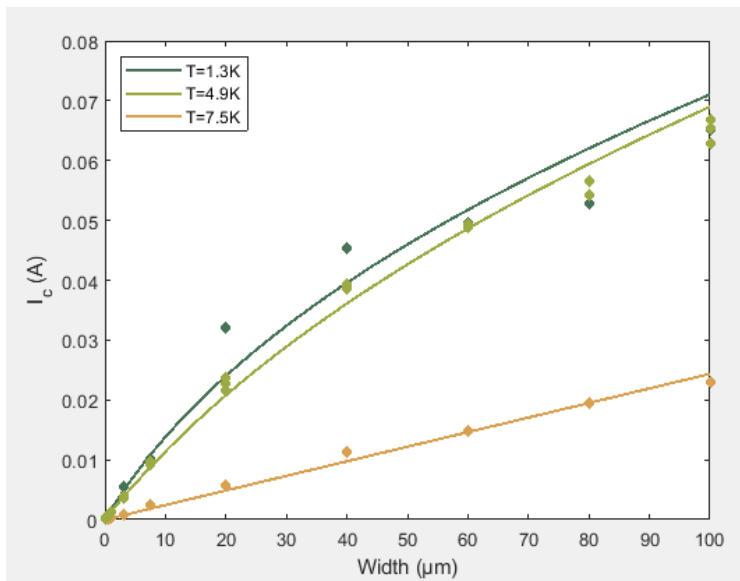
PearlLength (micron) = (0.2312 0.8648 5.1241) --- (not correct, far too small)

Jc (amps) = (0.1210 0.0645 0.0123)

Perhaps there is problem with weight of smaller currents. For $w < \text{Pearl Length}$ $I(w) = j_c \cdot d \cdot w$.

Fitting with $\log(\text{current})$

$\log_{10}(\text{current}) = \log_{10}\left(\frac{26.0E-3 \cdot x \cdot b}{1 + (0.6925 \cdot x)/(2 \cdot \pi \cdot a)} + \left(\frac{.584 \cdot x}{4 \cdot \pi \cdot a}\right)^2\right)^{1/4}$



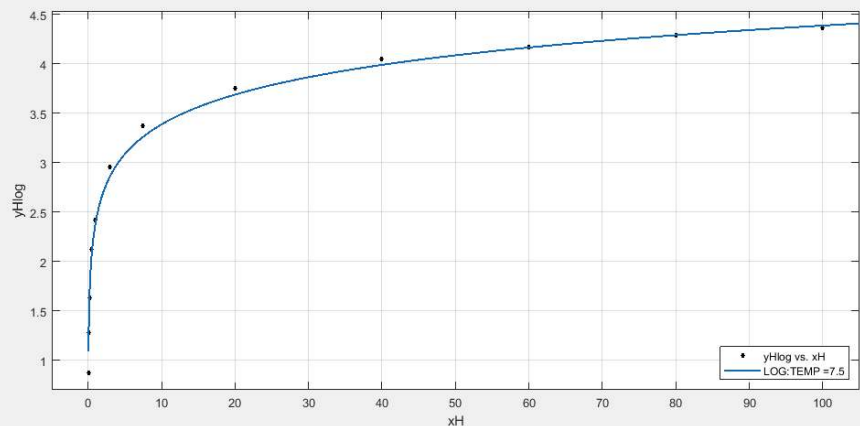
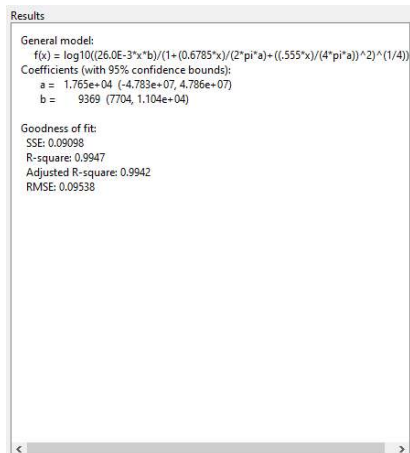
Slope at lower points is better.

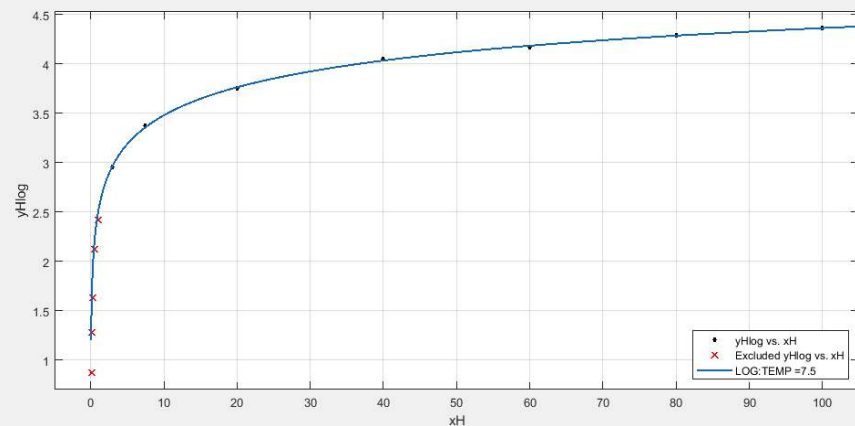
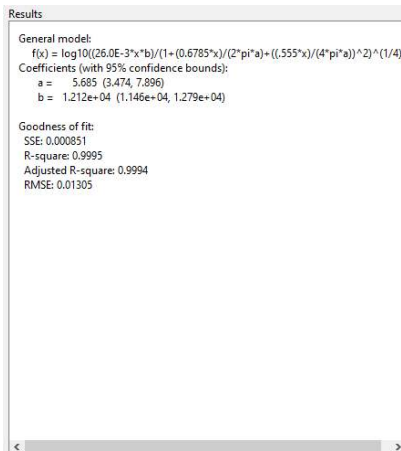
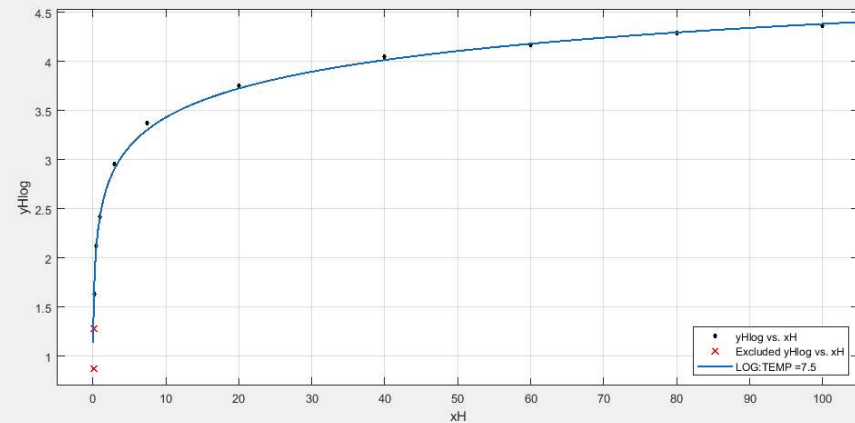
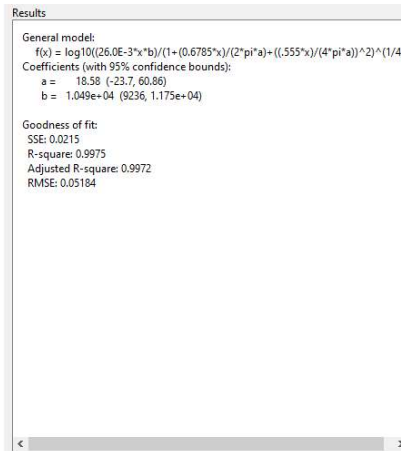
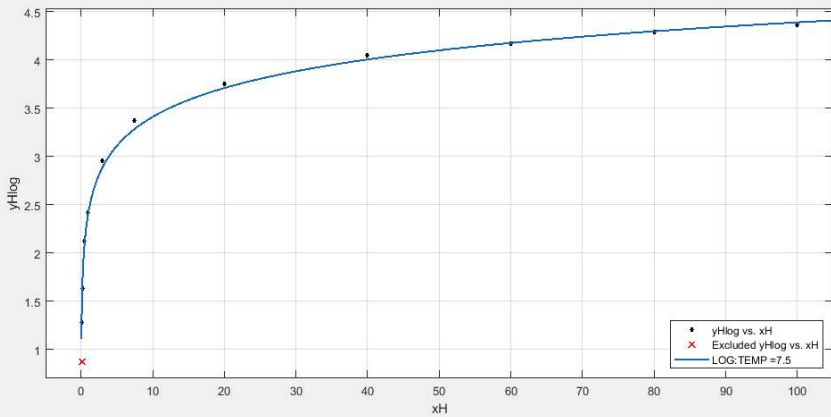
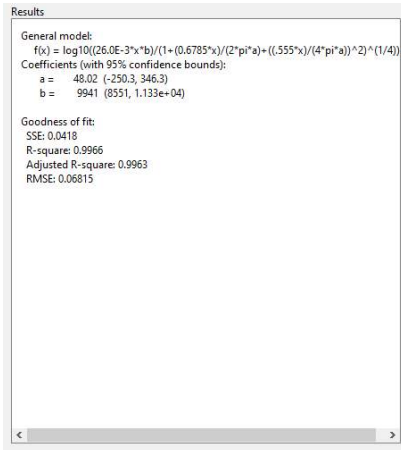
Pearl Length (um) = 1.0195, 2.0376, 17699 (last one does not converge well)

Instead of fitting J_c going to extract it from xdata less than 1um. $J_c = d \cdot w \cdot j_c$

@7.5K — $J_c = 9.7 \text{ mA}/\mu\text{m}^2$

@4.9K — $J_c = 51.2 \text{ mA}/\mu\text{m}^2$





Now the 95% bounds make more sense. Still, this is a sketchy fit method.

pearlLength = (um)

$(A/\text{um}^2) = 1e2 (MA/\text{cm}^2)$

$J_c = 1.0e+04 * (A/\text{um}^2)$ or **$*1e6 (MA/\text{cm}^2)$**

rquare =

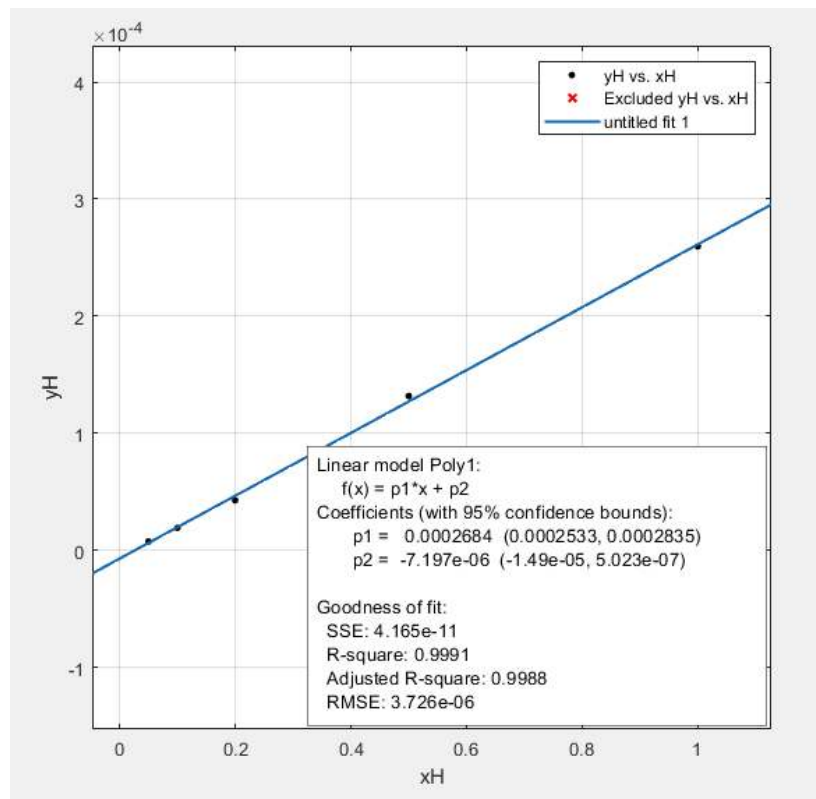
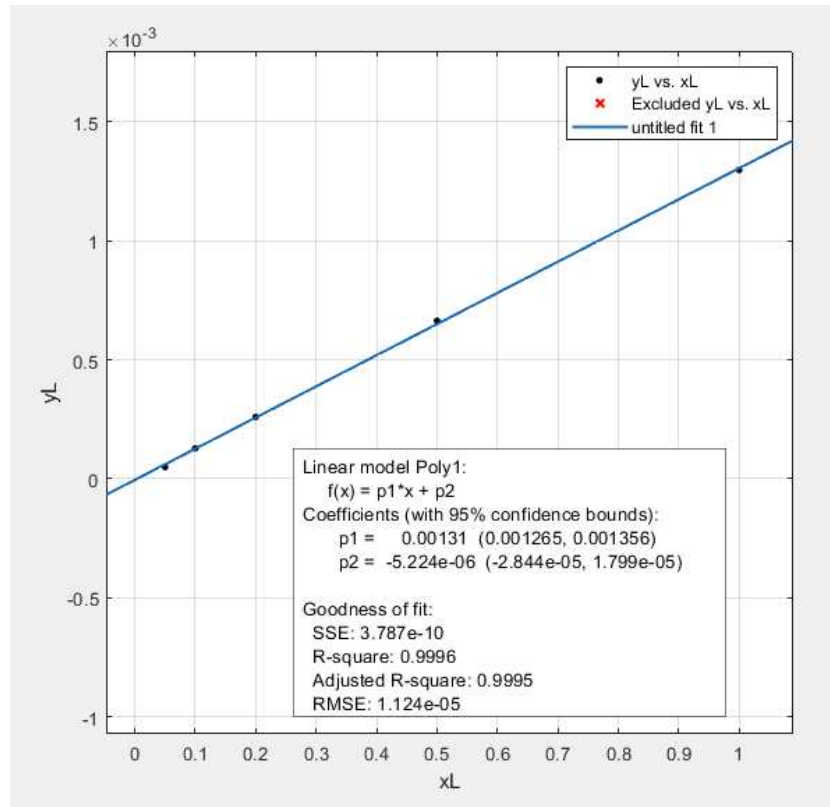
0.9881, 0.9986, 0.9995

J_c is typically $\sim 8 \text{ MA}/\text{cm}^2$

02/18/2020

x axis in micron

y axis in Amps



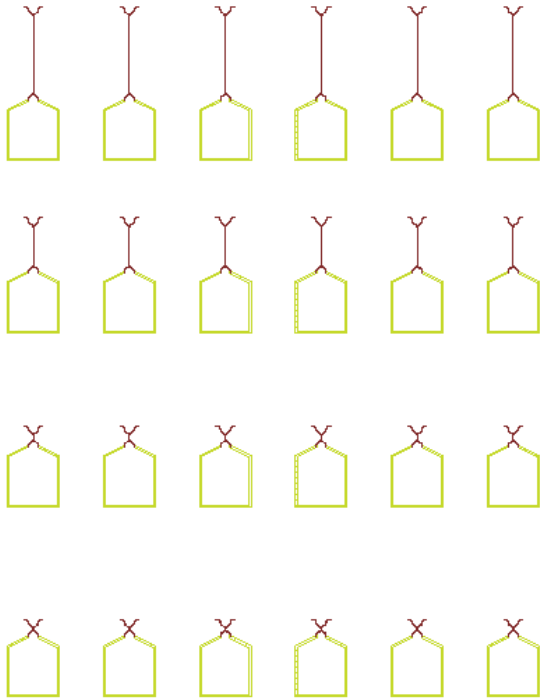
kinetic inductance measurements

October 3, 2019

Categories: Electronics, Fabrication, Materials, Superconductivity

Wires for kinetic inductance measurements.

Layout *



D

C

B

A1 2 3 4 5 6

SPG148 – 173.30hms/sq 13.84nm.

Bonded to middle 8 devices. Starting from top right moving in a U shape

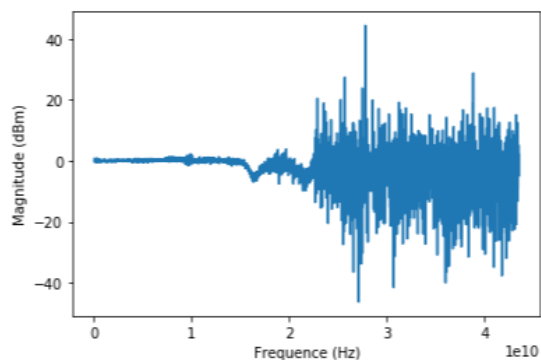
1. 388.7kOhm
2. 196.4kOhm
3. 24.00kOhm
4. 6.142kOhm
5. 9.92kOhm
6. 48.95kOhm
7. 426.6kOhm
8. 845.5kOhm

Free space ports: 5→8, 8→5

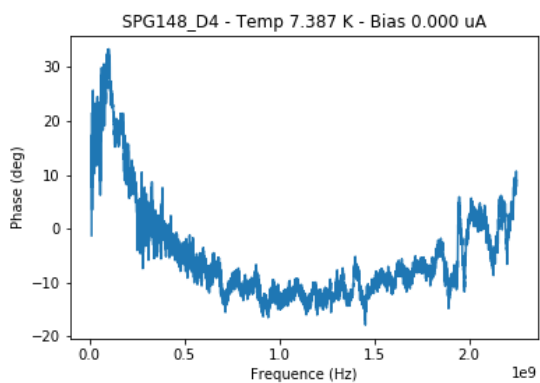
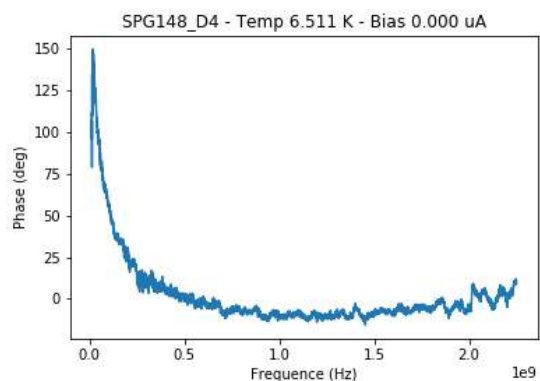
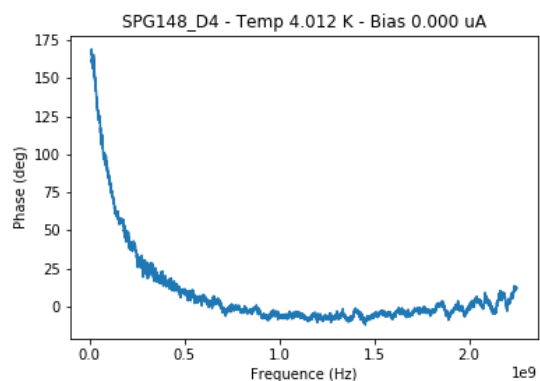
VNA

5uA → $\log_{10}((5e-6 * 50)^2 / 200 * 1000) * 10 \sim -65\text{dBm}$ considering loss in cable... -50

Calibration with -50 dBm // 5001points // IF bandwidth – 10kHz //



Swept temperature with no bias. Very little/no change from 4K-6.5K. Switched around 7.3K.

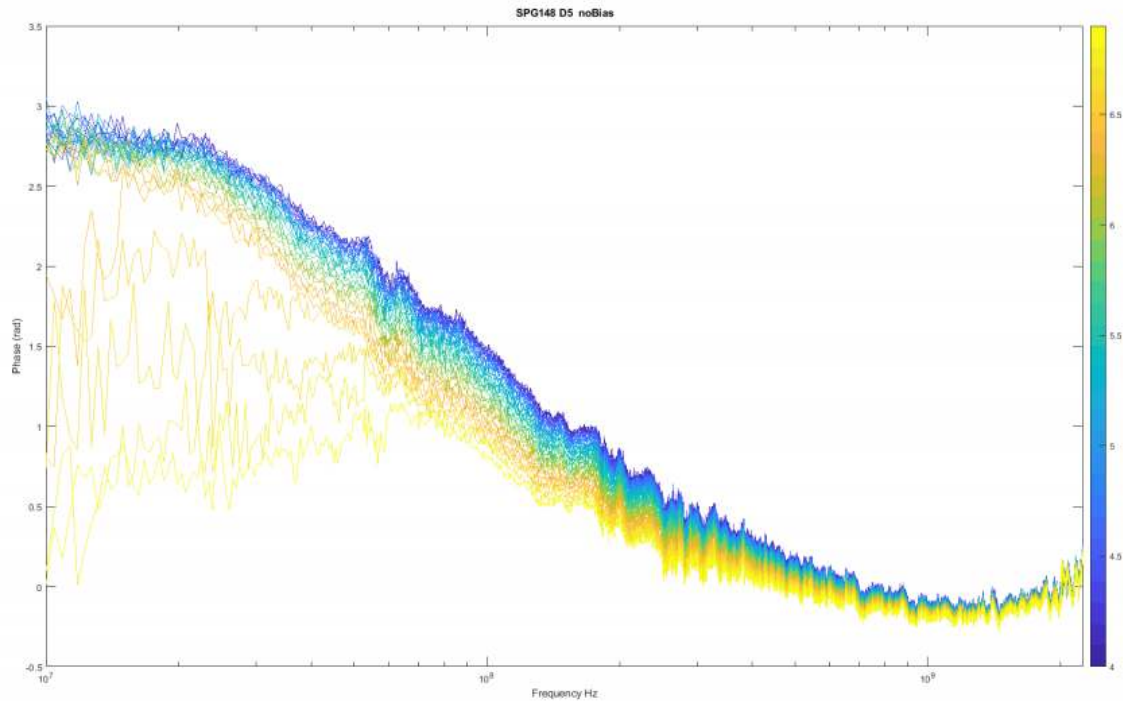


With Bias

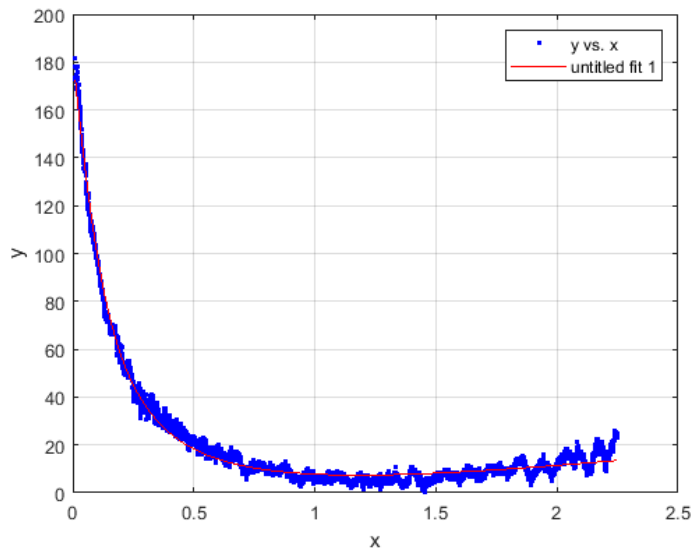
D5 @ 3.8K Isw = 7.1uA

D5 @ 6K Isw = 1.5uA

Temp Dependence



fit at 4K



result =

General model:

$$\text{result}(x) = a \cdot x + c \cdot (180/\pi) \cdot \text{atan2}((100 \cdot 2 \cdot \pi \cdot x \cdot L), (((2 \cdot \pi \cdot x \cdot L)^2 - 50^2))) + b$$

Coefficients (with 95% confidence bounds):

$L = 59.59$ (58.91, 60.28)

$a = 12.25$ (11.98, 12.52)

$b = -21.69$ (-22.22, -21.16)

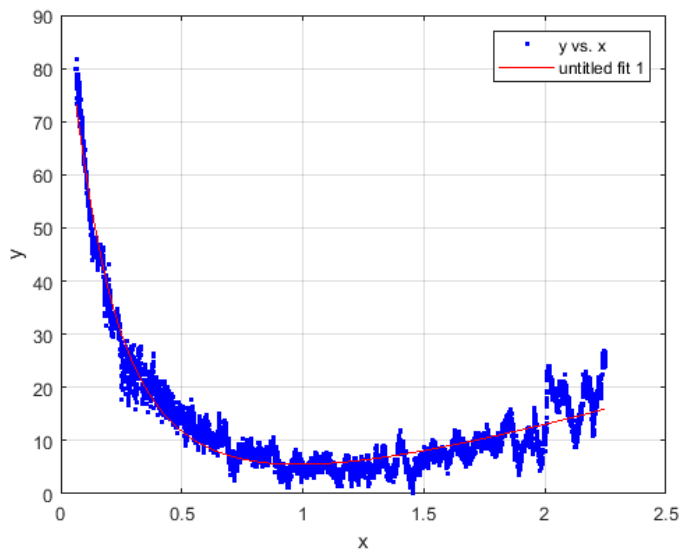
$c = 1.133$ (1.129, 1.138)

gof =

struct with fields:

sse: 4.832899424904734e+04
 rsquare: 0.988132146173623
 dfe: 4997
 adjrsquare: 0.988125021186335
 rmse: 3.109919904257344

fit at 7K



result =

General model:

$$\text{result}(x) = a \cdot x + c \cdot \left(\frac{180}{\pi} \right) \cdot \text{atan2} \left((100 \cdot 2 \cdot \pi \cdot x \cdot L), (((2 \cdot \pi \cdot x \cdot L)^2 - 50^2)) \right) + b$$

Coefficients (with 95% confidence bounds):

$L = 41.21$ (40.04, 42.38)

$a = 14.79$ (14.44, 15.14)

$b = -23.87$ (-24.64, -23.1)

$c = 0.6687$ (0.6621, 0.6752)

gof =

struct with fields:

sse: 4.556623100048192e+04

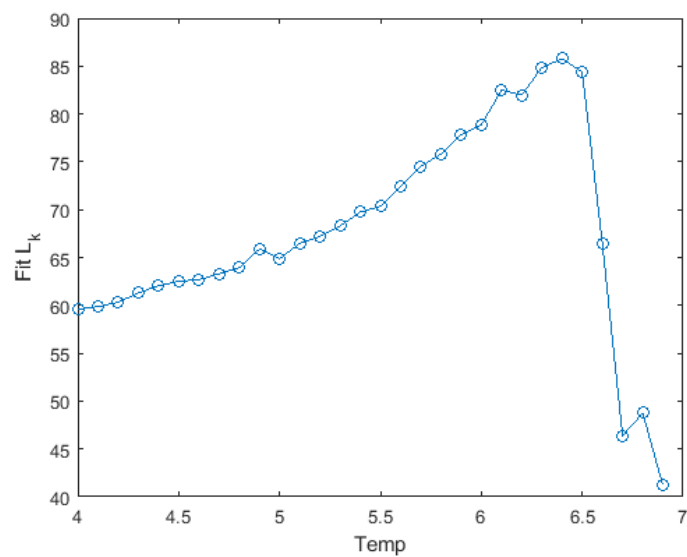
rsquare: 0.940411580054567

dfe: 4878

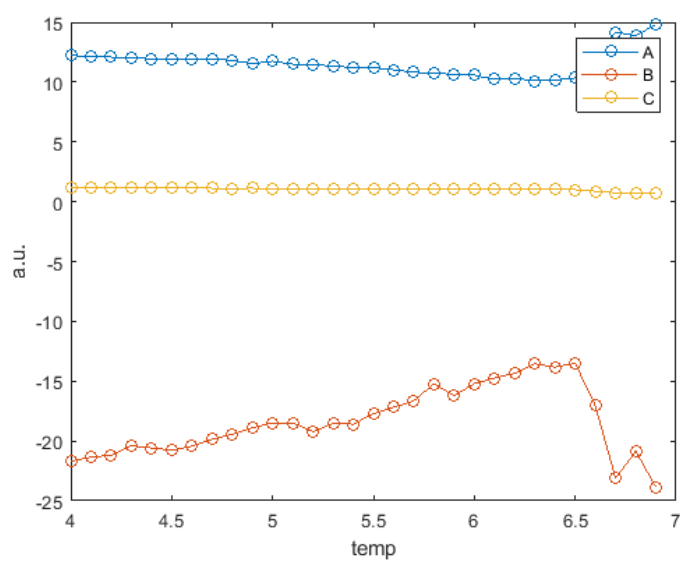
adjrsquare: 0.940374932809828

rmse: 3.056332895285862

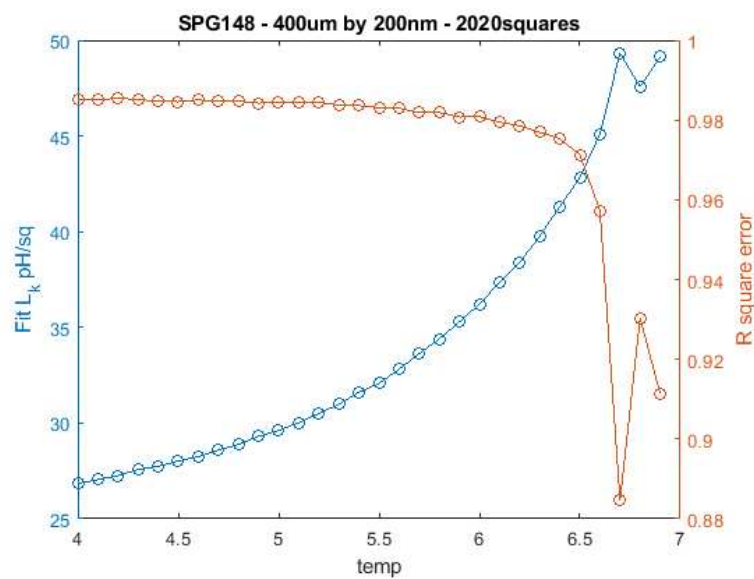
Across Temperature gradient

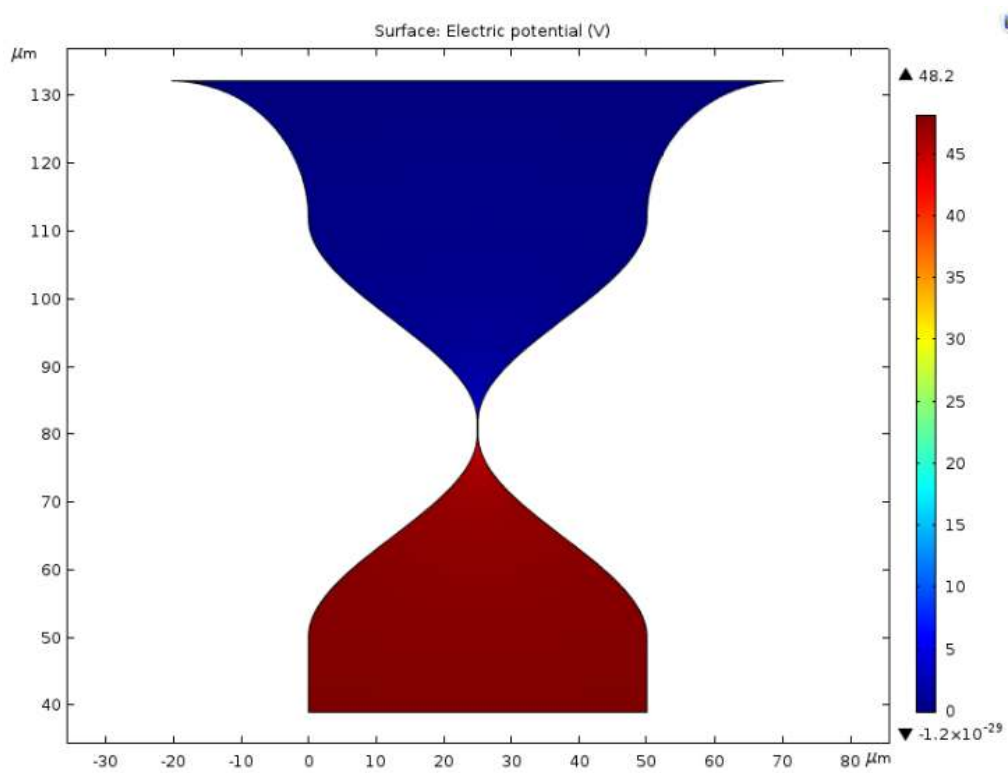
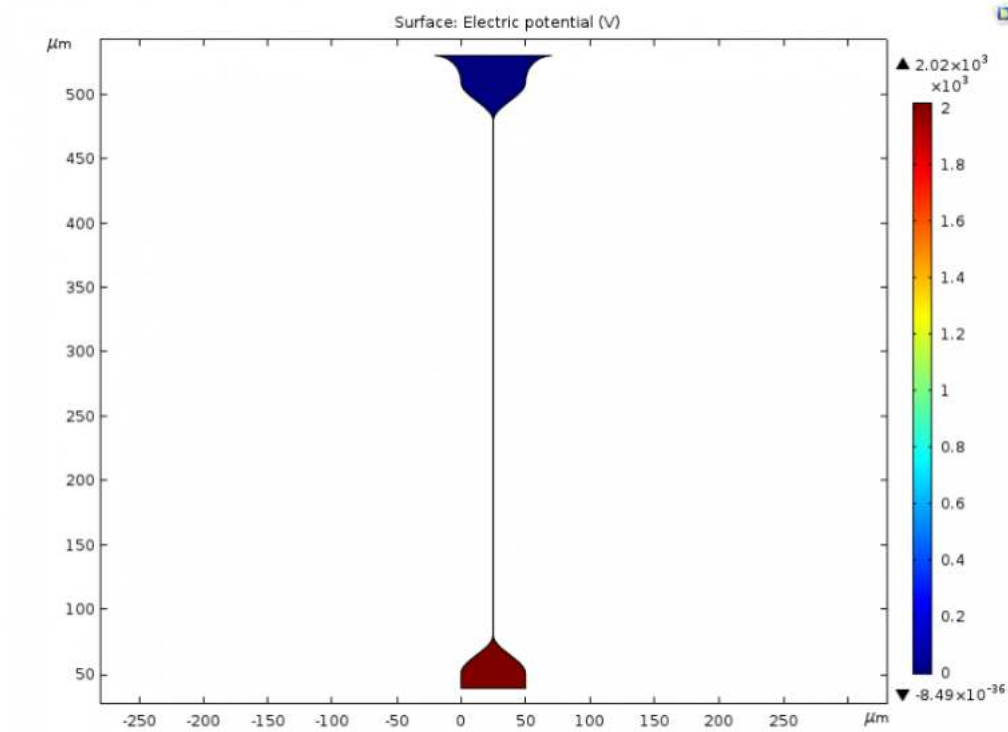


fitting parameters

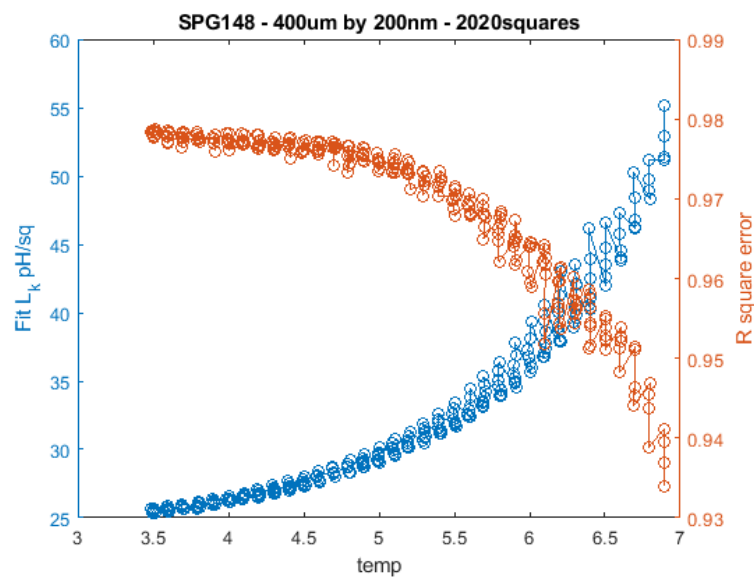


Took averages of A and C. Left B as a fitting parameter. With the fixed A, C showed in the plot below.

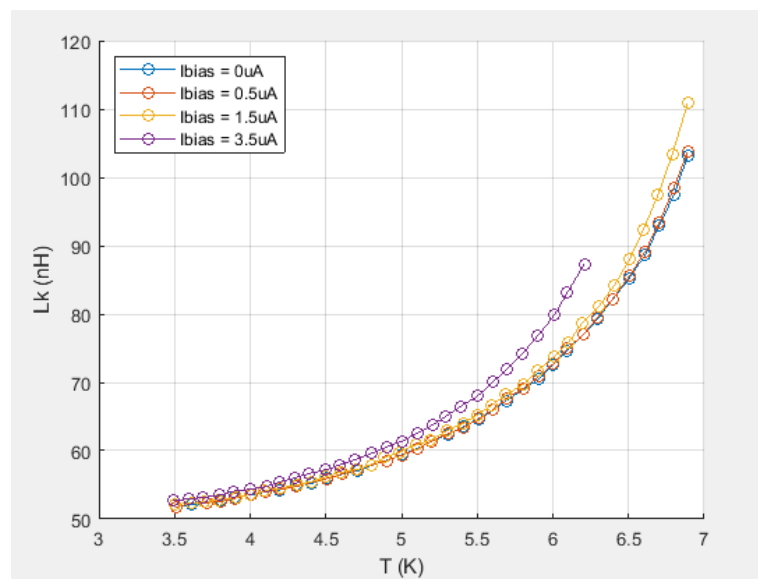




next -65dBm — 5001 points — 300Hz IF bandwidth —



Extracting curves as a function of bias. Very little change



SPG148_D5_lowNoiseSweeps.zip

Probe station temperature control

October 7, 2019

Categories: nTron

Quick post describing a measurement method for higher temperature measurements in the probe station.

Follow the normal procedure to cool down to $\sim 4.8\text{K}$ wait until the radiation shield reaches a minimum, around 27K .

The helium flow on the medium pressure pump is typically 70L/min . Decrease the flow by half, the temperature should remain $\sim 4.8\text{K}$. At this point turn on the heater for the sample stage. We set a set point of 7K and medium power. The PID control kept the temperature at 7.55K .

This method takes quite a bit of time and drastically shortens the amount of time available for measurement, due to the helium consumed. For temperature based measurements this should be a final option.

He Transfer Notes

October 16, 2019

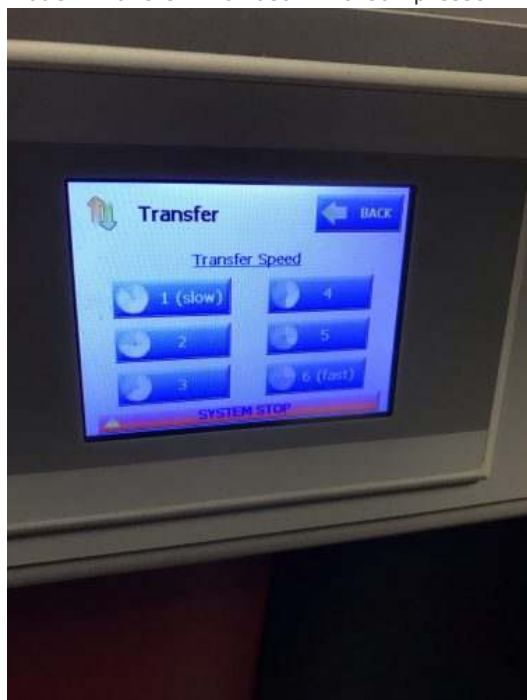
Categories: nTron

Notes on transferring helium into the dewar.

1. Disconnect liquefier (similar to probe station)
2. Connect Dewar to probe station reclaim line.
3. Insert long end of transfer line using silver coupler into the liquefier . Insertion should be moderately slow. Make sure to perform with ample ceiling clearance.
4. Gas will begin to exit short end of transfer line, wait until gas flow creates audible frequency shift (very noticeable a few seconds after first audible recognition, helicopter like) before inserting short end into dewar.
5. Pressure on liquefier should approach ~6psi (<10psi). Wait for pressure to decrease below 3psi.



- 6.
7. Mode->Transfer-> 6 Fast-> No Compressor



- 8.
9. Frosting is typical



10.



11.

12. Monitor transfer volume. Dewar max 100L usually target 70-80L. There is usually a large drop from inaccurate measuring.



13.

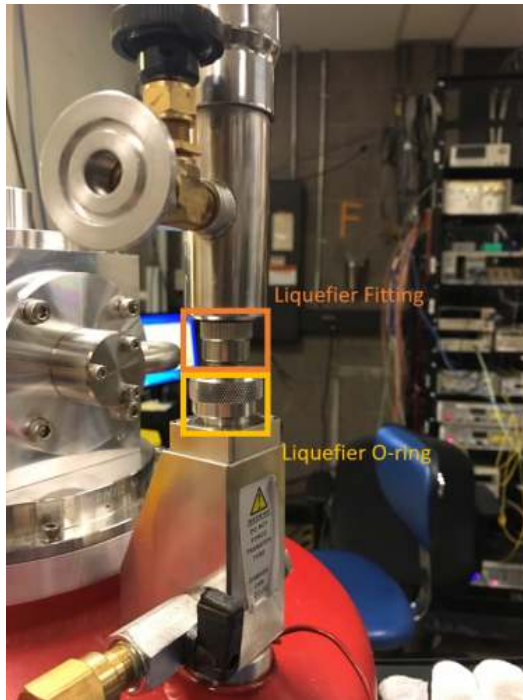
14. From the bottom of the initial drop we targeted ~ 50 L.



- 15.
16. To exit this menu. Select the red/yellow triangle in the bottom left.

Exit

1. Mode -> Stop
2. Removal is more difficult. Liquefier is more critical. Both ends of transfer line must be removed at the same time.
3. CRYO GLOVES ON
4. Loosen the liquefier fitting and begin lifting the transfer line. After 1 ft out loosen the liquefier o-ring and hold the fitting down in the liquefier while you continue to remove transfer line.



- 5.
6. Once the majority of the line is out ~3.5ft be prepared to remove fitting with line.
7. It is better to remove fitting earlier, with <1ft of line still in the liquifier.
8. If the fitting comes out early, the smaller diameter of the transfer line will come out easily. If the fitting stays in the liquifier with the transfer line removed, the ball valve will remain open. Losing lots of helium and potentially freezing the fitting in the liquifier. remember. **Losing helium is bad. But it is not nearly as bad as the burns that can result from helium gas or handling supercooled metal.**

Liquid Helium Dip Probe F-35

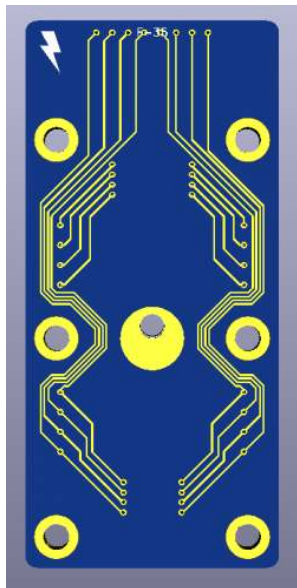
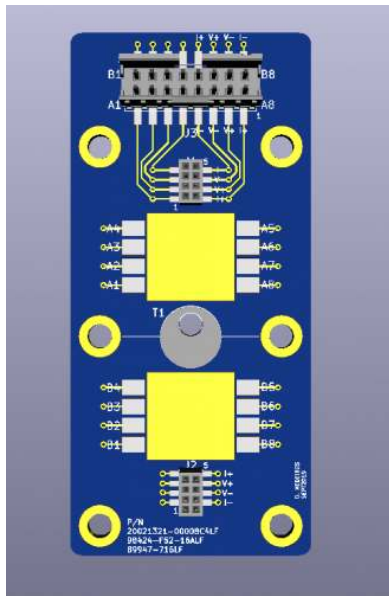
October 24, 2019

Categories: nTron

This post contains all the documentation for the F-35 dip probe.

Main Features

- Two 1x1cm sample positions
- Temperature sensor
- 2 Four point measurements
- 16 conductors total. One (or more) will have to be designated as ground



Some minor details were corrupted and removed from this save. For second version, silk screen would need updating.

[pogoBoard.zip](#) [topPogoBoard.zip](#)

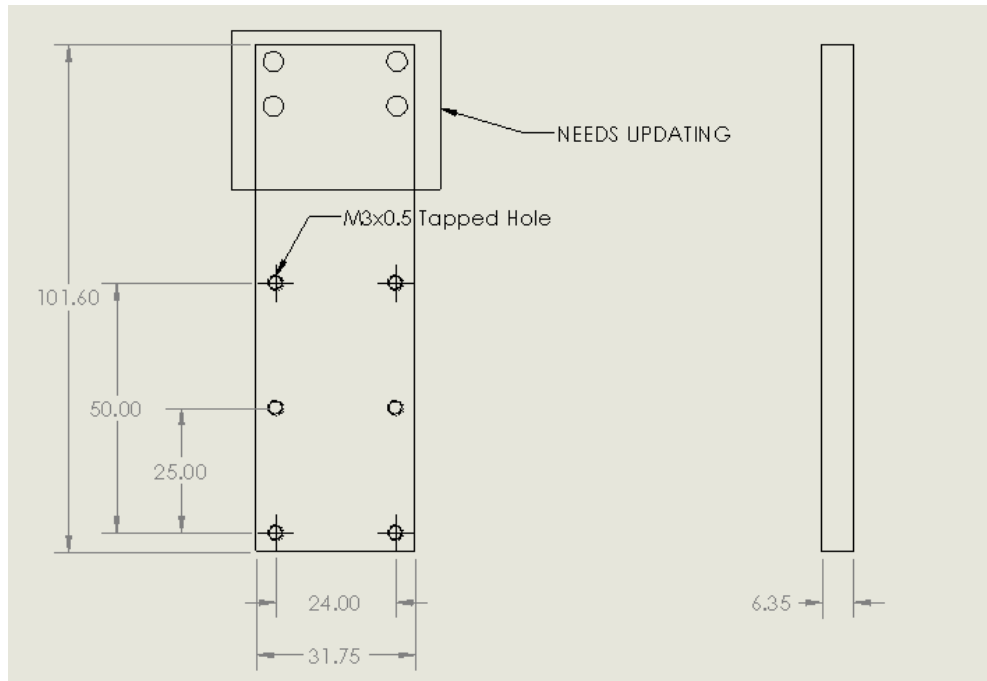
Component List

Digikey Order – [60998061.xlsx](#)

McMaster – Low profile socket head M3 – 90666A105, 90666A103

Assembly

MECH



As of 10/24/2019. The mount is left over from the first construction of the Tc dip probe. When a new mount is built it should be longer. I am currently not sure of the threads at the top.

Hex standoffs were machined down to match clearance between boards.

Front = top

PINOUT – FTACIR19AC

The due to a few design/assembly errors the silk screen does not accurately reflect the pinout. Please reference this list. The top sample is connected to the front of the source meter in the script >>def setup4WR() set TERM:FRON. The rear panel is connected to the bottom sample TERM:REAR.

Connector – Board

- A – B8 – (I+)
- B – A8 – (I+)
- C – B7 – (V+)
- D – A7 – (V+)
- E – B6 – (V-)
- F – A6 – (V-)
- G – B5 – (I-)
- H – A5 – (I-)
- J – B4
- K – A4
- L – B3
- M – A3
- N – B2
- P – A2
- R – B1
- S – A1

T – NC

U – NC

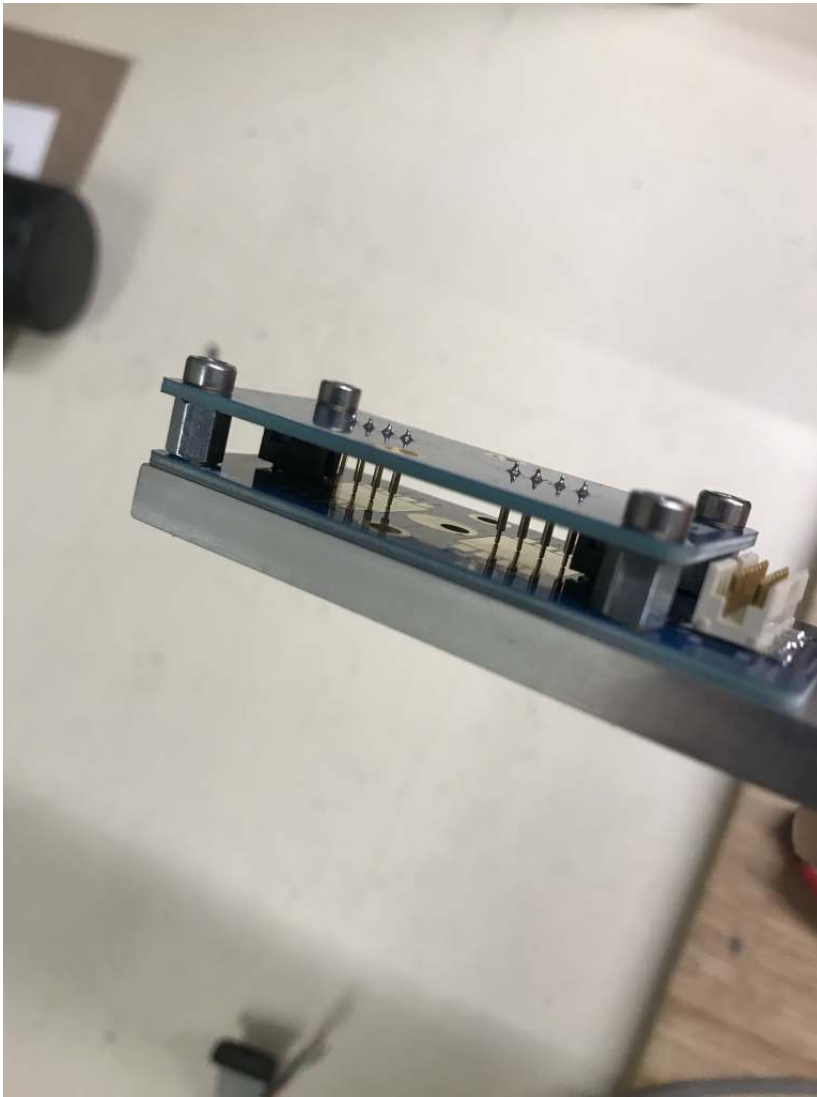
V – NC

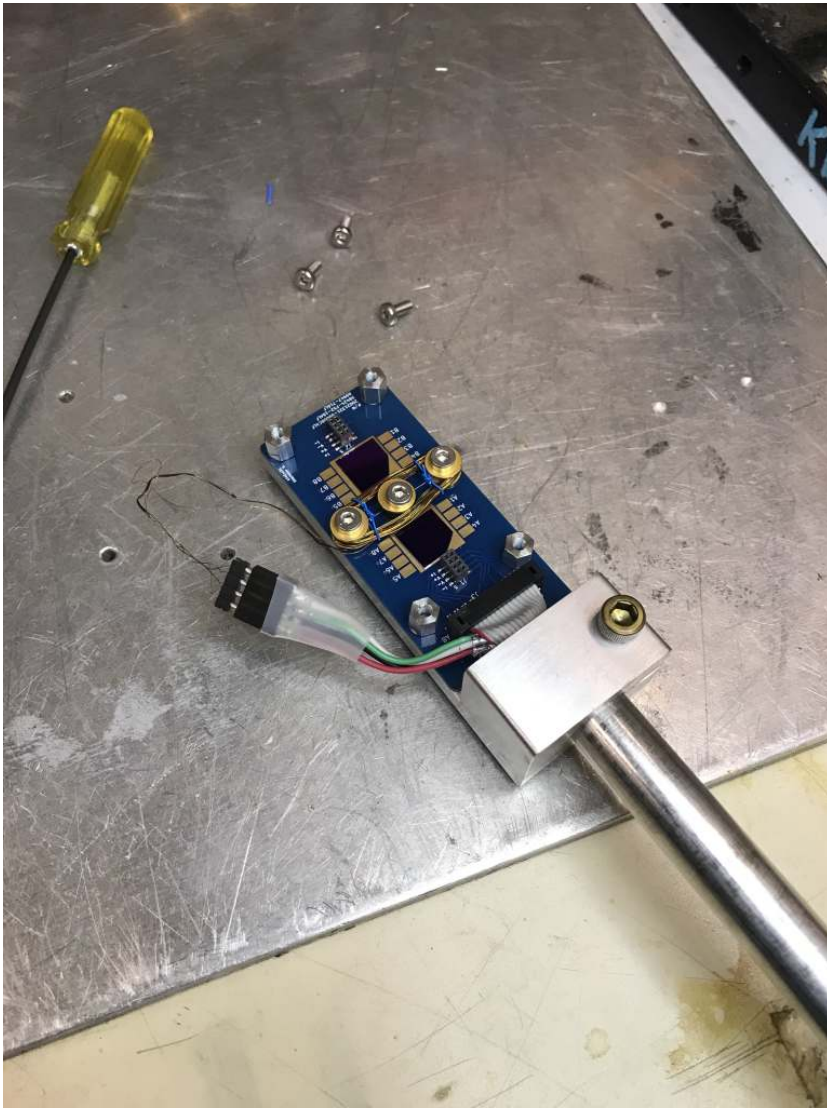
Standard Operating Procedure

No grease! Pogo pins are only source of sample mounting, have not experienced a sample falling out. If you are concerned about losing your chip, use foil on outside.

No scratches!





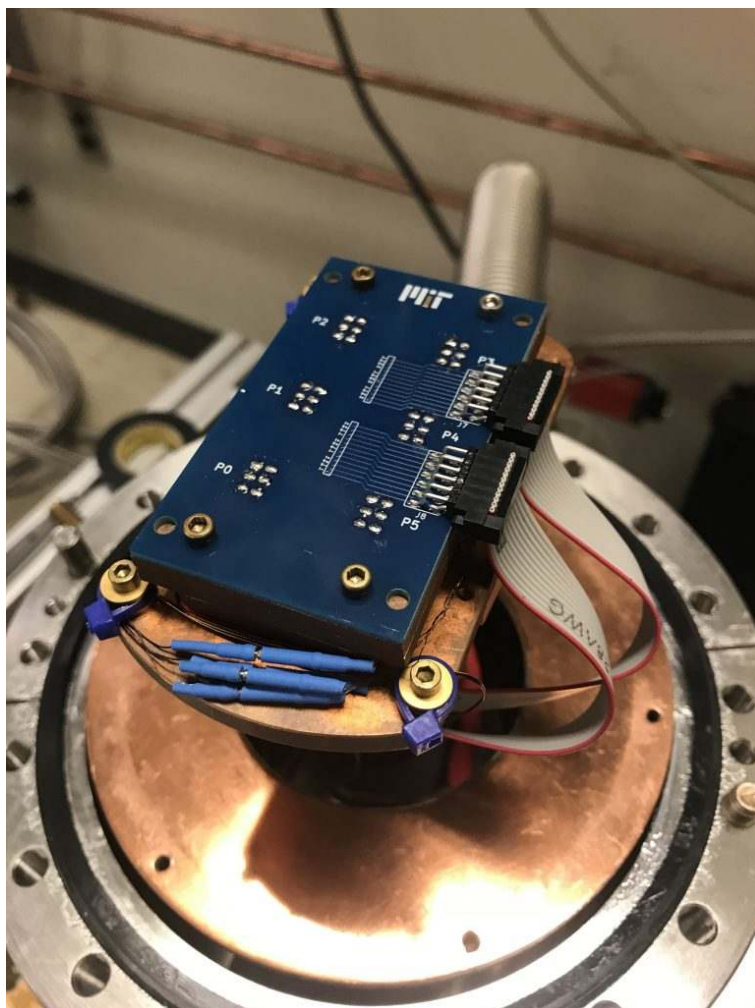
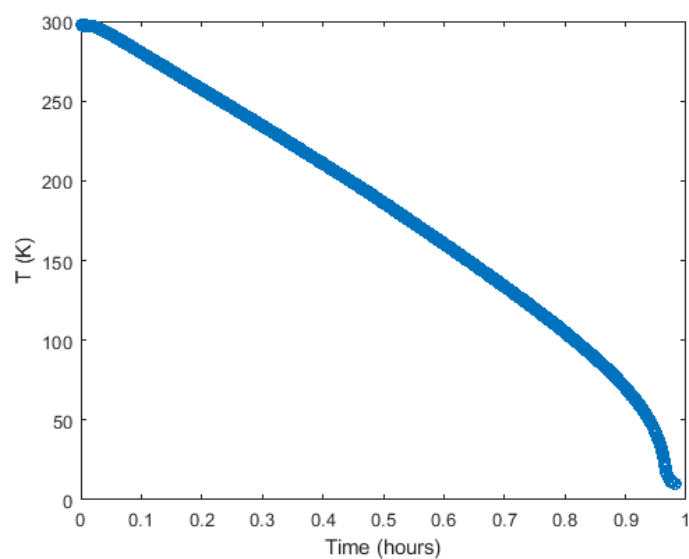


Tc Cryo – New cold head from vikas + pcb F-117

December 4, 2019

Categories: Cryostat

Cooldown to 10K



Pinout

A	Temp:RED	X	I+
B	Temp:GREEN	Y	V+
C	Temp:BLACK	Z	V-
D	Temp:CLEAR	a	I-
E	I+	b	I+
F	0 V+	c	V+
G	V-	d	V-
H	I-	e	I-
J	I+	f	Heater +
K	V+	g	Heater -
L	V-	h	NC
M	I-		
N	I+		
P	V+		
R	V-		
S	I-		
T	I+		
U	V+		
V	V-		
W	I-		

kinetic inductance measurements 2

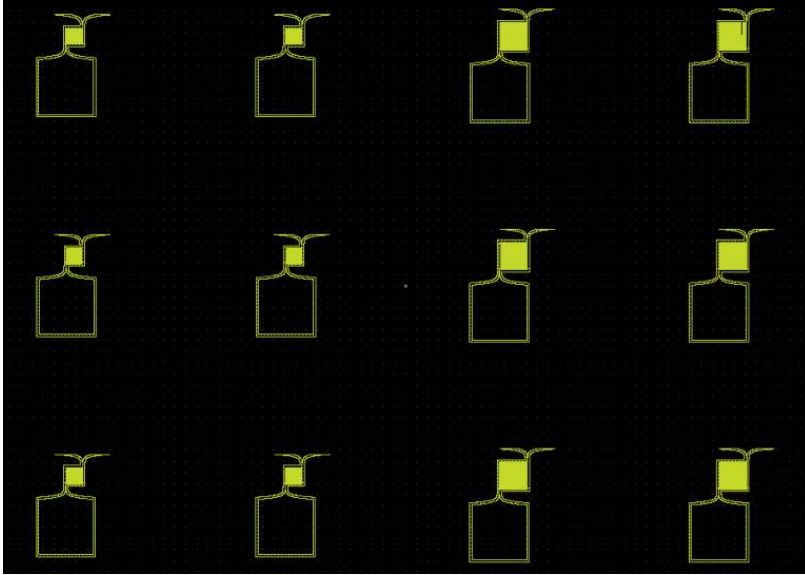
January 20, 2020

Categories: Kinetic inductance

Last post: <https://qnn.mit.edu/wordpress/archives/20912>

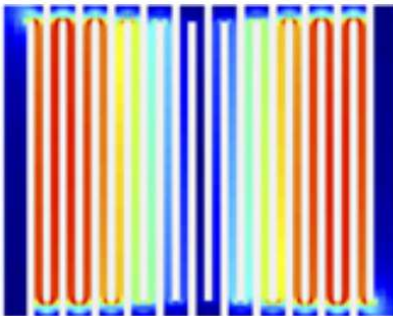
SPG193 – 7

wireWidth=nm, wireArea = um, pitch = 4um



Ic Testing in Free Space at 3.4K. The switching current was 2X the previous set of devices. 750nm – 125um had a **Isw = 14.7uA** with no RF bias, with **-65dB** had a **Isw = 14.3uA**. Little change in phase, not a good inductor. Same number of squares as the last measurement. Could the meander be an issue. does not make sense as most of the inductance should be kinetic and not geometric.

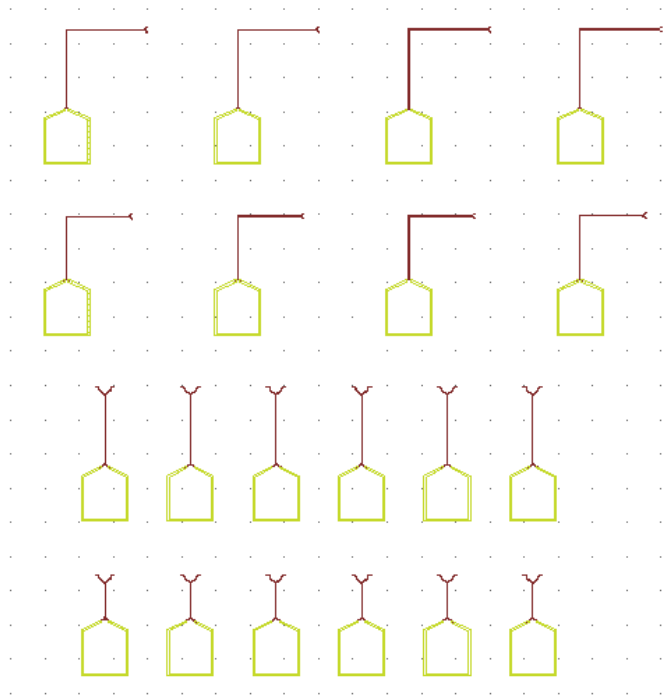
From: Annunziata, A. J., Santavicca, D. F., Frunzio, L., Catelani, G., Rooks, M. J., Frydman, A., & Prober, D. E. (2010). Tunable superconducting nanoinductors. *Nanotechnology*, 21(44), 445202.



Color is current density. Perhaps the effective length of the wire is much shorter.

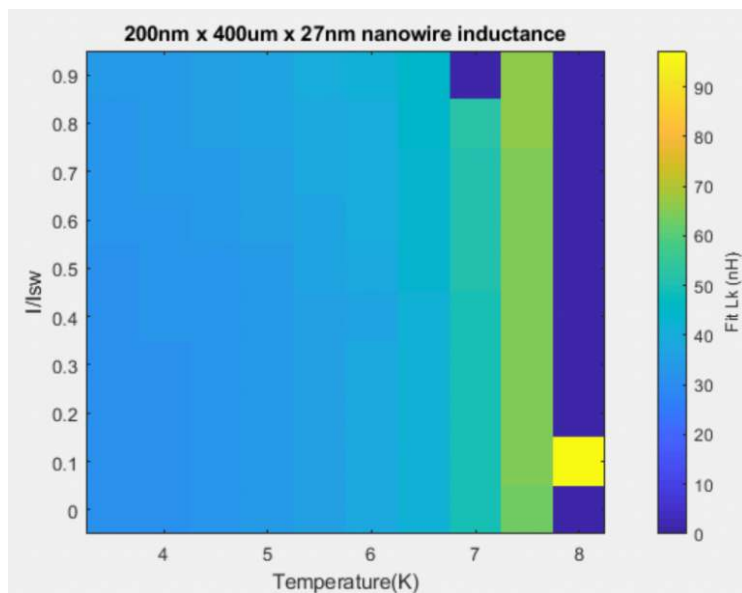
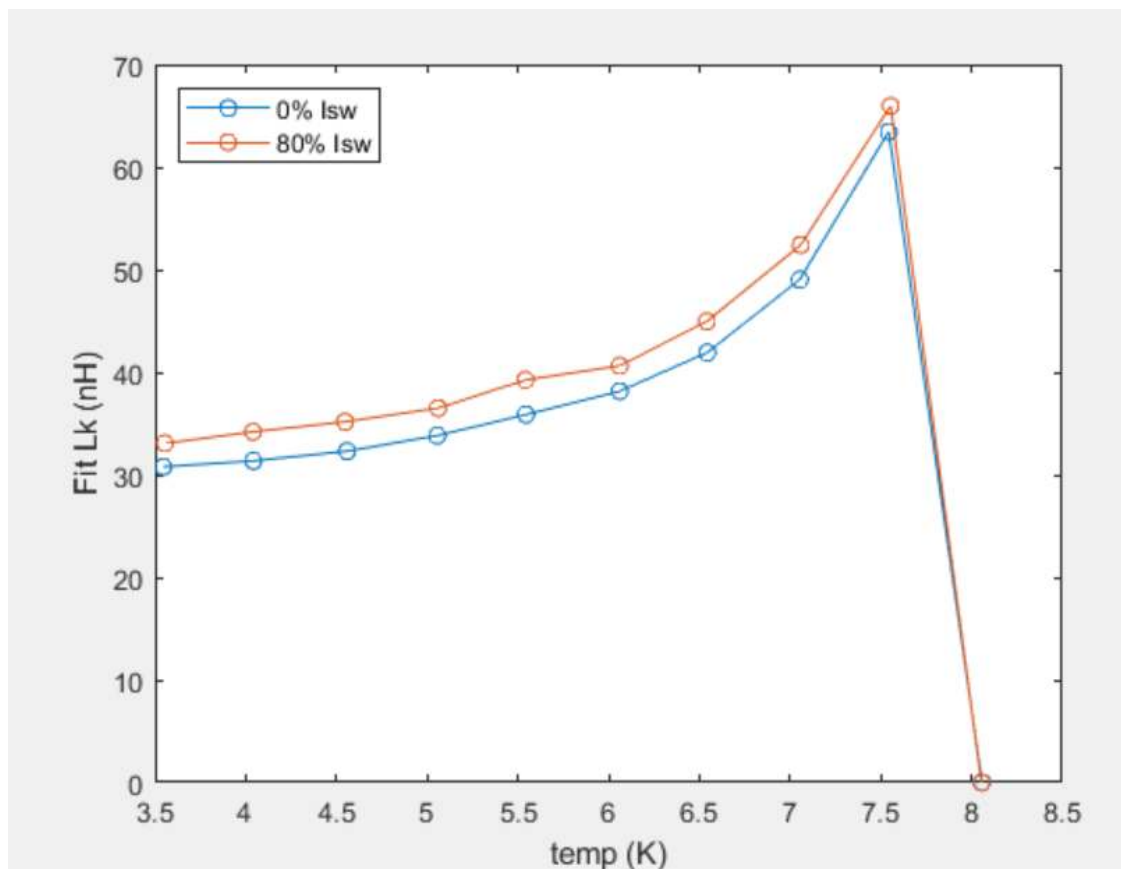
New thicker device. SPG200 – 27nm

Bend devices are 800um or 1000um long and have widths left to right of 400nm, 600nm, 800nm, 1um. The straight devices are the same design as the first round of measurement. They are 100nm, 200nm, 400nm, wide with lengths of 200um and 400um.

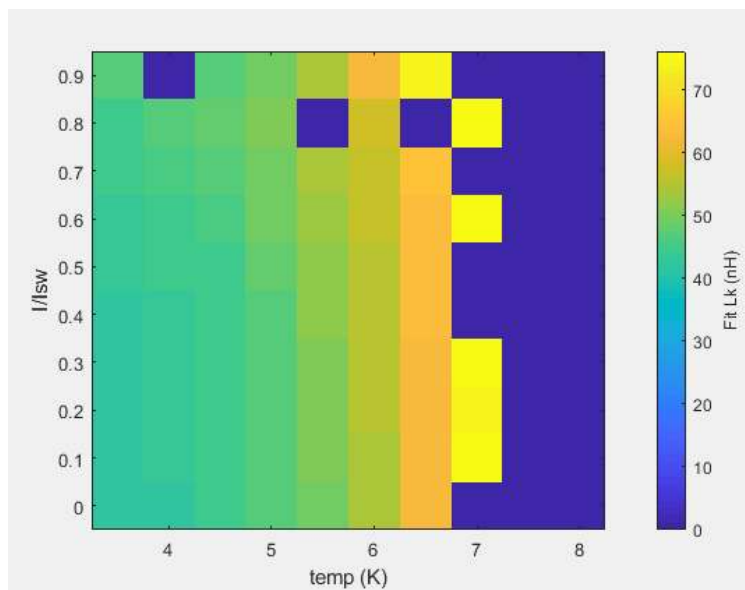


Initial findings

Fabricating on a thicker film would allow us to have a greater range of DC bias before switching, meaning the RF bias would be a smaller percentage of the switching current. For a 200nm X 400um device the switching current at 3.5K was:
 $I_{sw}(\text{no bias}) = 25.39 \text{ uA}$, $I_{sw}(-60\text{dBm}) = 24.19 \text{ uA}$.



similar results for other devices. Below is a 100nmX400um



kineticInductance_BB_AED_3_SPG200.zip

Wide Wire NbN Detectors

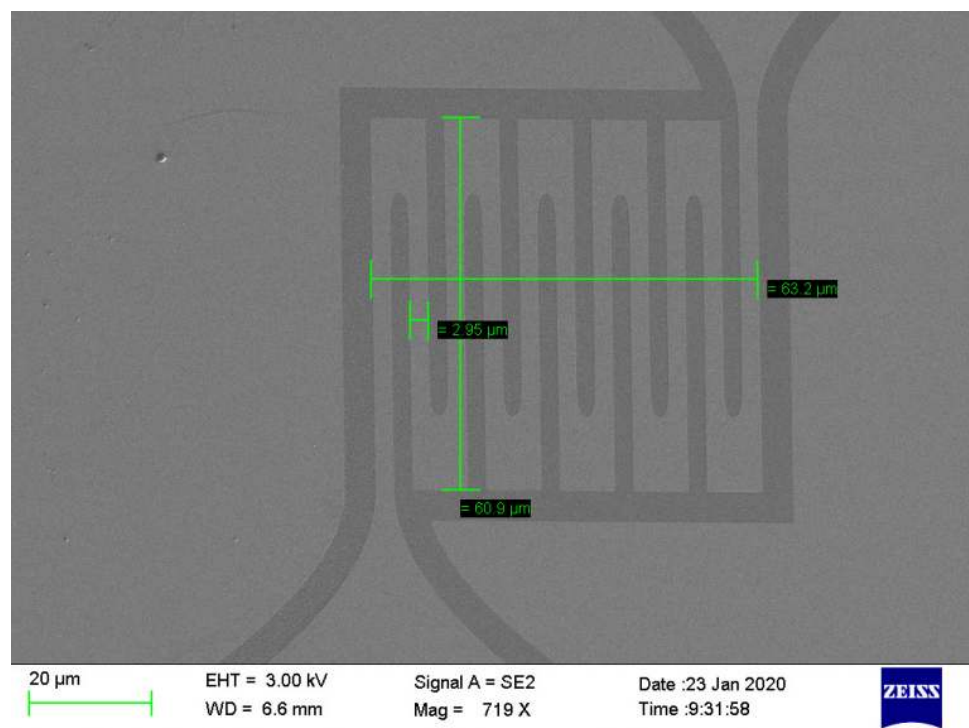
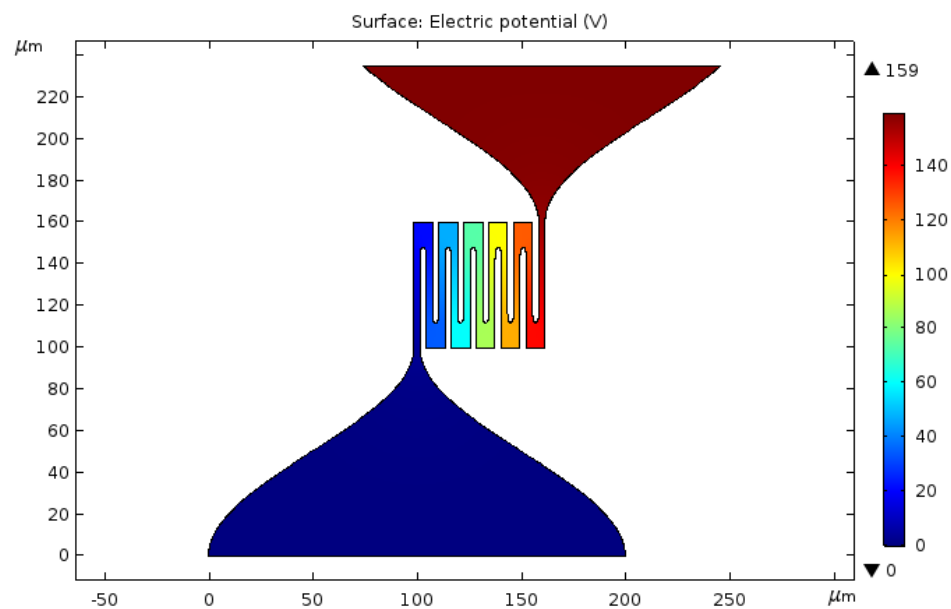
February 3, 2020

Categories: SNSPD

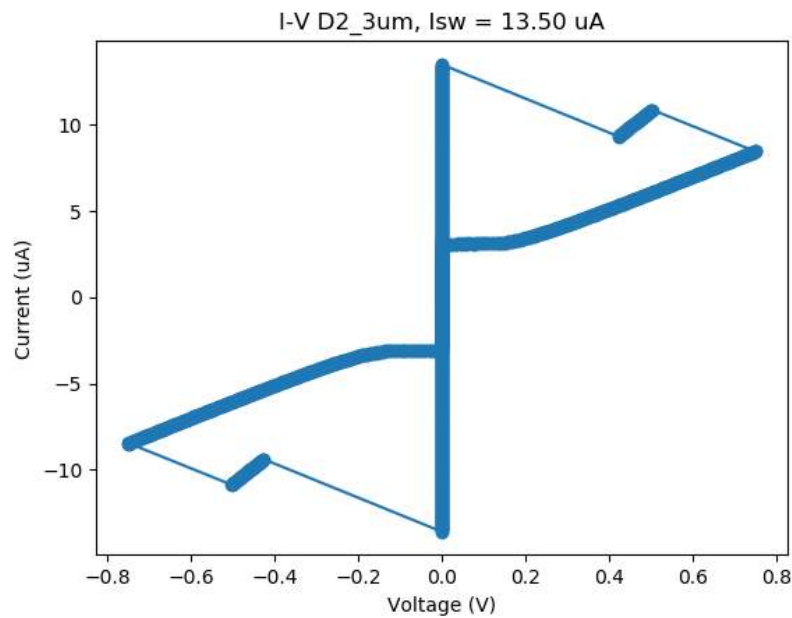
SPG202 – 2.7nm

DetWidth=
size=

Device 2 – 3um

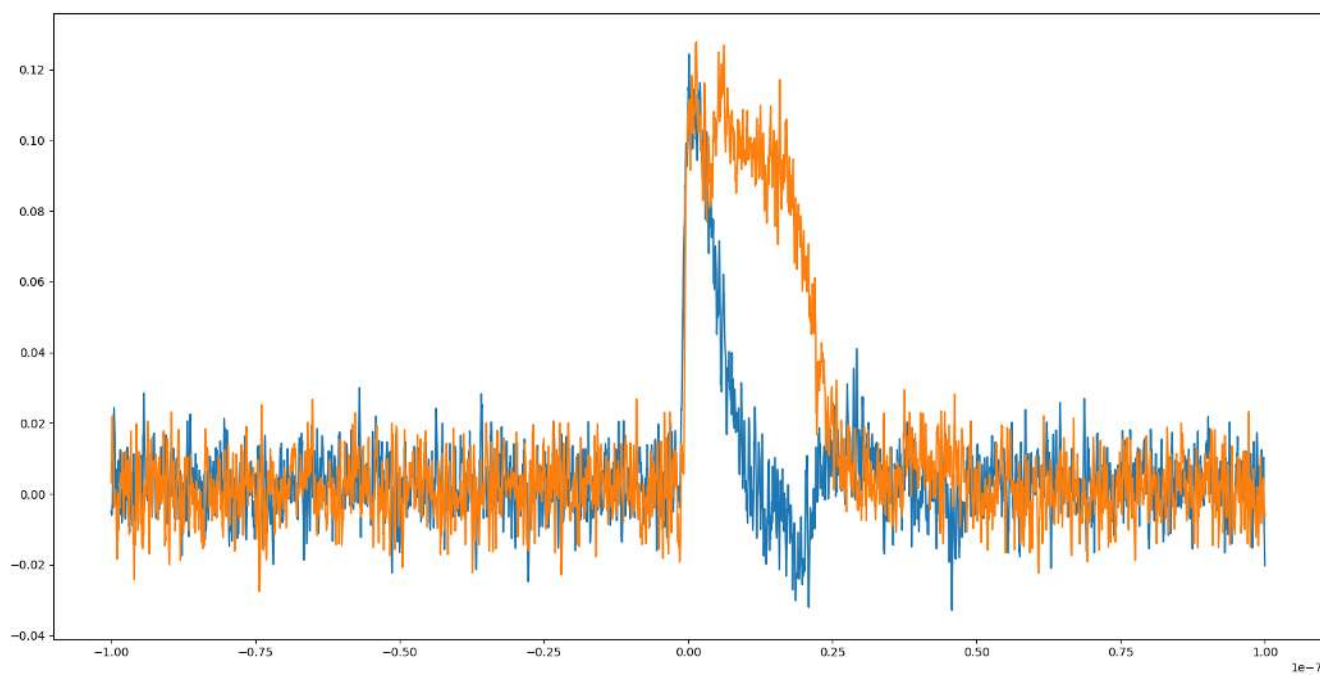


SMA-BiasT-3dB-2500-3dB-2000



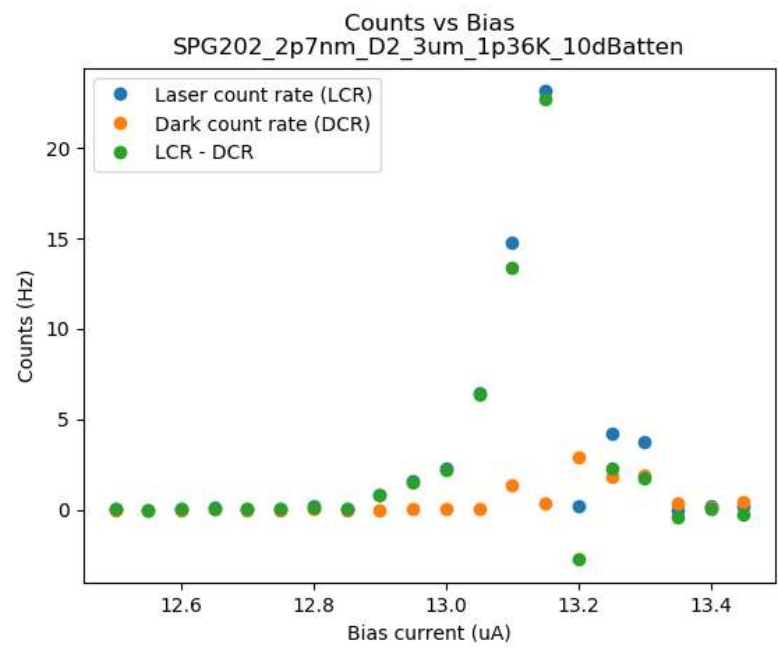
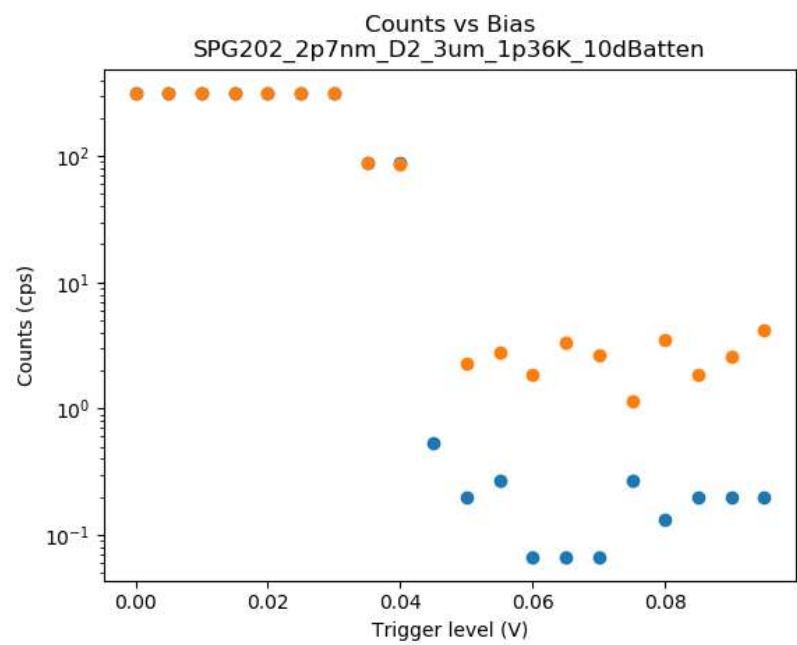
On scope. Dark counts at a bias of 13.1uA up to switching at 13.45. 80mV trigger

Latching behavior

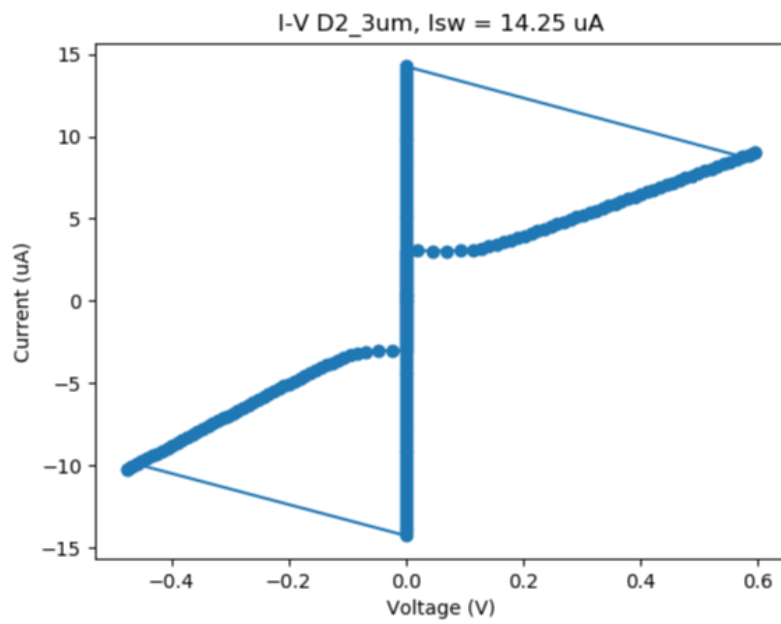


Having problems with counter injecting a lot of noise into the detector. Decided to set AUX out of scope as 1V on trigger. Then port the AUX to the counter so the remaining code can stay the same.

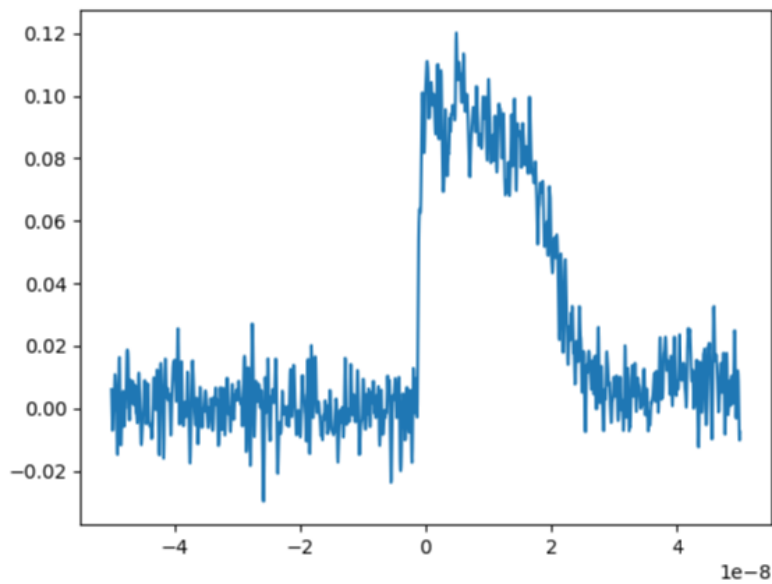
Trigger sweep with and without illumination (1550nm, -10dB)

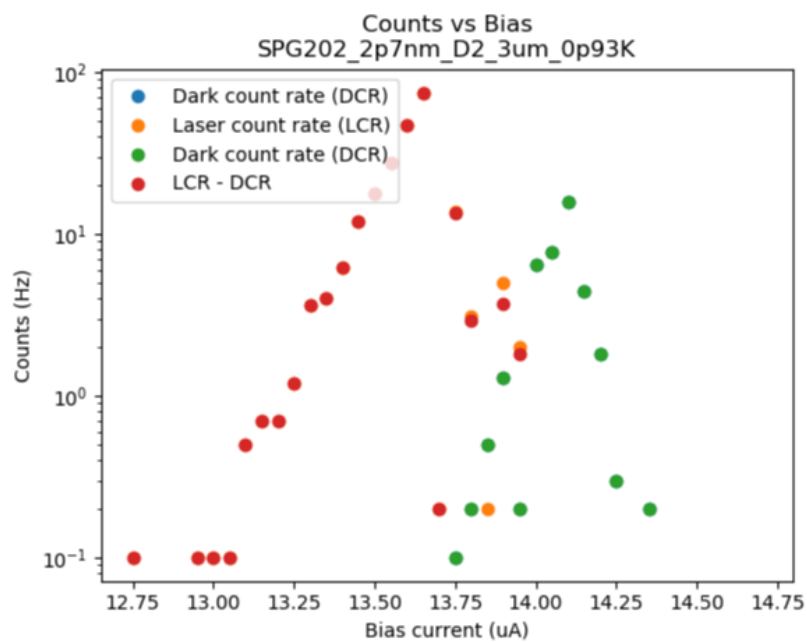
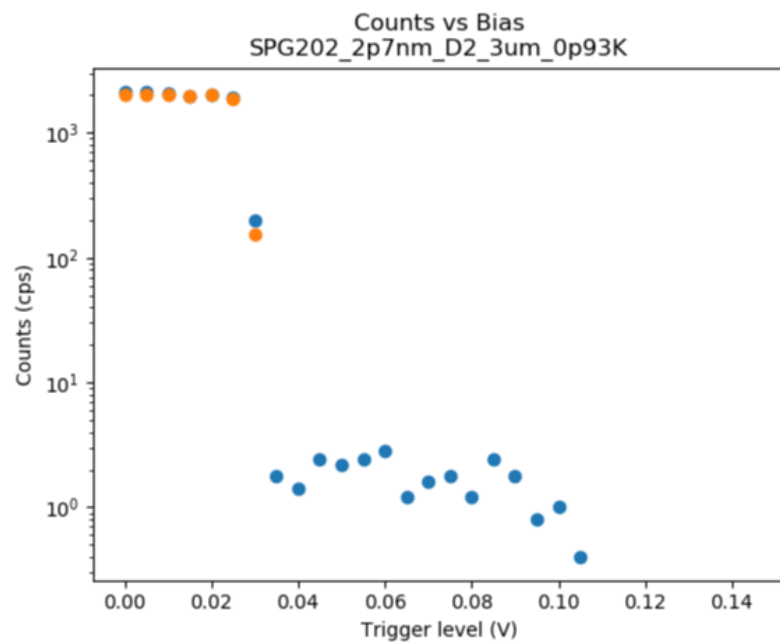


Second measurement at 0.93K



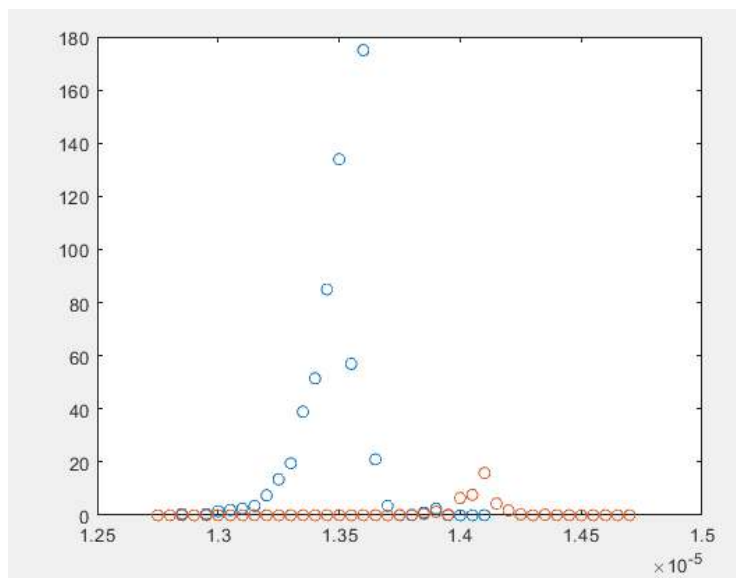
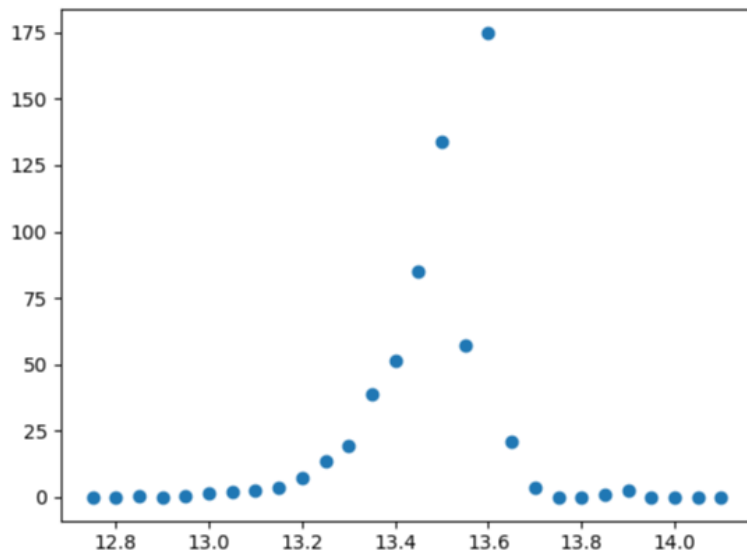
Similar latching behavior. Y axis is Volts. X is seconds





Count time was too long.

Plot below is 1550 nm, 5dB attenuation, 2 second counting time. Yaxis is Hz. Xaxis is uA.



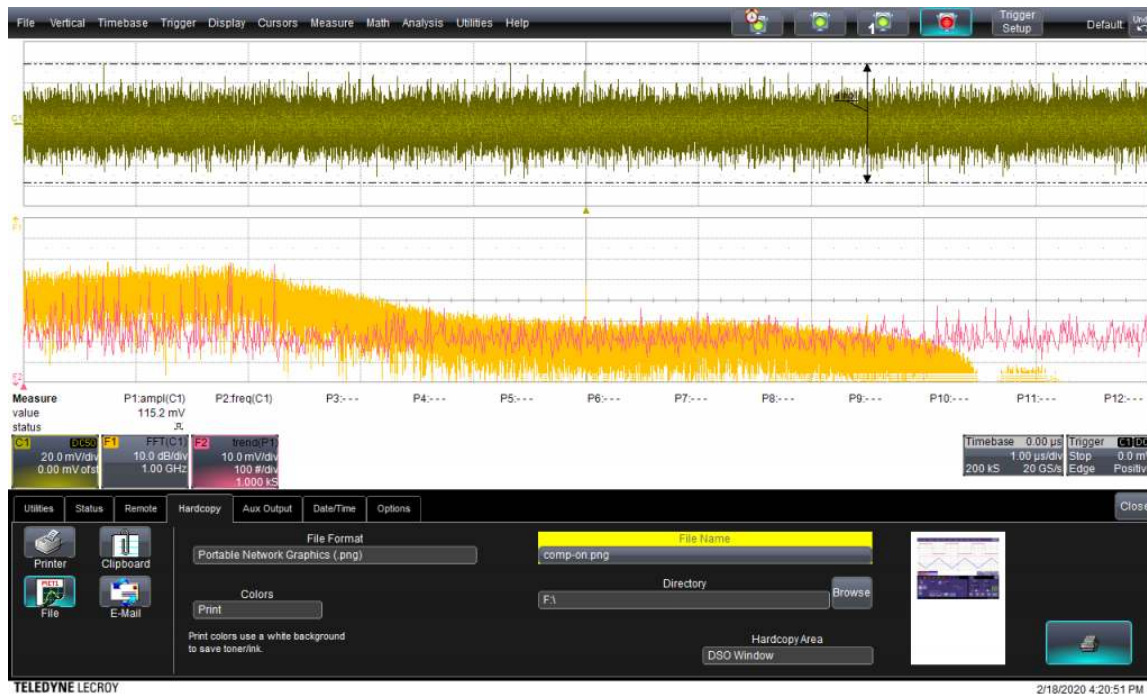
300mK noise

February 25, 2020

Categories: Cryostat

Peak 2 peak measurements

base, scope-LNA-2000-LNA2500 – Cryo under vac

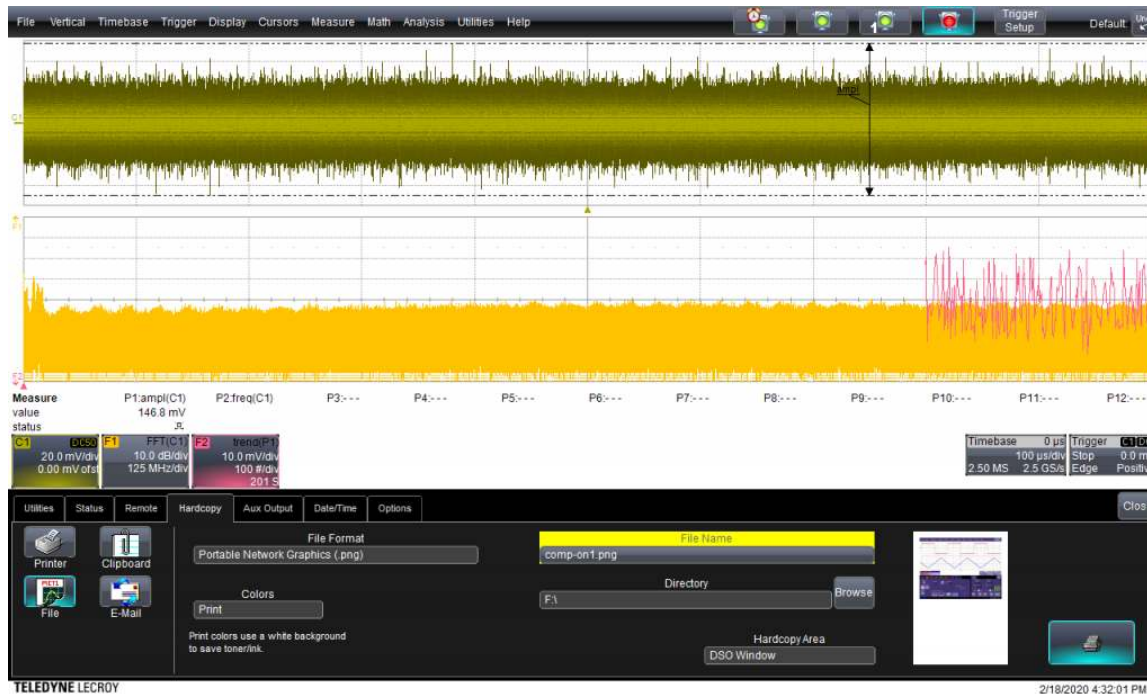


Ground braid at sma connected to scope === Same

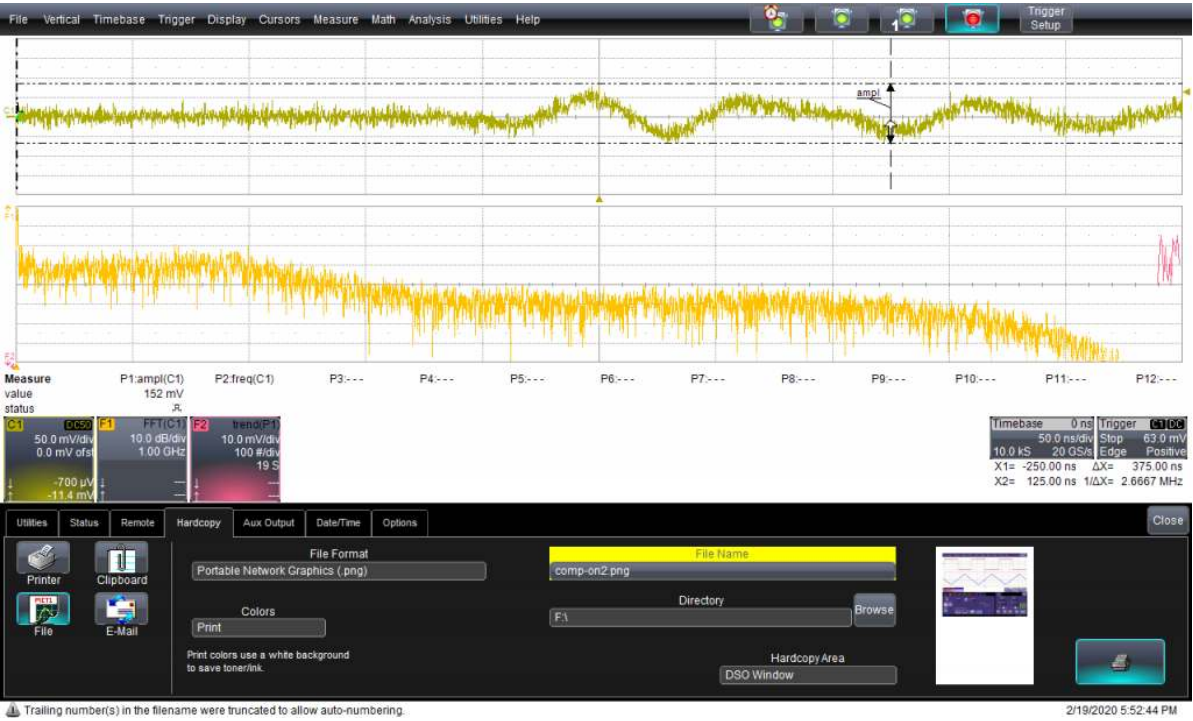
Ground braid at sma connected to wall ground === Same

Amps terminated with 50ohm powered by 12V battery === Same

Compressor on, with larger spikes corresponding to compressor freq



Zoom in on compressor pulse



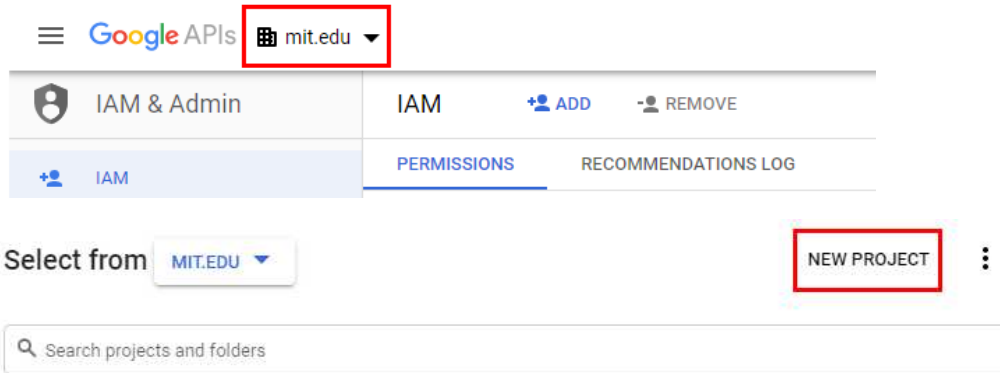
Creating an IoT Log – Google Sheets and Python

April 15, 2020

Categories: Cryostat, Lab

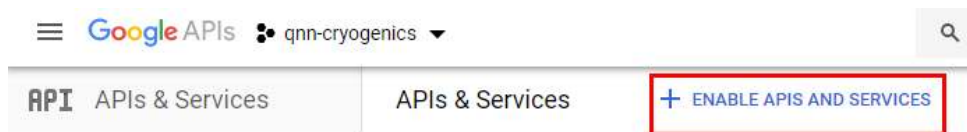
Setting up Google APIs

Start by going to console.developers.google.com (log in using your MIT Gsuite account) and create a new project.



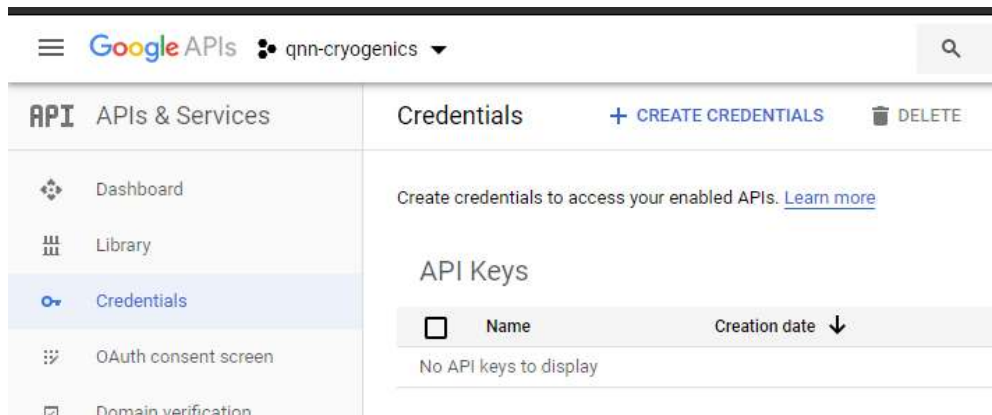
Here I have created a project called *qnn-cryogenics*. In this project I will create a gserviceaccount and show how that account can be used to connect python to a google spreadsheet. (If you would like to add to the qnn-cryogenics project please email me and I can add you)

Once your project is created we are going to add the APIs that would would like to employ. Click enable **APIs & Services**. Make sure that you can see you are under the current project qnn-cryogenics. If you do not see *enable APIs* make sure that you are in APIs and services (if not you are probably in *IAM & Admin* and you can switch using the left menu).



Simply search, click, and enable the APIs you want. For this project I have enabled the **Google Sheets API** and **Google Drive API**.

The next step is to create credentials. **Credentials** will authenticate the python script we write later. Depending on what language you are coding in some credentials might be easier than others. For python, **Service Accounts** are the easiest. Click: credentials, create credentials, service account. Then enter account name and description.



I name my service account "qnn-log" and you should see it under the corresponding section. Double click the email.

Service Accounts

☐	Email	Name 
☐	qnn-log@qnn-cryogenics.iam.gserviceaccount.com	qnn-main

This should bring you to IAM & Admin\Service Accounts\Service Account Details. Here there are two things that we need. First is simply the email attached to the service account. Simply **share** your google sheets document with this email. Second, is to scroll to the bottom and select **Create Key**. Then select JSON and then create. Move this file to a safe location on the machine you are running python on.

We are ready for python.

Getting started in Python

Controlling google sheets from python requires two packages: gspread and oauth2client. Installing using pip:

```
pip install gspread
```

```
pip install oauth2client
```

Import packages

```
import gspread
from oauth2client.service_account import ServiceAccountCredentials
```

Include scope

```
scope =
```

Setup Credentials. Change directory to location of the JSON file downloaded from the service account.

```
credentials = ServiceAccountCredentials.from_json_keyfile_name(r'C:\Users\ICE\Documents\IoT\qnn-  
cryogenics-30efacb33145.json', scope)
```

Authorize your credentials and open a work sheet. Make sure to put the name of your spreadsheet and .identify what worksheet you want.

```
gc = gspread.authorize(credentials)
```

```
wks = gc.open("Cryo Log").sheet1
```

Gspread only defined the command ".sheet1" for other worksheets use .get_worksheet(i) where i is indexed at 0.

With wks defined, the [gspread documentation](#) would be more useful to your application.

Here is an example for the 300MK cryostat.

```
scope =
credentials =
ServiceAccountCredentials.from_json_keyfile_name(r'C:\Users\aedan\OneDrive\Documents\IoT\qnn-  
cryogenics-e758cf73b682.json', scope)
gc = gspread.authorize(credentials)
wks = gc.open("Cryo Log").get_worksheet(2)

cryocon = Cryocon350('GPIB0::13')

def next_available_row(worksheet):
    str_list = list(filter(None, wks.col_values(6)))
    return str(len(str_list)+1)

start = datetime.datetime.now()

while (True):
    try:
        #Setup time and row
        now = datetime.datetime.now()
```

```
#Read temp
temp2 = cryocon.read_temp( channel='D2')
temp3 = cryocon.read_temp( channel='D3')
temp4 = cryocon.read_temp( channel='D4')

#Insert Row at top of page. Delete last row
wks.insert_row(,index=2)
wks.delete_row(index=3000)

sleep(30) # Google only accepts a number of requests per 100s.🔒
```

I have attached the full script below. There are two common errors from the google API that can be caught by refreshing the credentials and waiting.

[Heres a link to the published cryo log.](#)

Creating a .exe from your Python script

One problem with everything described thus far is that the script is using the python kernel we would generally be using for measurements. To avoid this and allow our program to run in the background, we can generate an executable from our script.

Before creating an .exe it is wise to test your script thoroughly. If your .exe crashes there will not be any error message, making it very difficult to debug.

```
pip install pyinstaller
```

Then open a command window were your file is located.

```
pyinstaller -w -F yourscrip.py
```

This will create two folders and your .exe will be in the *dist* folder. Then run it!

Full script

```
# -*- coding: utf-8 -*-
"""
Created on Sat Apr 11 11:25:39 2020

@author: omedeiro
"""

import sys
my_module_dir = r'C:\Users\aedan\OneDrive\Documents\IoT'
my_module_dir1 = r'C:\Users\aedan\OneDrive\Desktop\snsdp-measurement-code\instruments'
if my_module_dir not in sys.path:
    sys.path.append(my_module_dir)
    sys.path.append(my_module_dir1)

import datetime
import time
from cryocon350 import *
#####
import gspread
from oauth2client.service_account import ServiceAccountCredentials

scope =
credentials =
ServiceAccountCredentials.from_json_keyfile_name(r'C:\Users\aedan\OneDrive\Documents\IoT\qnn-
cryogenics-e758cf73b682.json', scope)
gc = gspread.authorize(credentials)
wks = gc.open("Cryo Log").get_worksheet(2)
```

```

cryocon = Cryocon350('GPIB0::13')

def next_available_row(worksheet):
    str_list = list(filter(None, wks.col_values(6)))
    return str(len(str_list)+1)

start = datetime.datetime.now()

while (True):
    try:
        #Setup time and row
        now = datetime.datetime.now()
        #Read temp
        temp2 = cryocon.read_temp( channel='D2')
        temp3 = cryocon.read_temp( channel='D3')
        temp4 = cryocon.read_temp( channel='D4')

        #Insert Row at top of page. Delete last row
        wks.insert_row(index=2)
        wks.delete_row(index=3000)
        wks.update_acell('E1',str(now-start))
        sleep(30) # Google only accepts a number of requests per 100s.
    except gspread.exceptions.APIError:
        print('error 1')
        print(str(now))
        sleep(100)
        credentials =
        ServiceAccountCredentials.from_json_keyfile_name(r'C:\Users\aedan\OneDrive\Documents\IoT\qnn-
        cryogenics-e758cf73b682.json', scope)
        gc = gspread.authorize(credentials)
        wks = gc.open("Cryo Log").get_worksheet(2)
    except ConnectionError:
        print('error 2')
        print(str(now))
        sleep(100)
        credentials =
        ServiceAccountCredentials.from_json_keyfile_name(r'C:\Users\aedan\OneDrive\Documents\IoT\qnn-
        cryogenics-e758cf73b682.json', scope)
        gc = gspread.authorize(credentials)
        wks = gc.open("Cryo Log").get_worksheet(2)

```


qnn-nas

August 28, 2020

Categories: General, Lab, Operations

Access your measurement data from anywhere. Back up your measured data daily. Protect your data from drive faults. Save historical versions of data.

Static IP: qnn-nas-rle.mit.edu (18.25.16.44)

Basic access

username: lab

pw: group_password

Personal accounts can be created. Contact admin (Owen)

Map qnn-repo to Q:

Map Data to S:

Map Archive to A:

SPG277 resonator

October 29, 2020

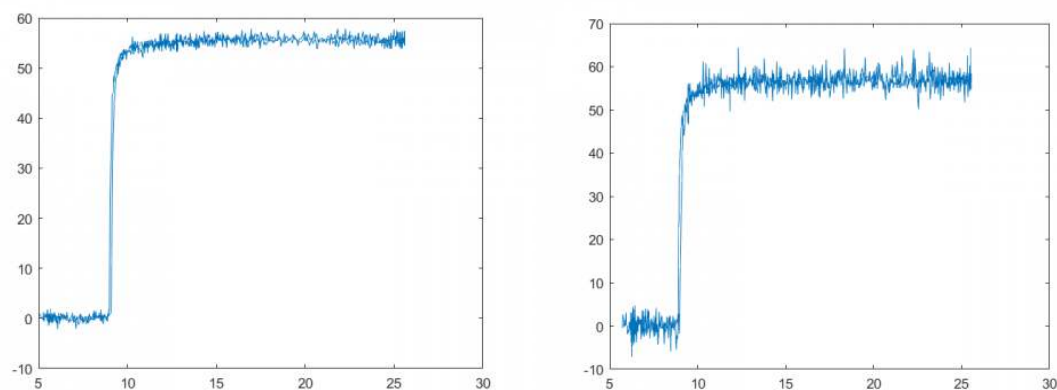
Categories: Electronics, Fabrication, Kinetic inductance

I am writing this post after taking the first measurements of the chip. There will be plenty of mistakes/bad practices below but it is a good opportunity to detail these mistakes before a second fab run. This design was created by Brenden.

[Fabrication Process for NbN Superconducting Resonator.pdf](#)

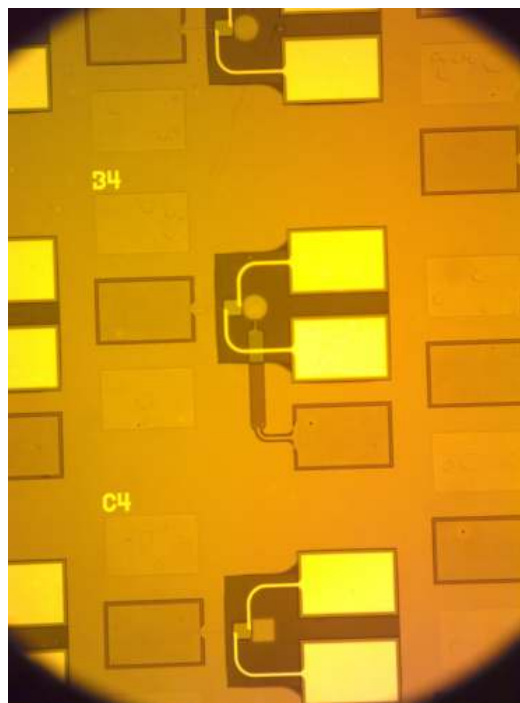
The pdf includes entire fabrication process and additional information about film and T_c . 2% HSQ spacer/bake did not change T_c SPG280 and SPG279 (9.1K, 9.0K).

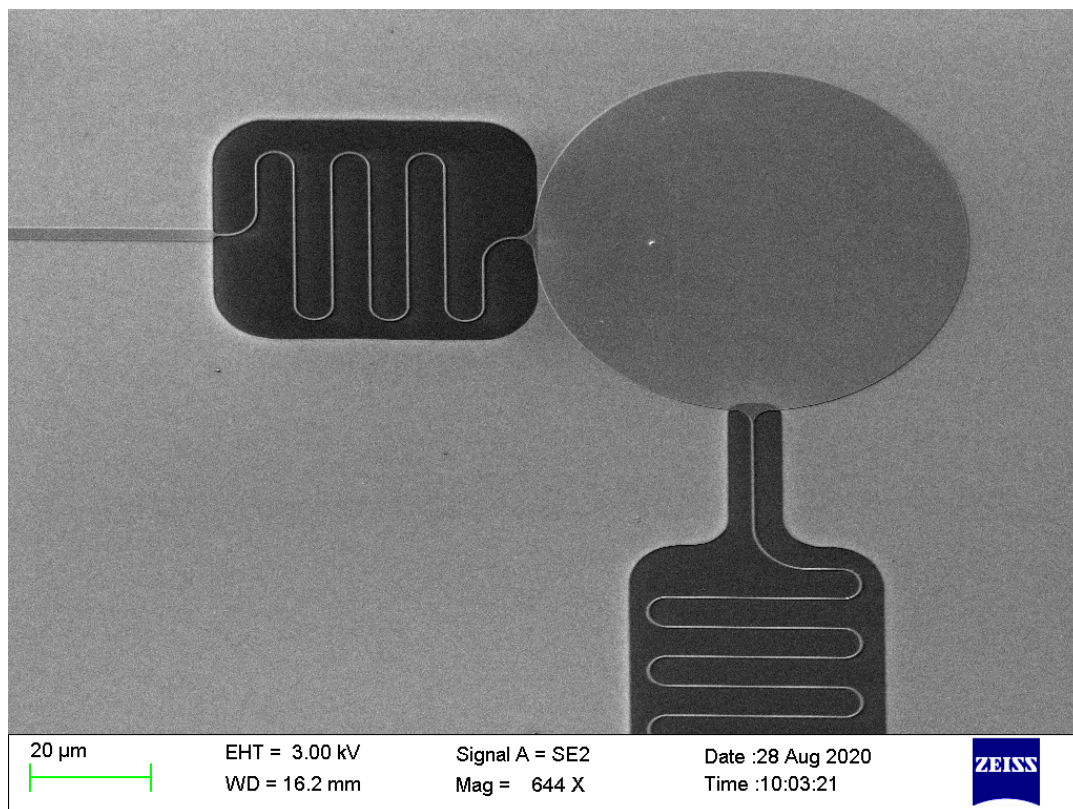
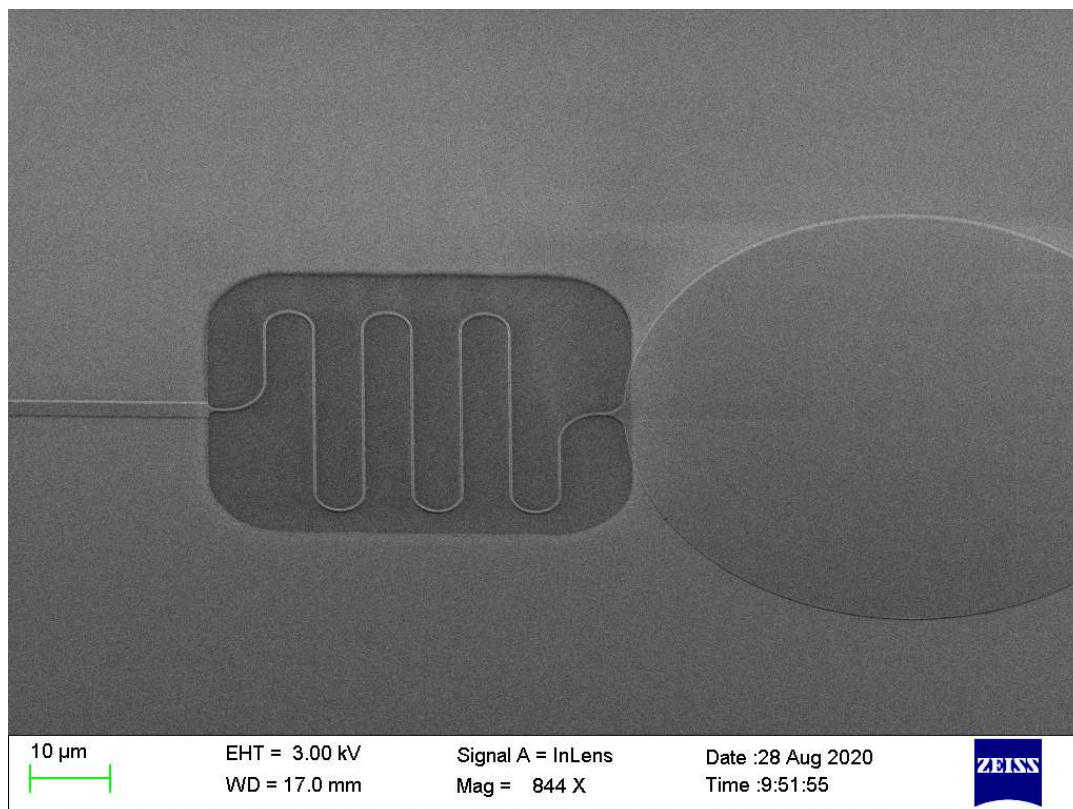
T_c of sister chips SPG276-Ground plane|| SPG283-Device Layer



Here are the devices.

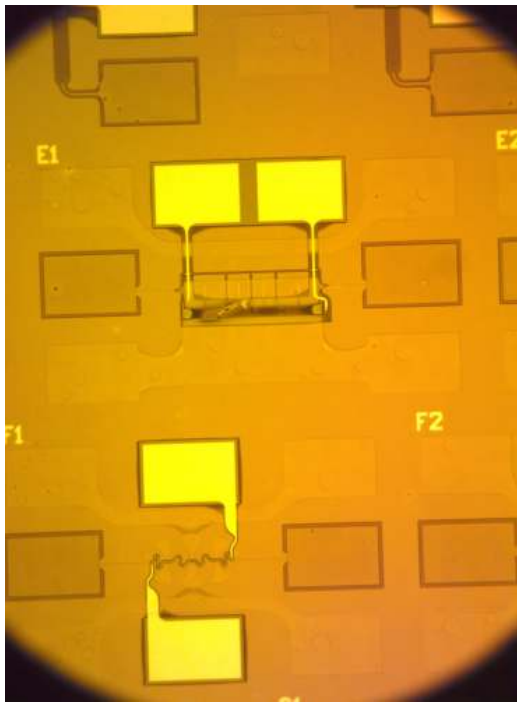
Resonator with drive line and heater. Pad the left center is referred to as the "main port" in this post, the bottom right is called the feed/drive line. and the gold pads are the heater



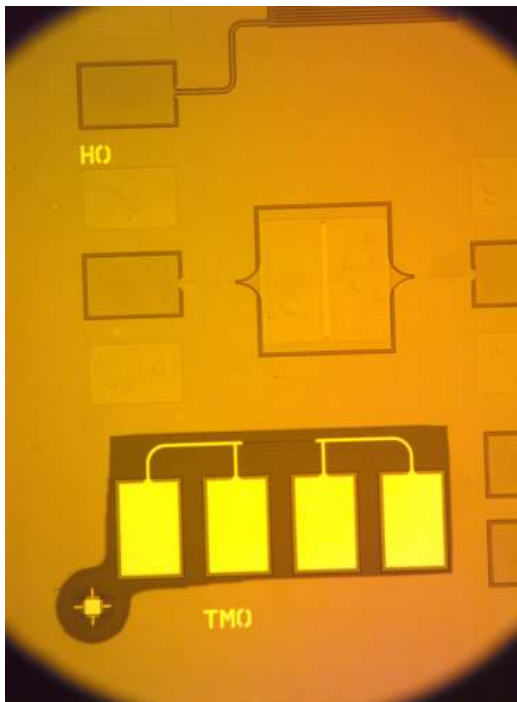


Detritus from 6% HSQ.

High pass and low pass filters. You can see the problems I had exposing large areas of 6% HSQ. I did not include PEC and I did not calibrate the dose, borrowed values from Marco. He helped me go through a PEC and the dose reduction in some areas is quite significant considering there is a lot of oxide. ~400nm. I have not tested these devices yet.



Another filter + 4point test structure

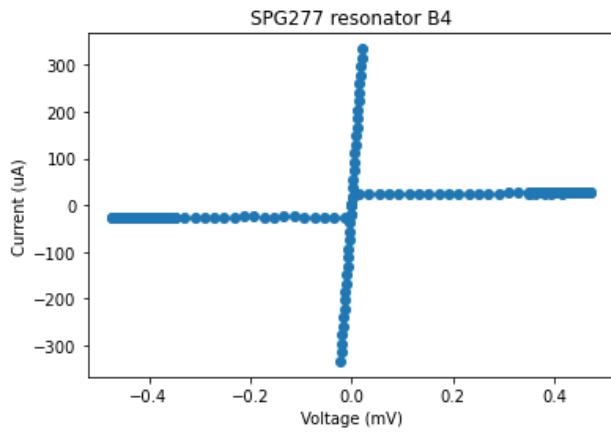


Overall not great. But RT measurements tell us that the idea of using 2% HSQ as a spacer would work.

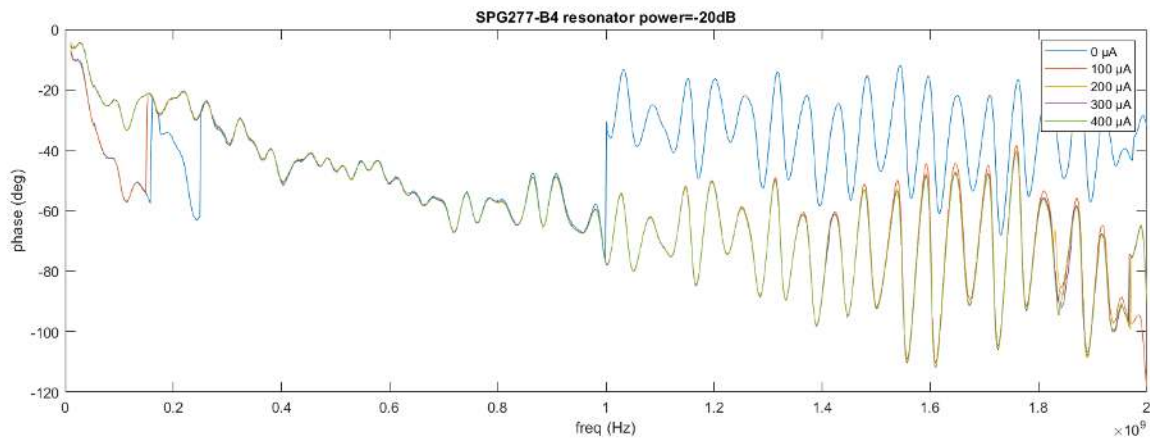
Initial Tests

10/27/2020

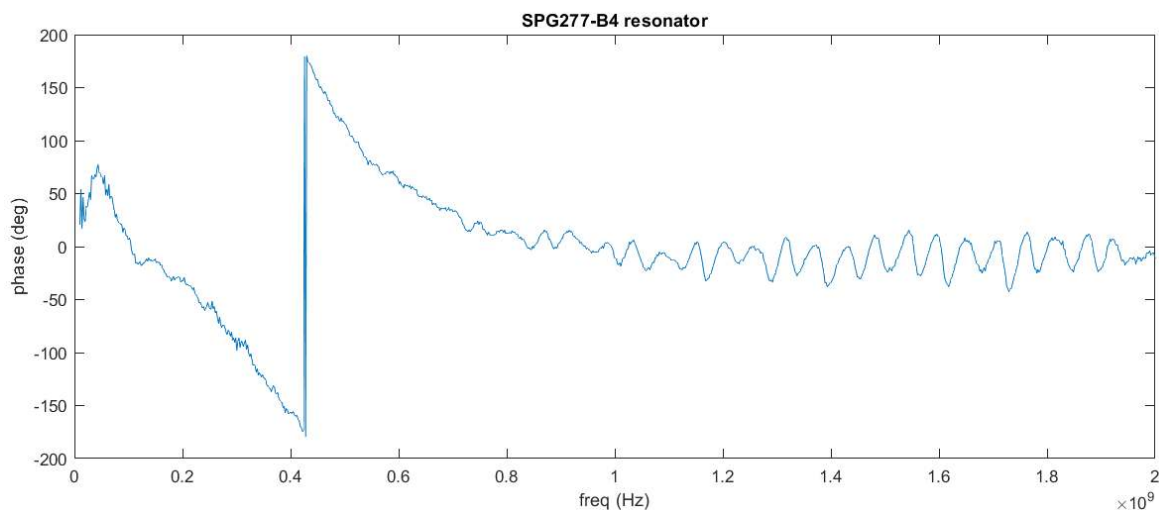
B4 IV curve. $I_c = 334\mu A$



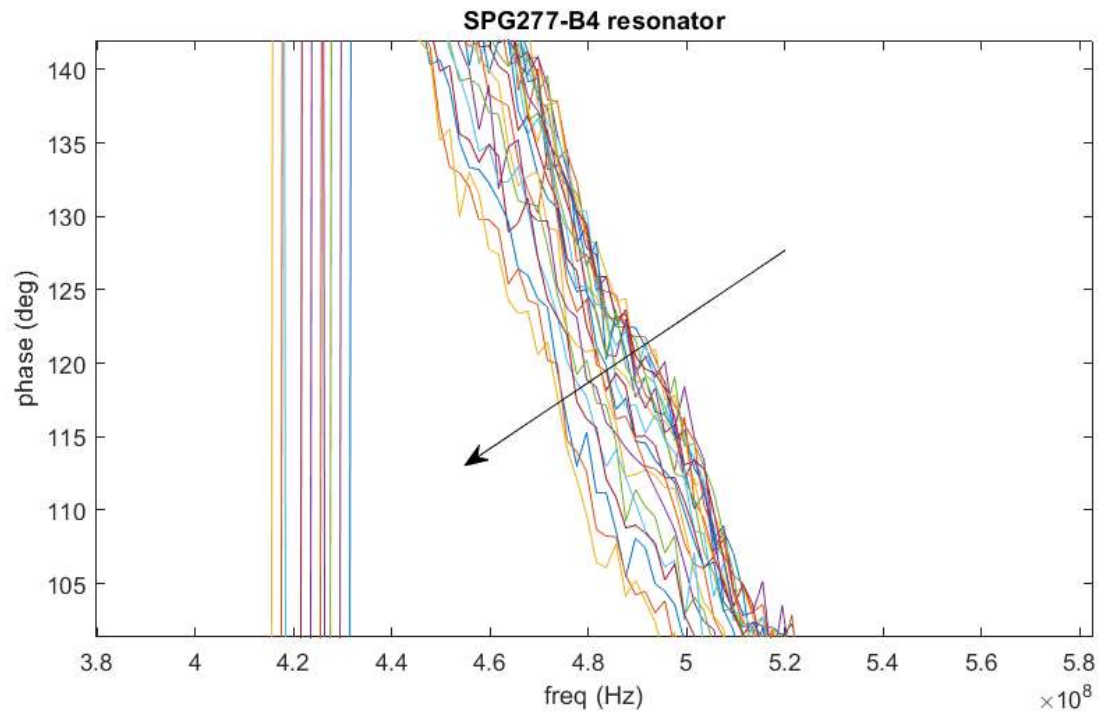
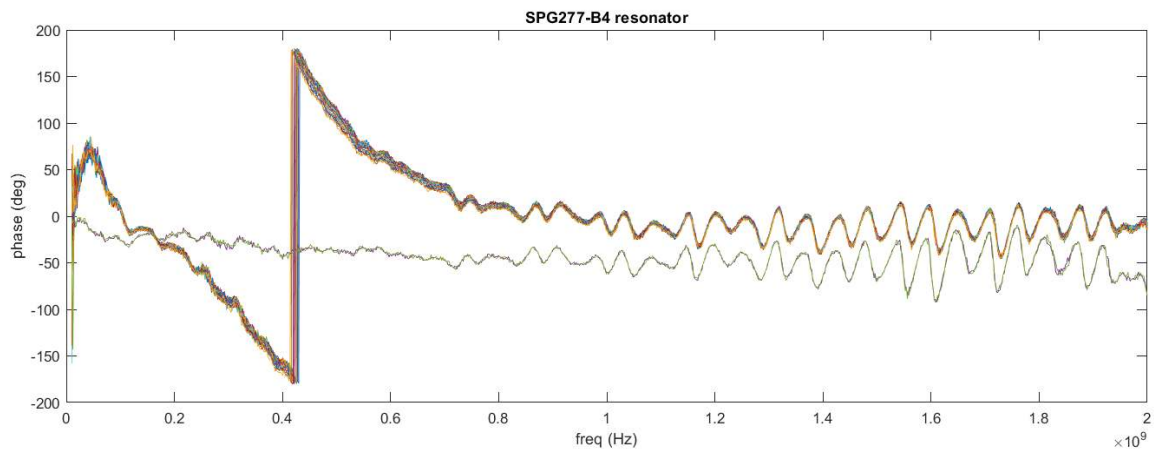
Here I am applying a bias current to the device on the main port and ground on the feed line and monitoring the frequency response. Nothing is visible in the S11 magnitude so I will only consider the phase. The jump in phase at 1GHz was promising, that is the exact resonant frequency we designed for, but it is too exact. Zooming in it is exactly 1GHz... would lead me to believe that it is an artifact of the experiment or the setup. Here the phase is unwrapped by setting and electrical delay of $\sim 9\text{ns}$. Interestingly, the jump goes away once the wire is switched, which makes us think that the 1GHz jump in phase might be due to the device. You can see that as the current increases further the low frequency artifacts go away ($0 \rightarrow 100 \rightarrow 200\mu\text{A}$).



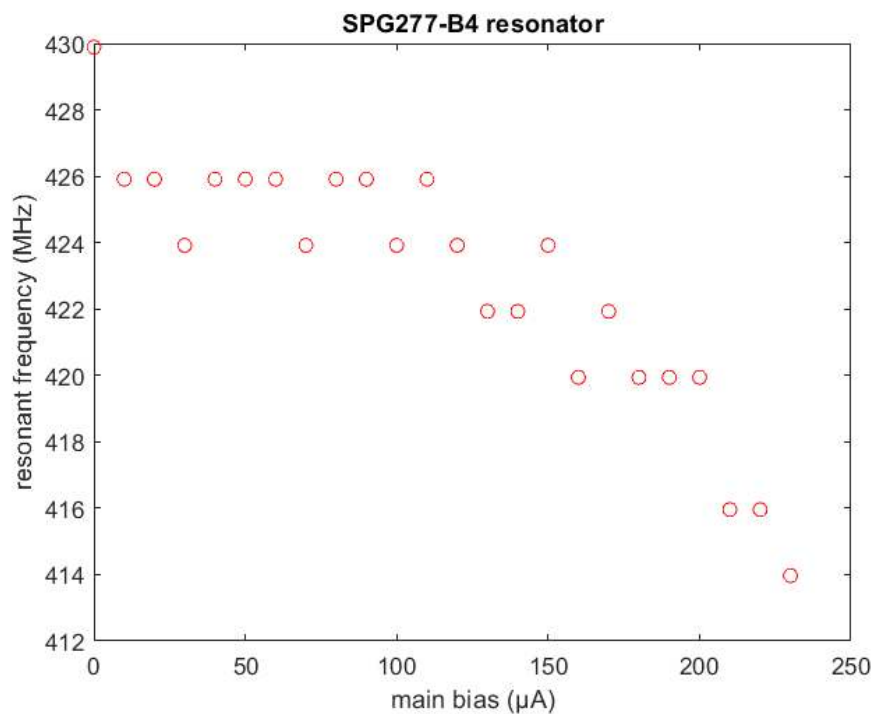
At lower power, **-40dB** there is a pronounced flip in the phase but at a much lower frequency. This is more reasonable.



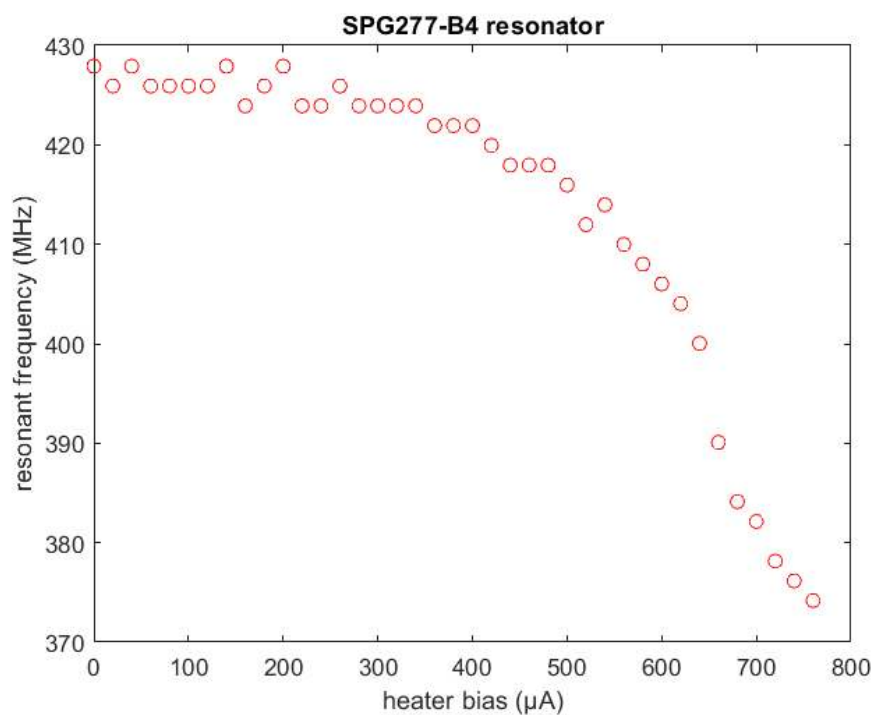
Above is zero bias to the main port. Below is a sweep of bias currents to the main port, the lower traces is when the wire is switched. The arrow shows increasing bias.

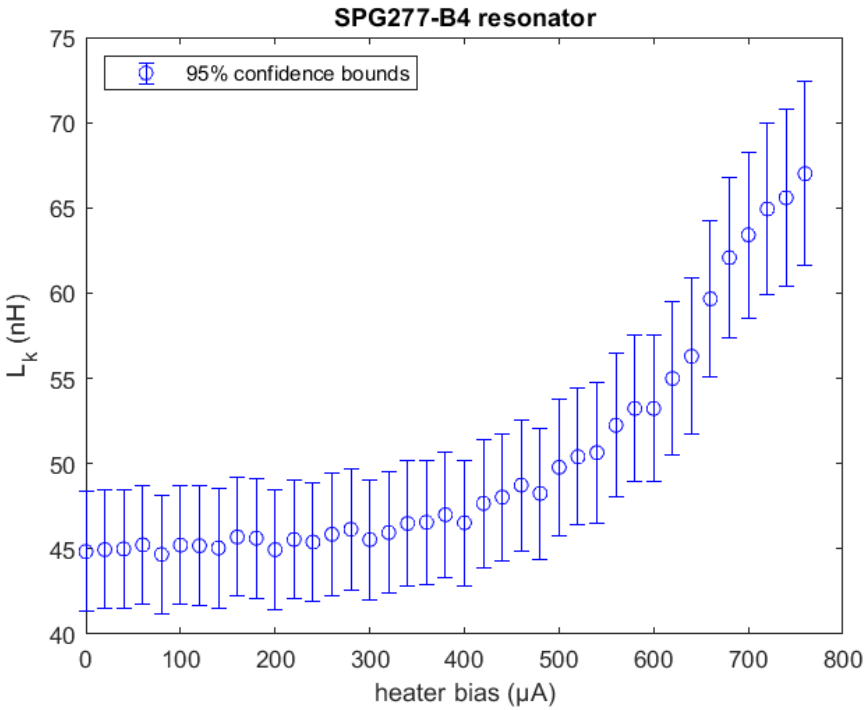
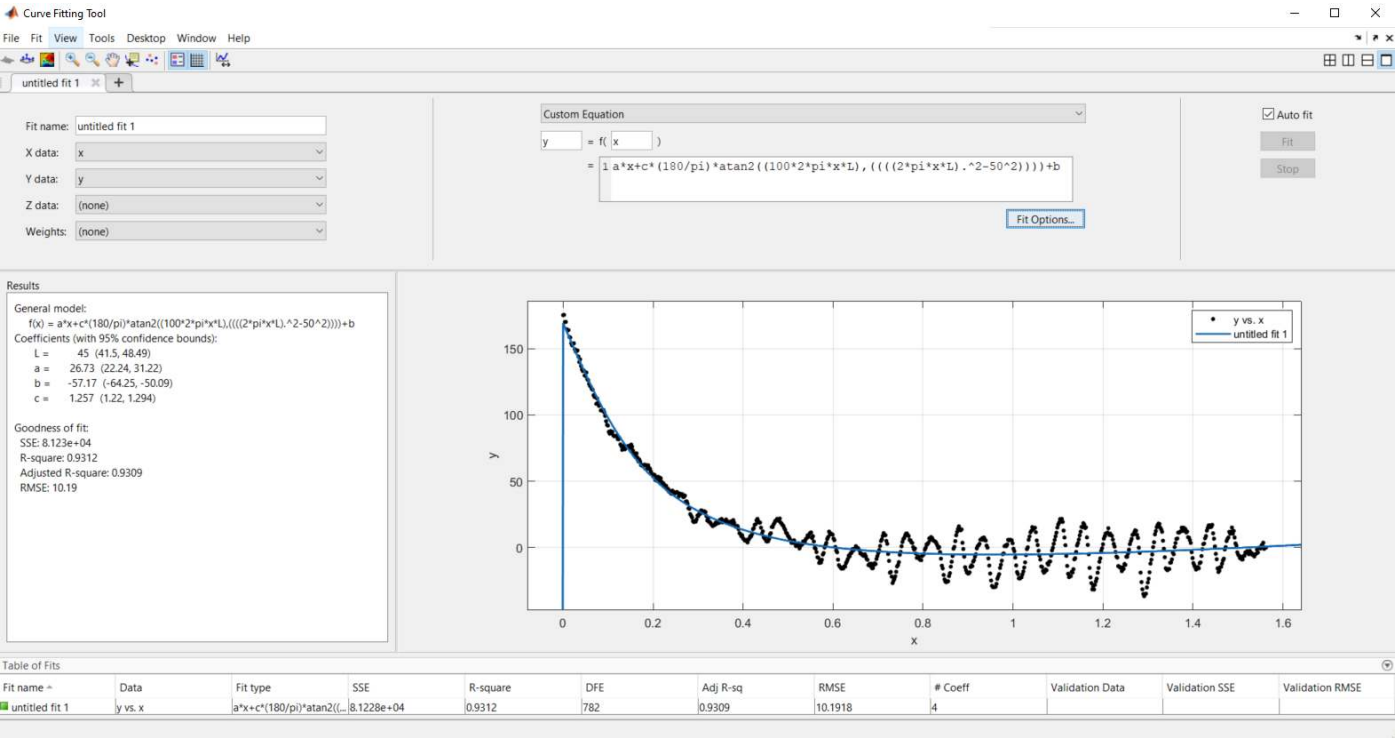


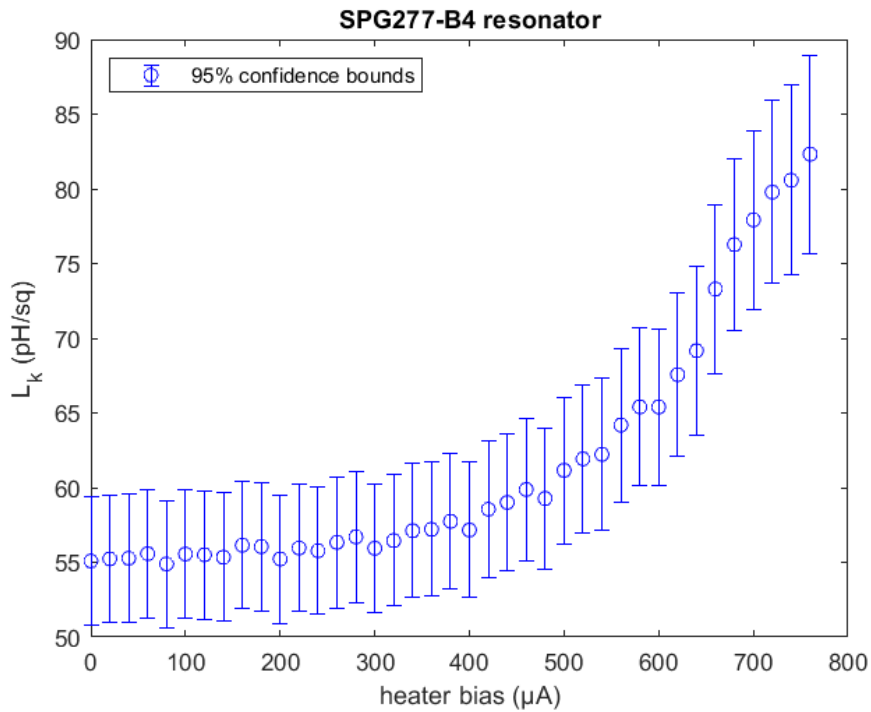
Plotting the resonant frequency as a function of the main port bias. The error in the points below is from careless matlab coding that can be improved later.



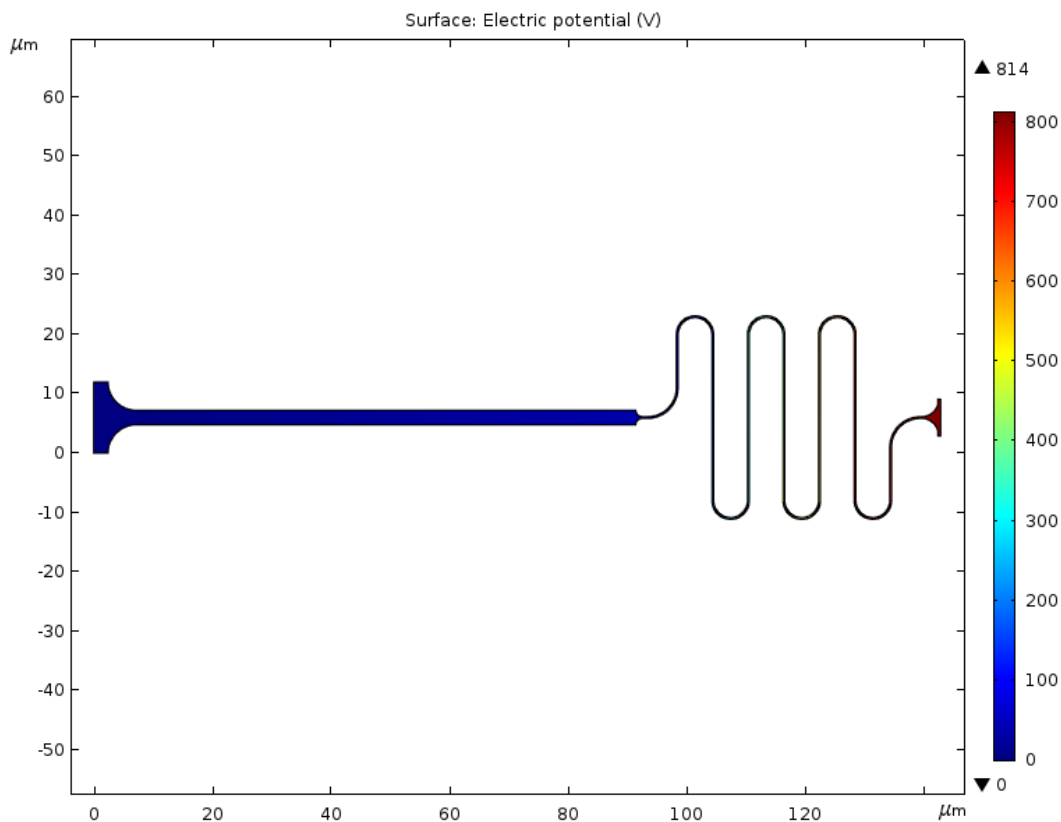
The same process can be repeated for the heater. You can see a larger shift in the frequency by applying heat rather than applying bias current.



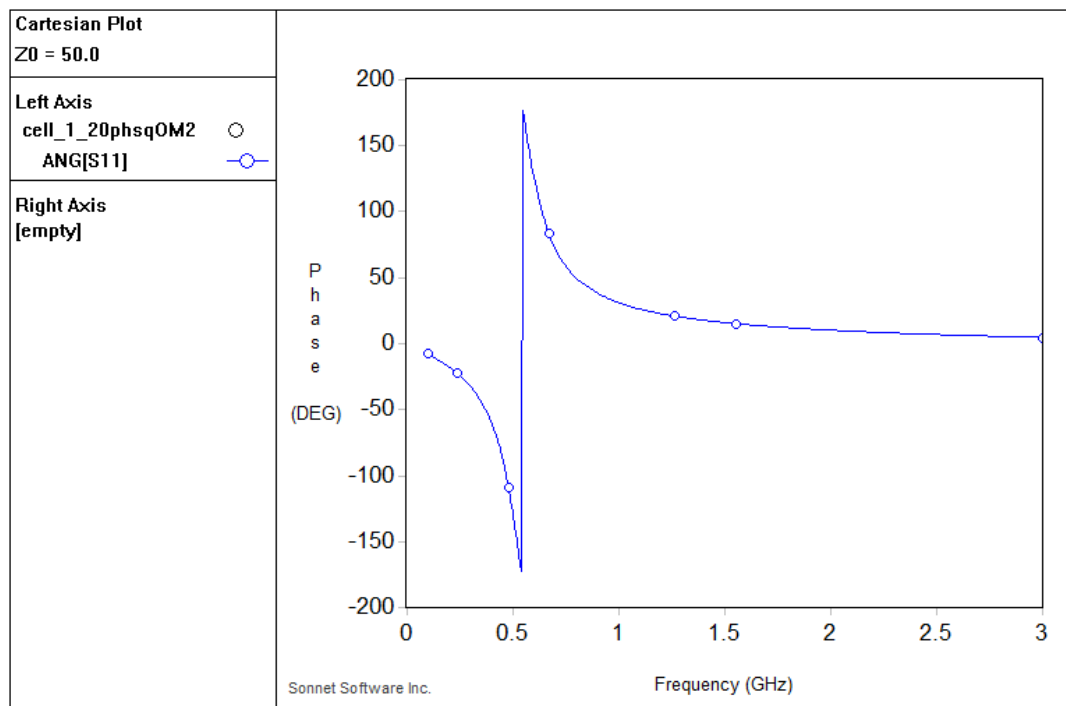




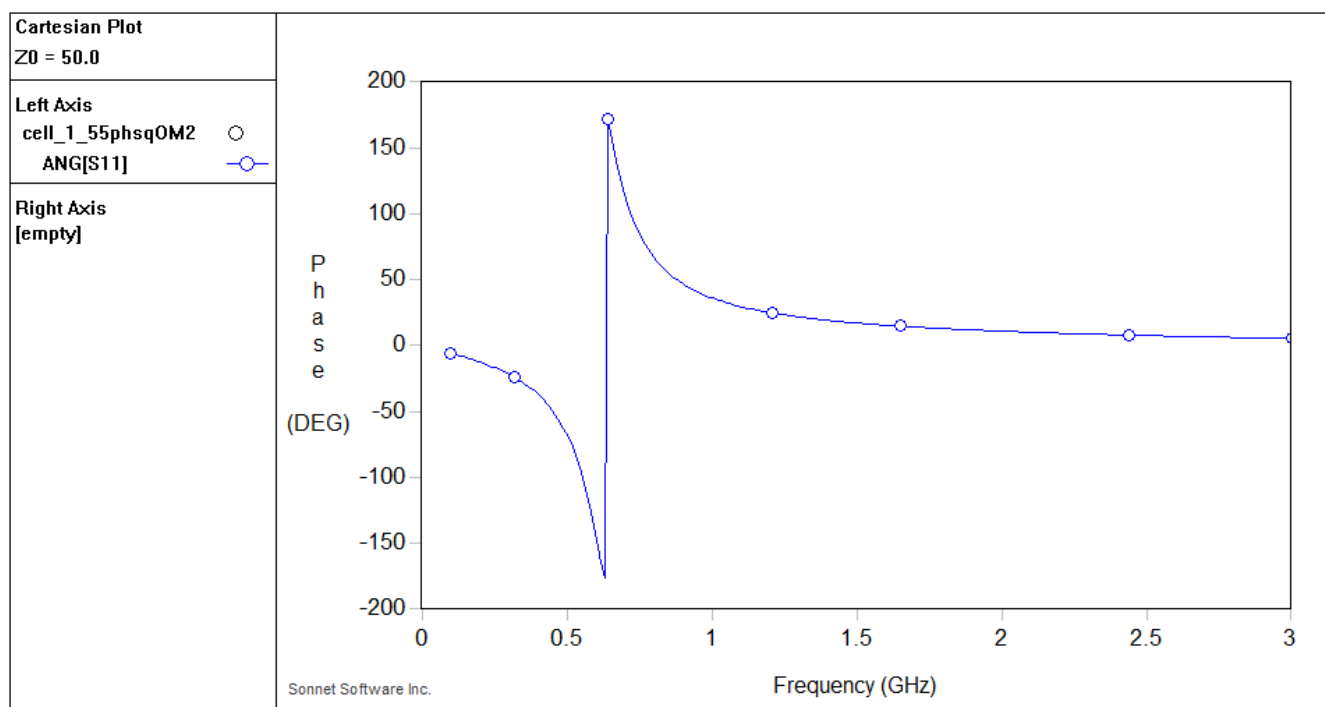
These values are about 10pH/sq higher than SPG200 27nm

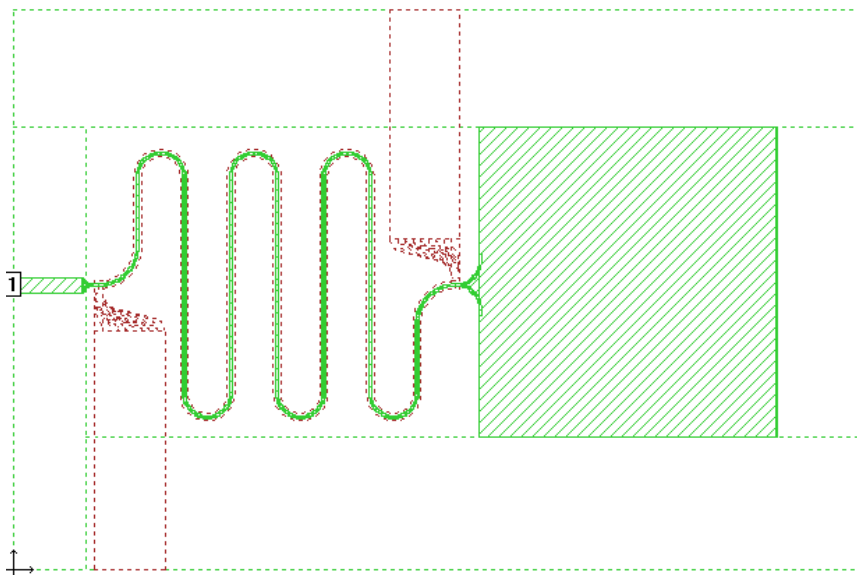
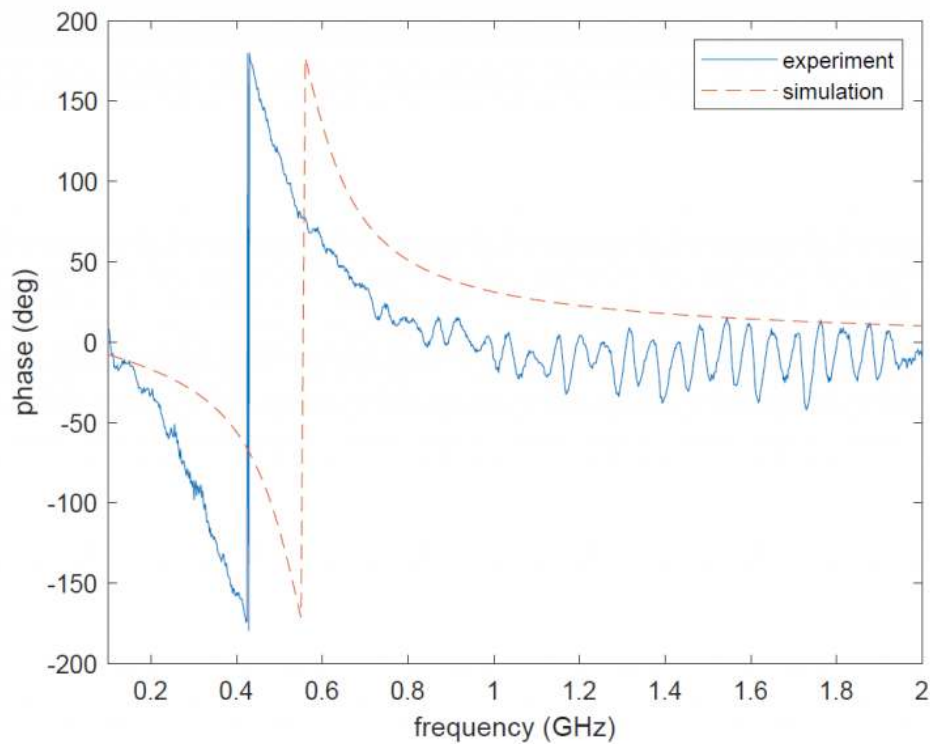


Sonnet simulation (Brenden). **With adjusted L_s (55pH/sq)**, the resonant frequency is pretty spot on but assumes the spacer dielectric constant is that of SiO₂ $\epsilon_r=3.9$. In the plot it says cell_1_20ph which is the file name and not the correct value for inductance.



The plot below is using 55pH/sq and a $\epsilon_r = 2.9$ for the HSQ spacer.





Notes

HSQ refractive index 1.398. MC said to use 2.9 for ϵ_r at microwave frequencies

Links to Andrew's posts that used this fitting

| *Replicating phase vs frequency vs power using LTSPICE:*

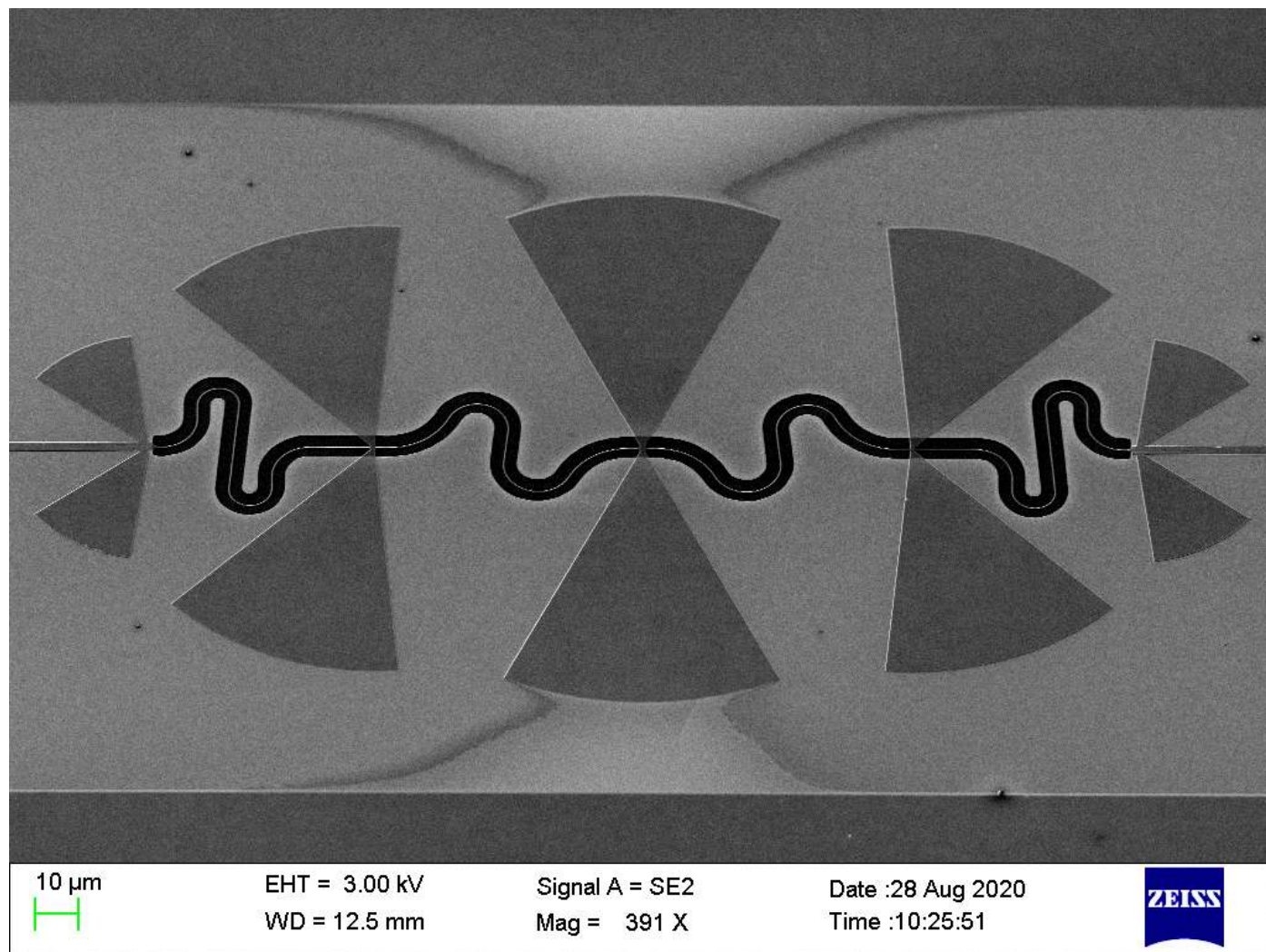
| *TaN resistors in the 300mK Cryo*

In case I cant find anything... the data is located at G:\My Drive\...\Projects_electronics\resonator\SPG277\resonator\B4

Bias Tee

Appendix

I am now wondering if the exposure problem between the largest capacitor and the outer film is actually the 2% HSQ spacer. It could be that it was not completely cured from the bake time. and that the ebeam for the device layer injected additional energy. If it is actually 6% HSQ from the device layer write then there should be NbN underneath it, but it does not appear that way.



SPG211 nMem

November 24, 2020

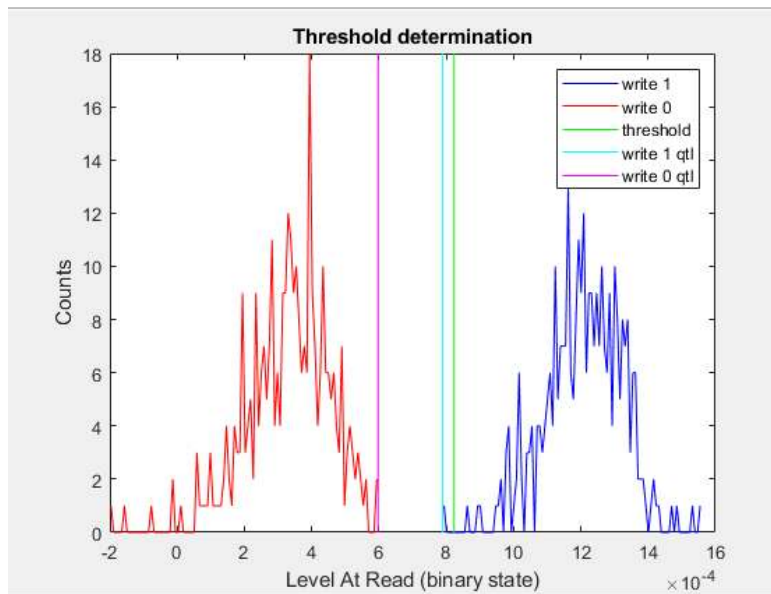
Categories: Electronics

11/23/2020 testing in the dewar using the RF probe. The probe is still leaking so it was not pumped down and the chip was covered in resist to reduce the noise from helium bubbles generated by the heater. Initial optimization of the write bias and the heater level did not return any improved operation.

Later, we (BB and OM) decided to depressurize the RF probe and we were surprised to see drastic improvement in the separation of logic states. We captured the image below where you can see switching currents of 1/0 shown in the bottom axis as orange-ish and light-ish pink. The regions of noisy overlap (directly in the center and to the right most side) were captured when the valve on the RF probe was closed. The flat and separated regions the left and directly above the word "adjust" were captured when the valve was open. During this measurement the pressure in the dewar was about 3psi and there was slight positive pressure at the RF probe valve, which we left open and covered with tin foil.



Below is a plot of 1000 points from the flat separated section. Showing zero bit errors. We will perform further measurements in a cryostat.



SPICE simulation of two stage nTron amplifier

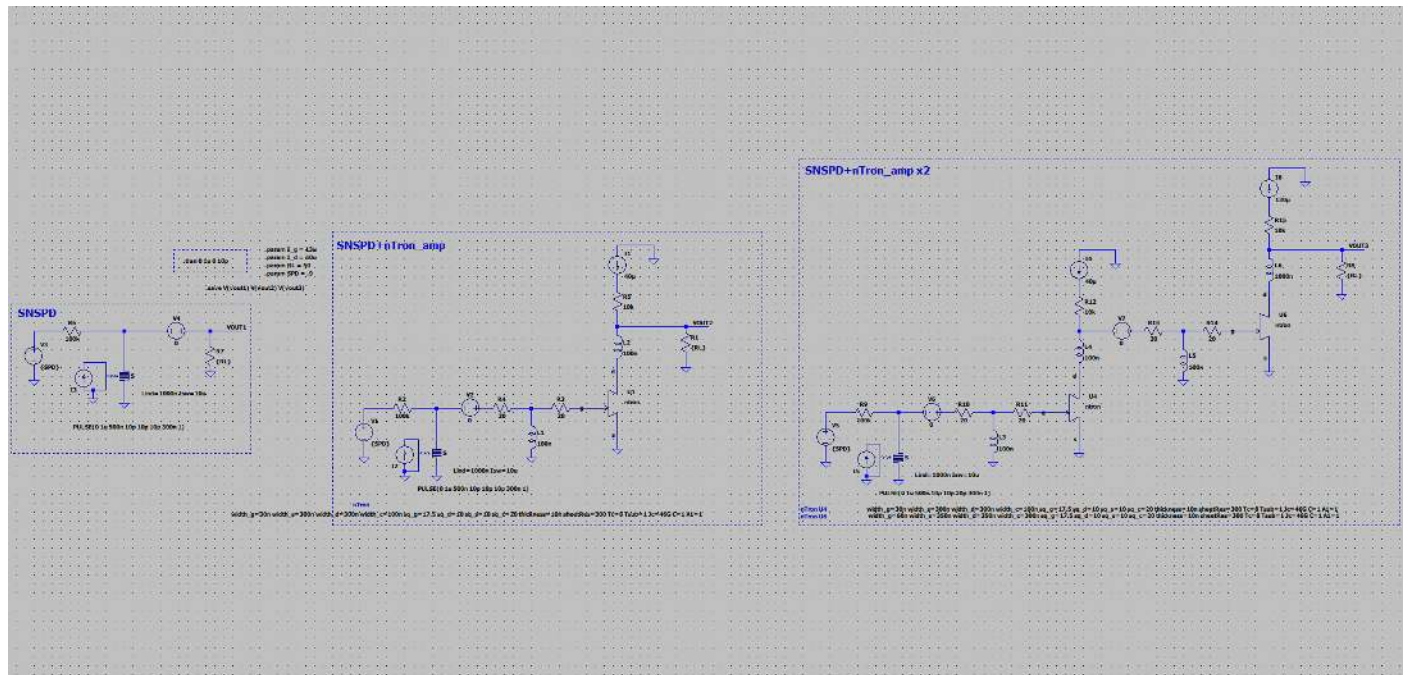
November 29, 2020

Categories: General, nTron

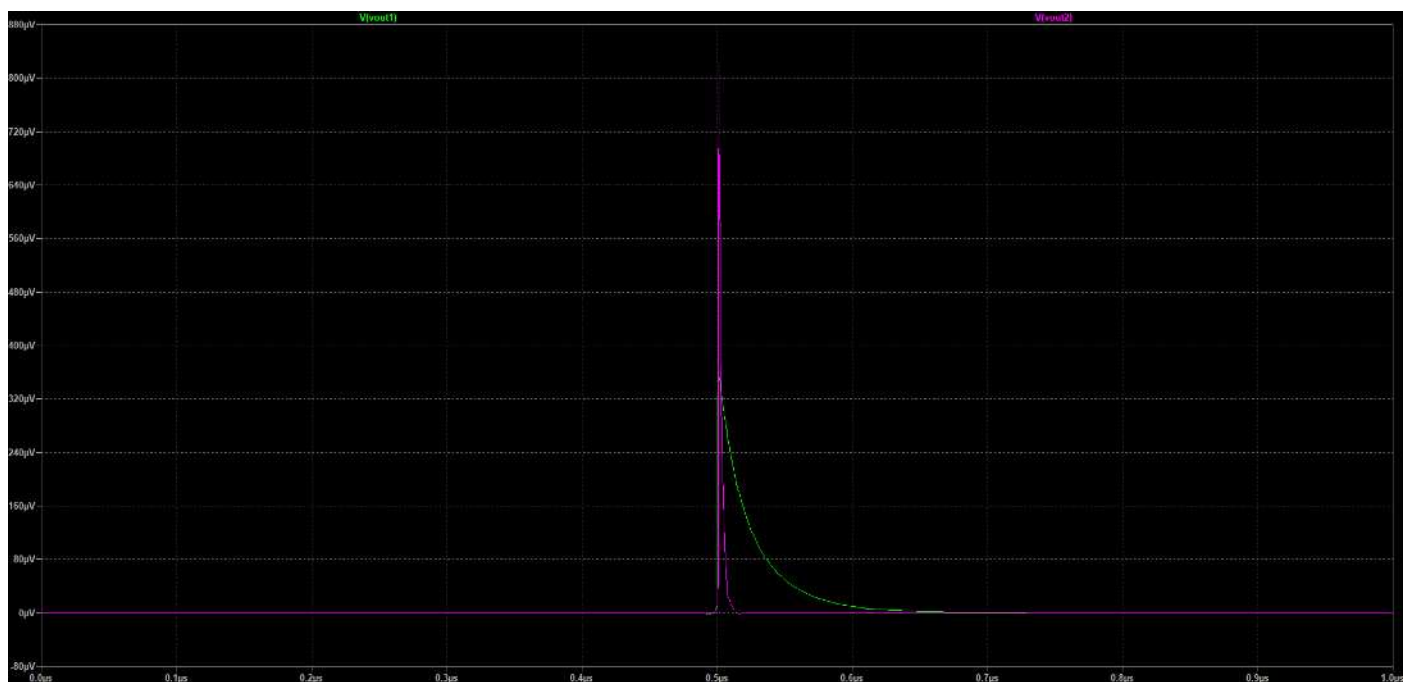
This post contains a SPICE model for a two stage nTron amplifier and some useful links to older nTron blog posts. The circuit uses Matteo's nTron model with realistic geometries. The circuit design is taken from Zhao's encoder paper which is linked below.

[nTron_snsdp.zip](#)

Circuit



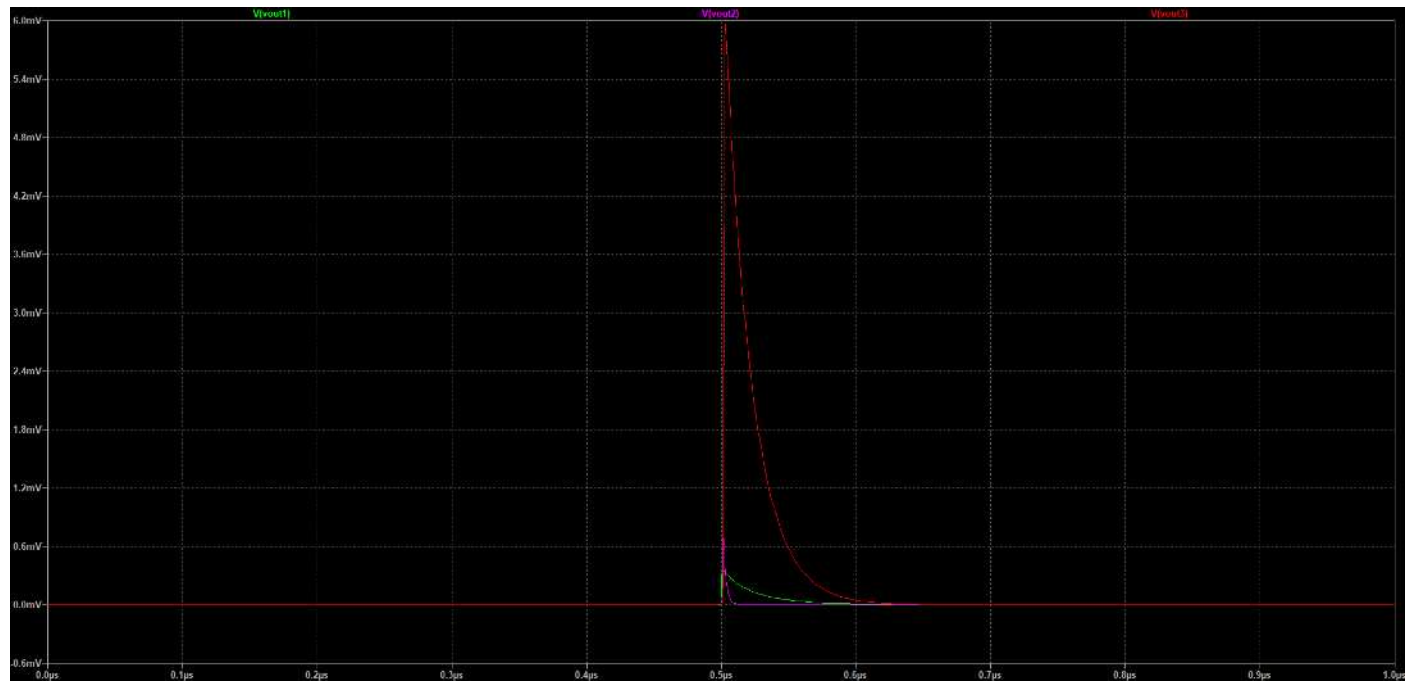
First stage output



Green pulse is the photon output. Purple pulse is the nTron output.

Second stage output

Requires large inductance to avoid latching. Fast operation can be achieved by clocking the channel.



The red pulse is the second nTron output.

Reference: [Zhao's encoder paper](#)

Links to other blog posts

Design: SNSPD timing jitter improvements using differential nTron configuration & new study of the propagation velocity

nTron Circuit experimental Plan:

hTron, cTron and potential tTron

Multiple-nTron SNSPD Amplifier

SNSPD with nTron amplifier

nTron design notes

December 1, 2020

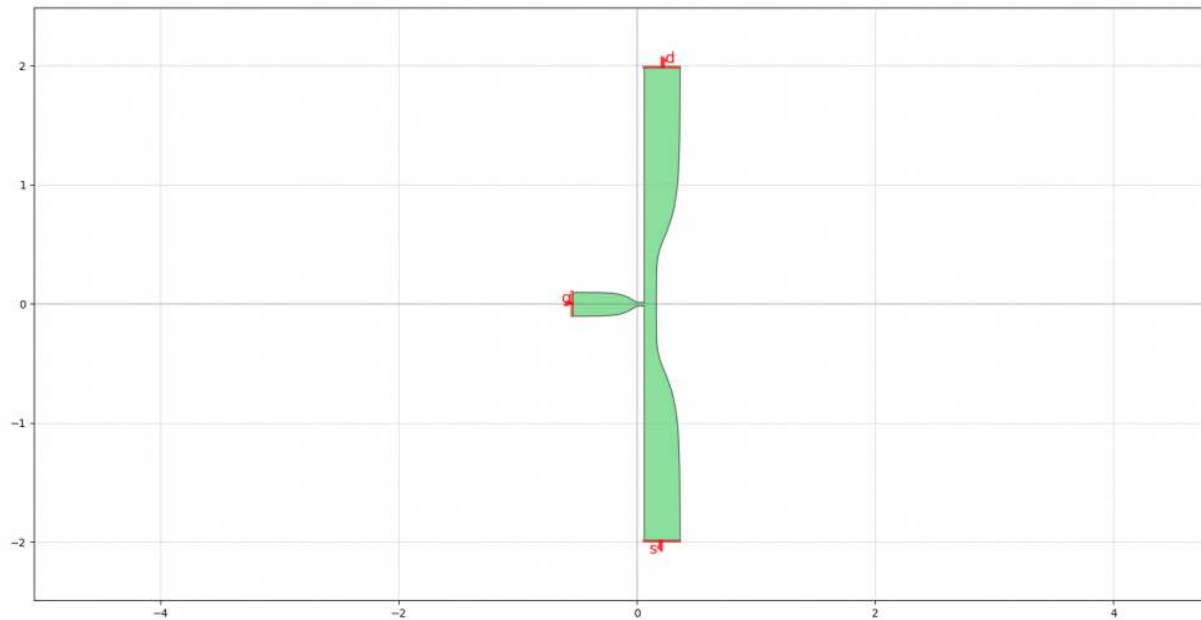
Categories: nTron

Resistors

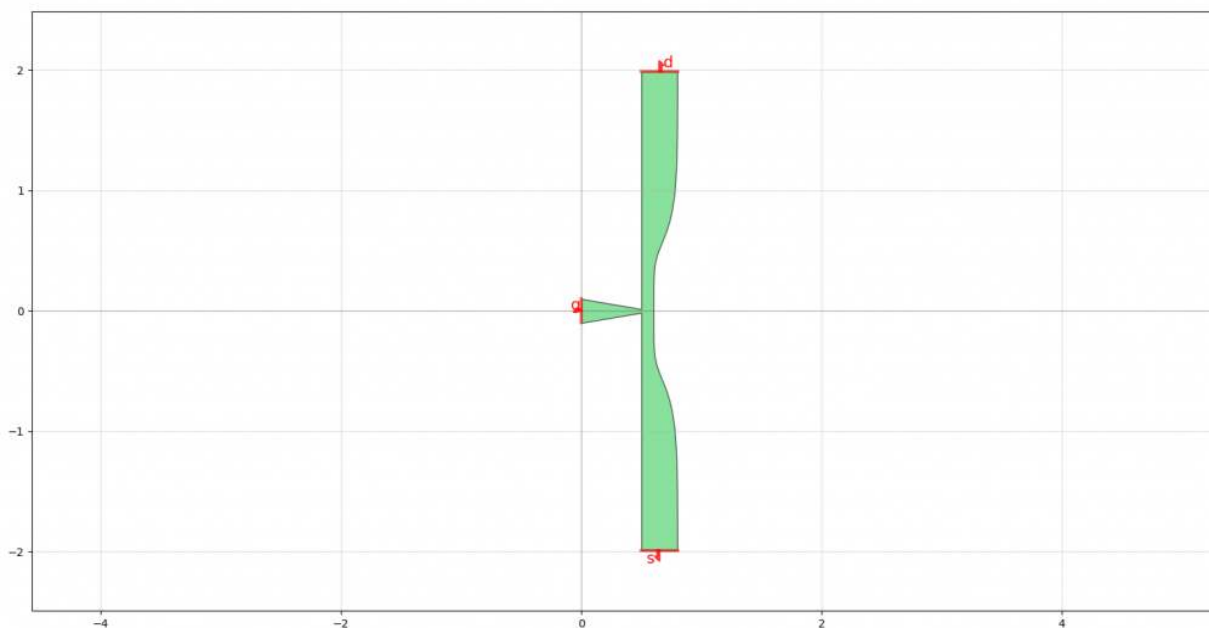
Matteo's thesis reports 10nmTi+25nmAu for $\sim 5\Omega/\text{sq}$. Needs to be deposited first to minimize contact resistance.

Using 50pH/sq for NbN Lk.

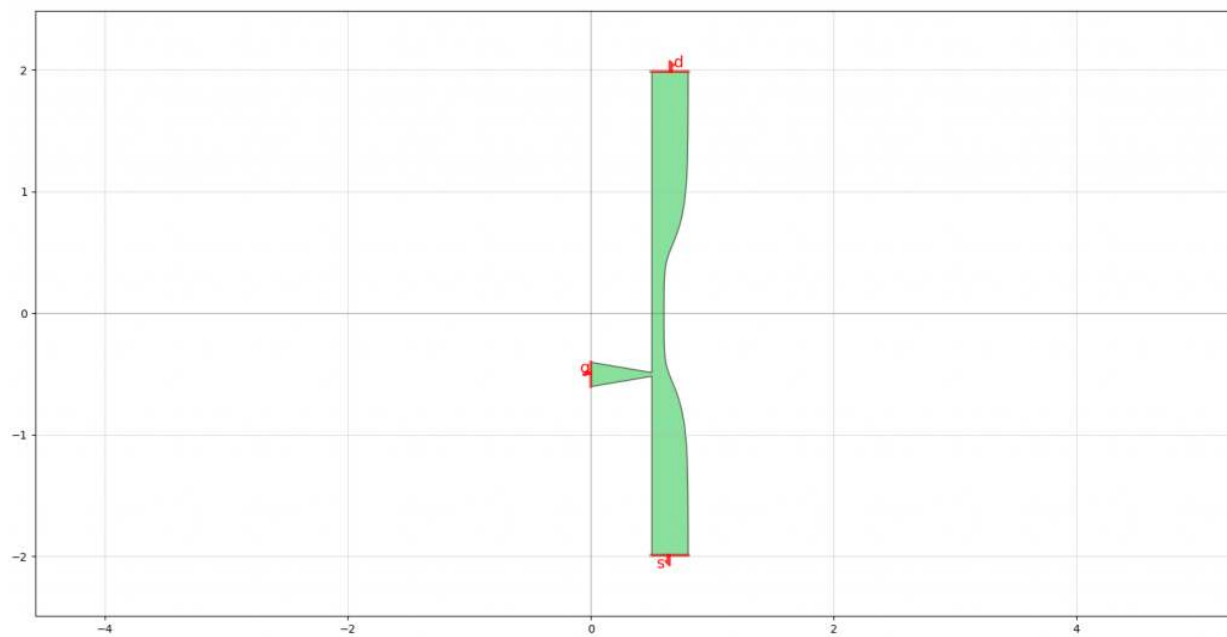
Phidl components



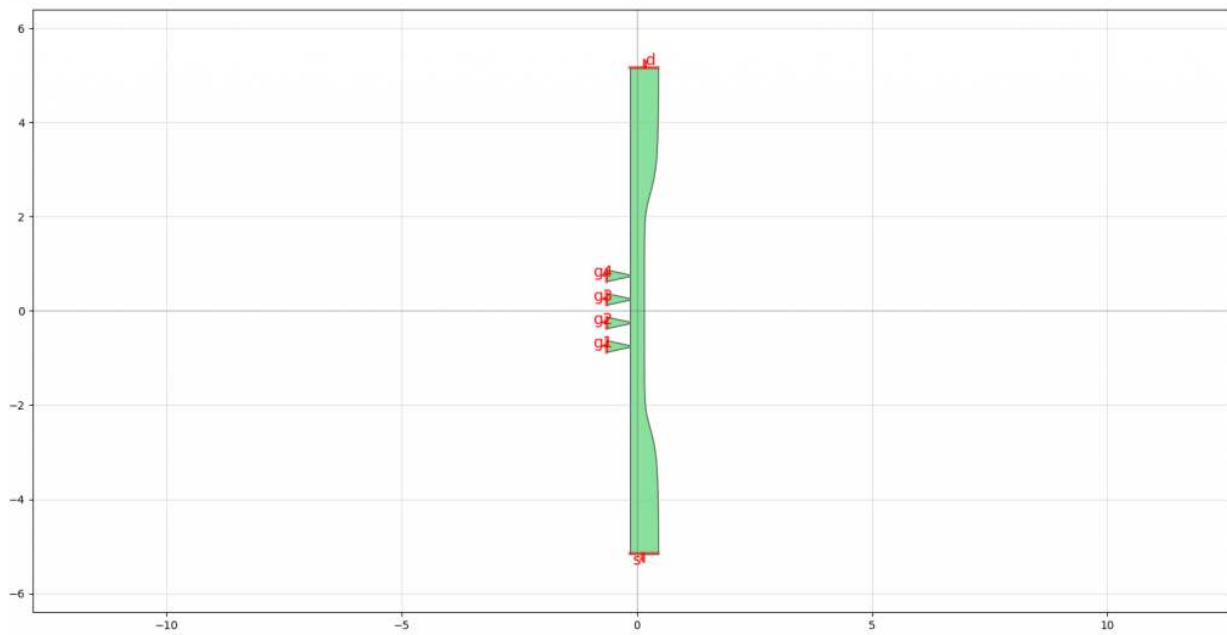
nTron. Optimal choke



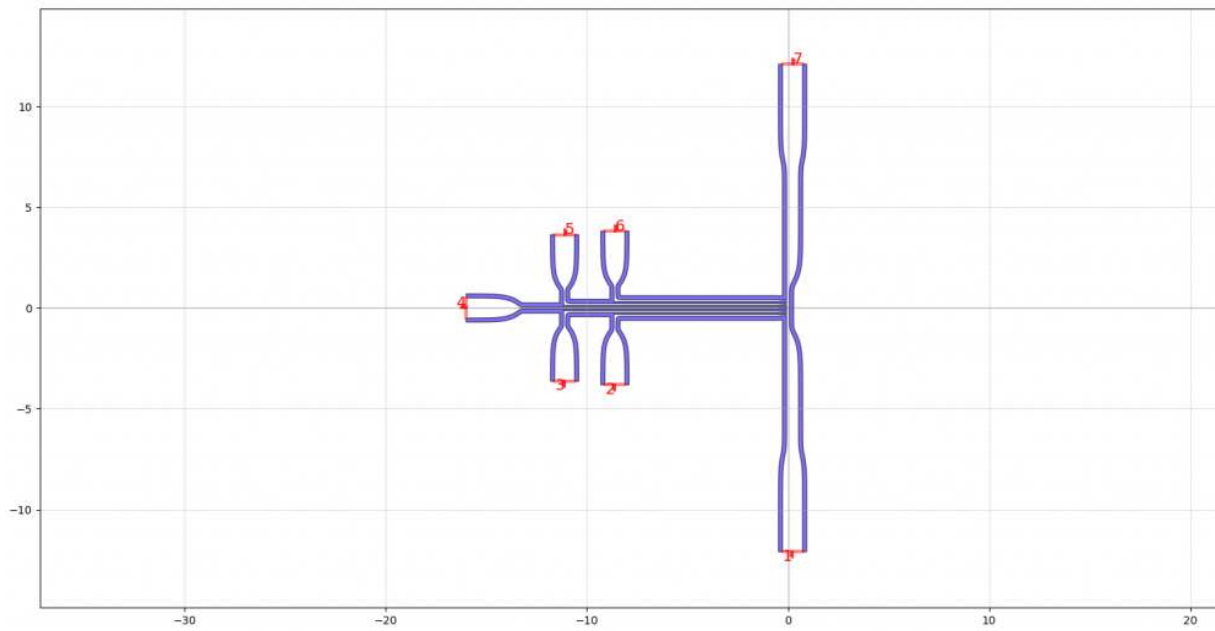
nTron. Straight taper choke



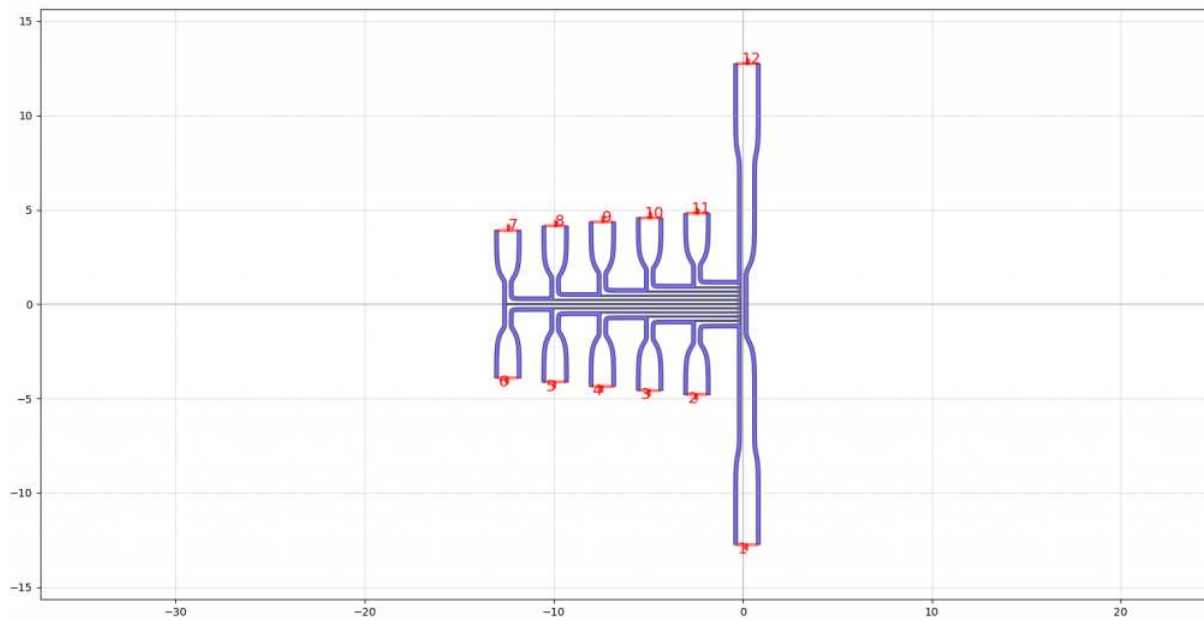
shift choke



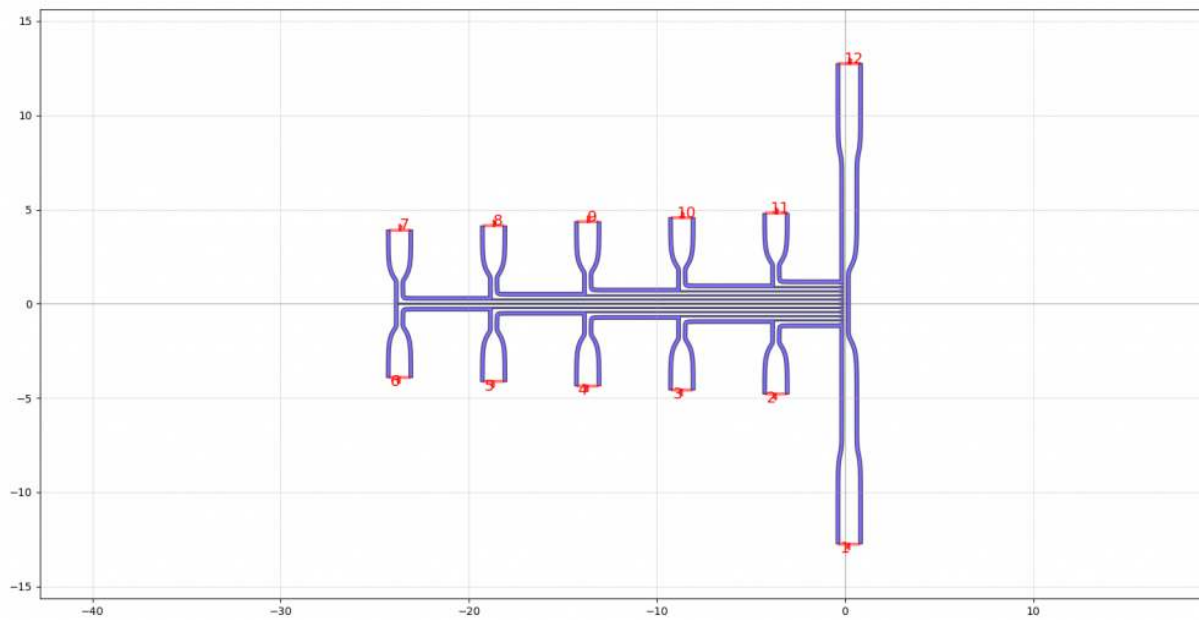
multi gate nTron



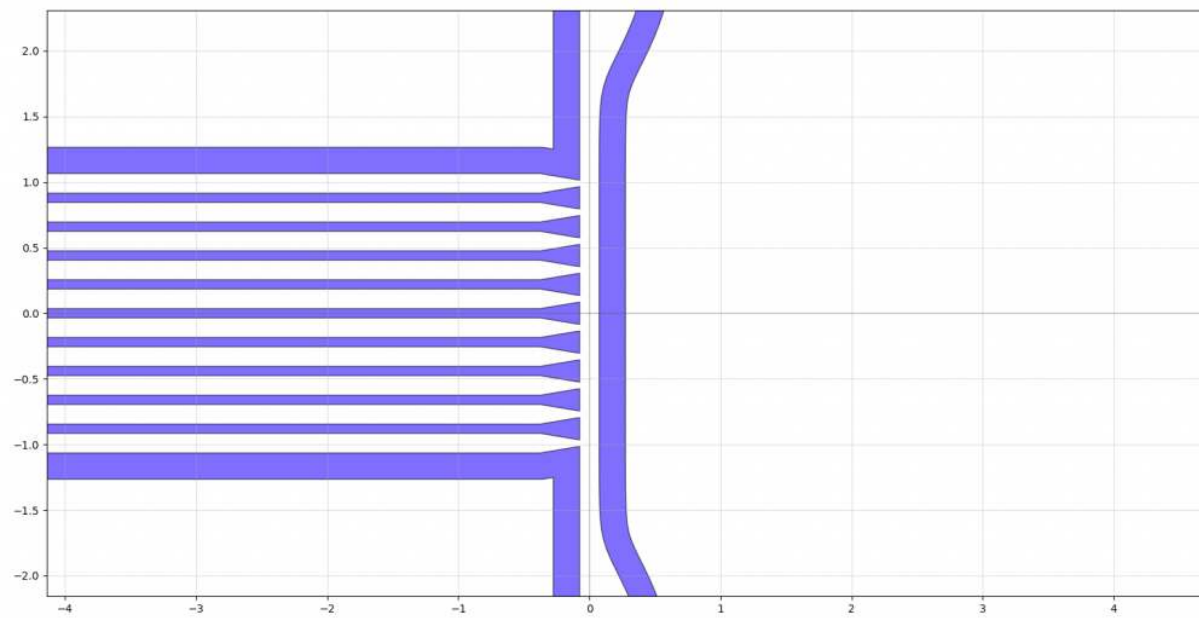
Positive tone 5-gate nTron with fanout



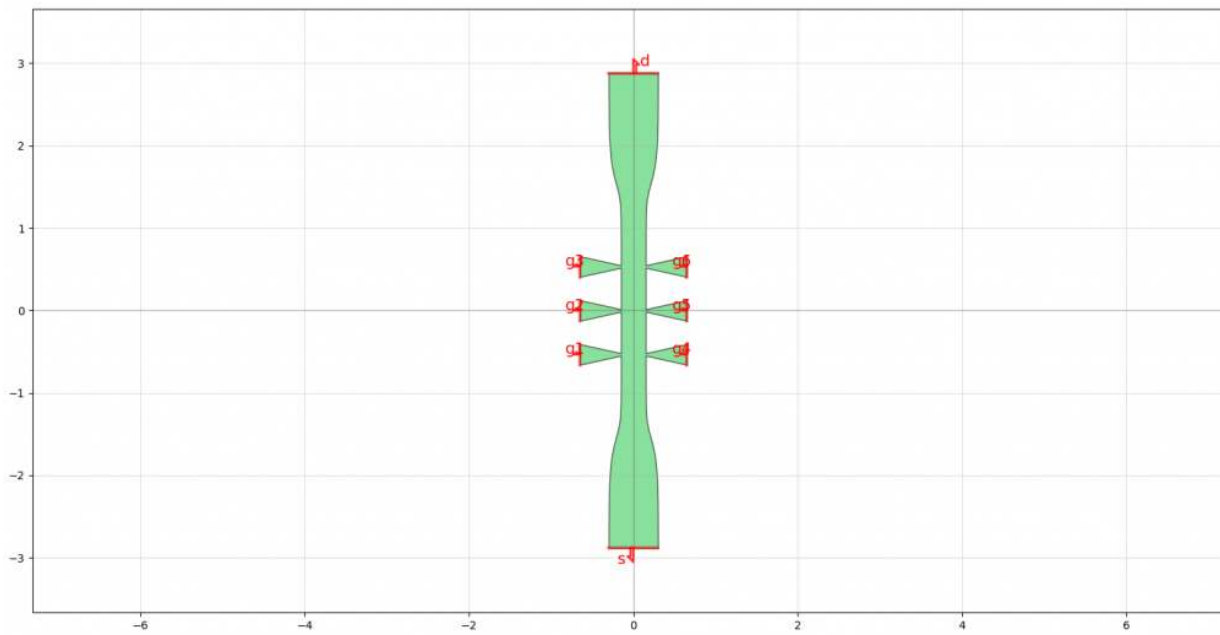
nTron fanout can support any number of evenly-spaced identical gates. Here are 10 gates.



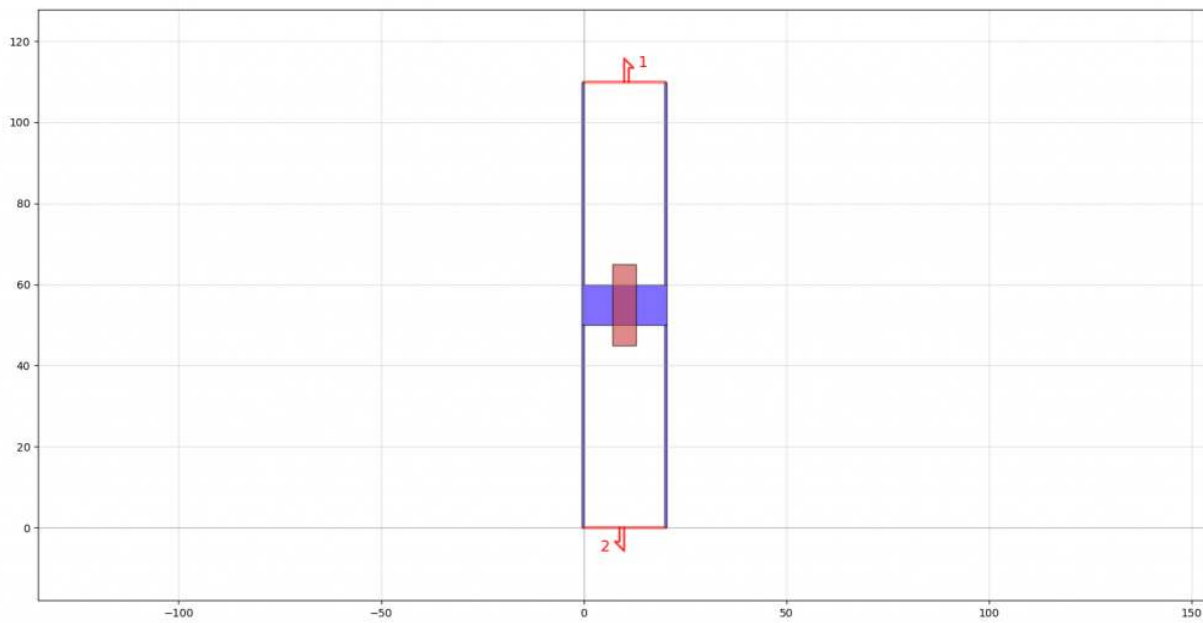
Spacing between gates can be increased using `gate_factor`



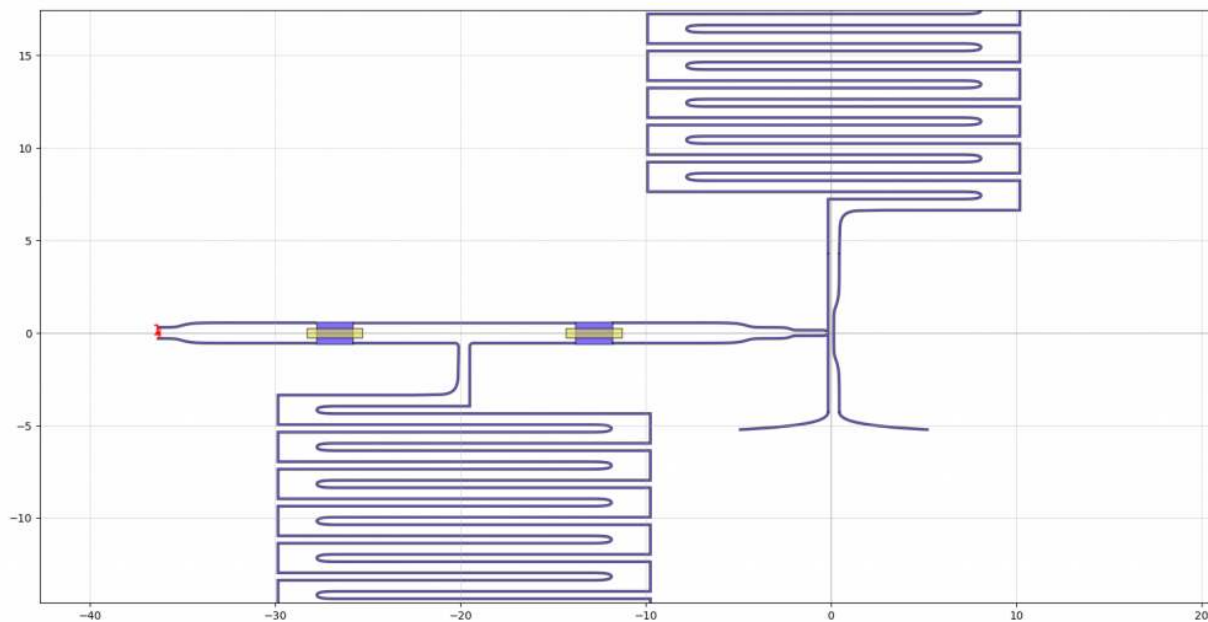
Zoom in on gates.



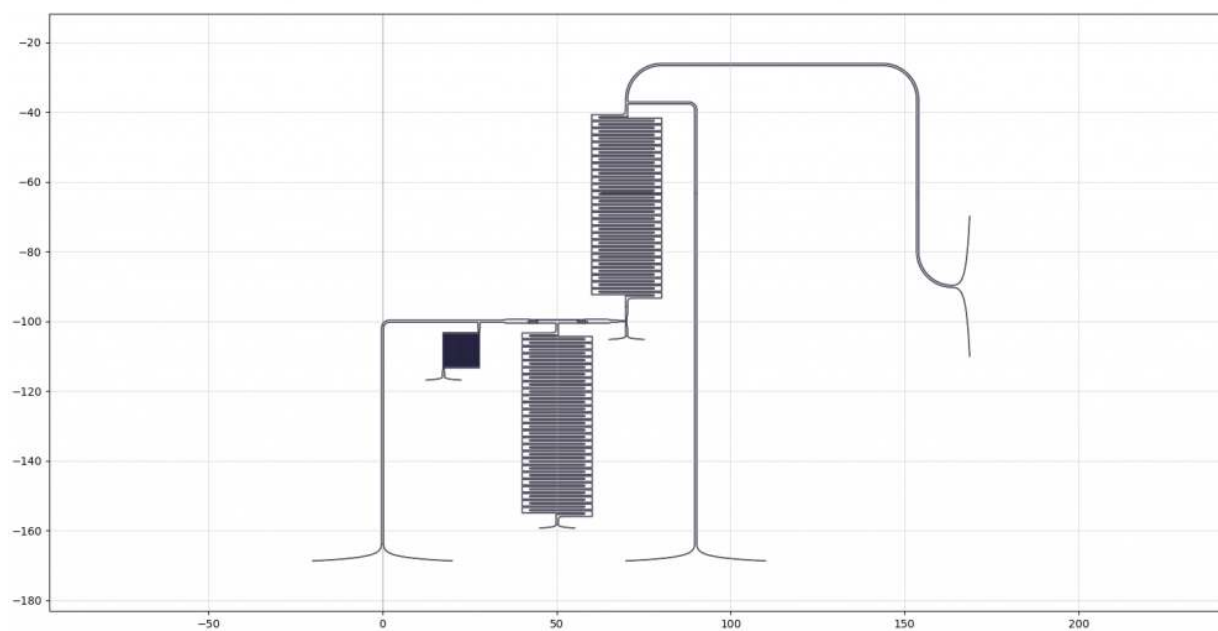
Double sided gate.



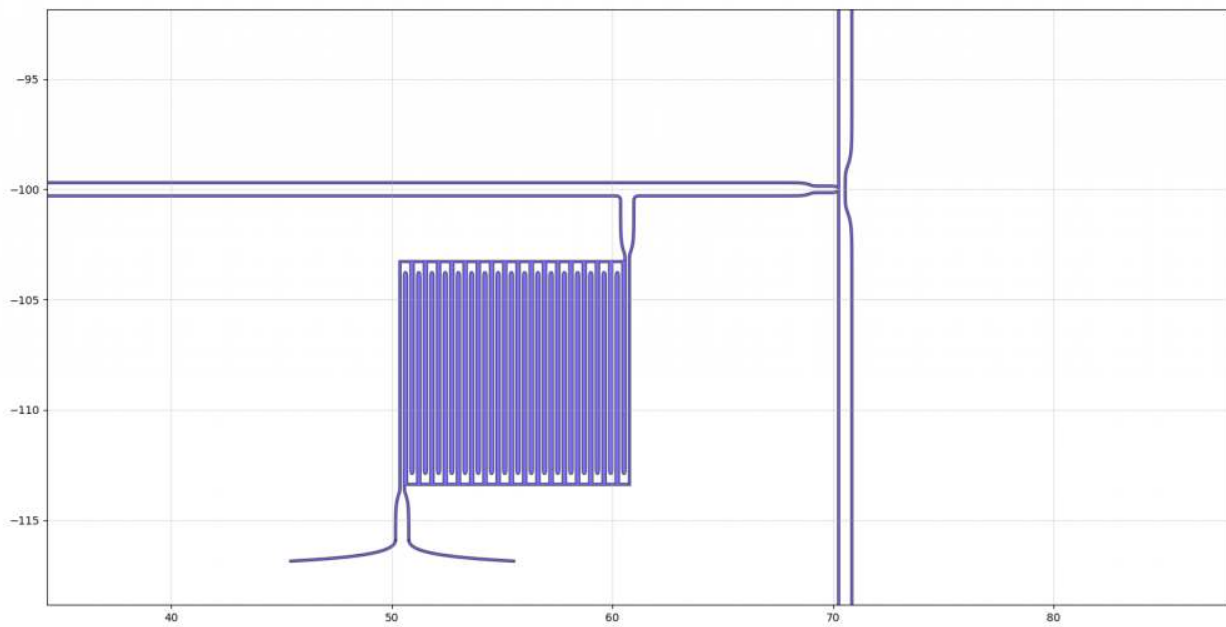
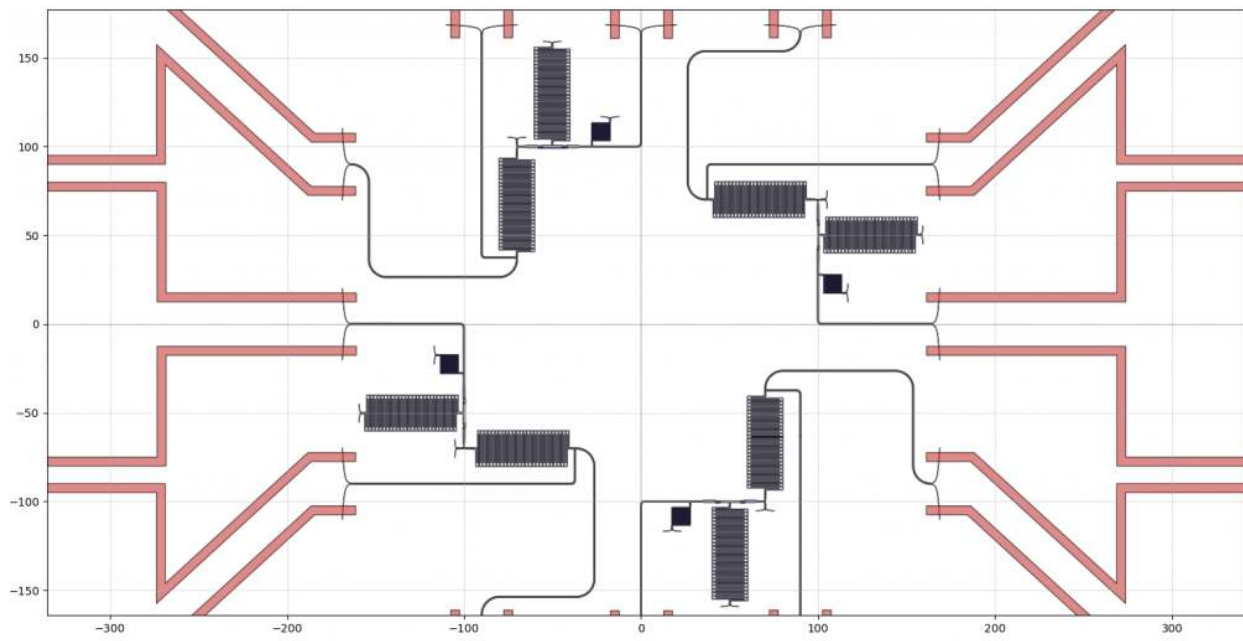
Resistor

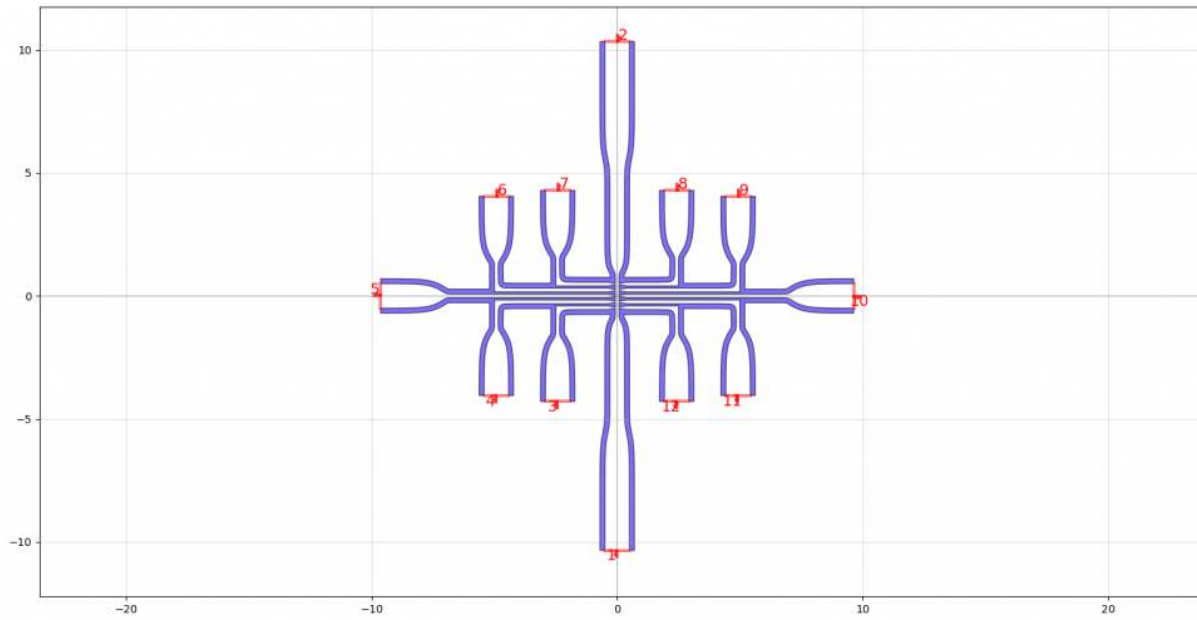


nTron amplifier with "high pass filter"



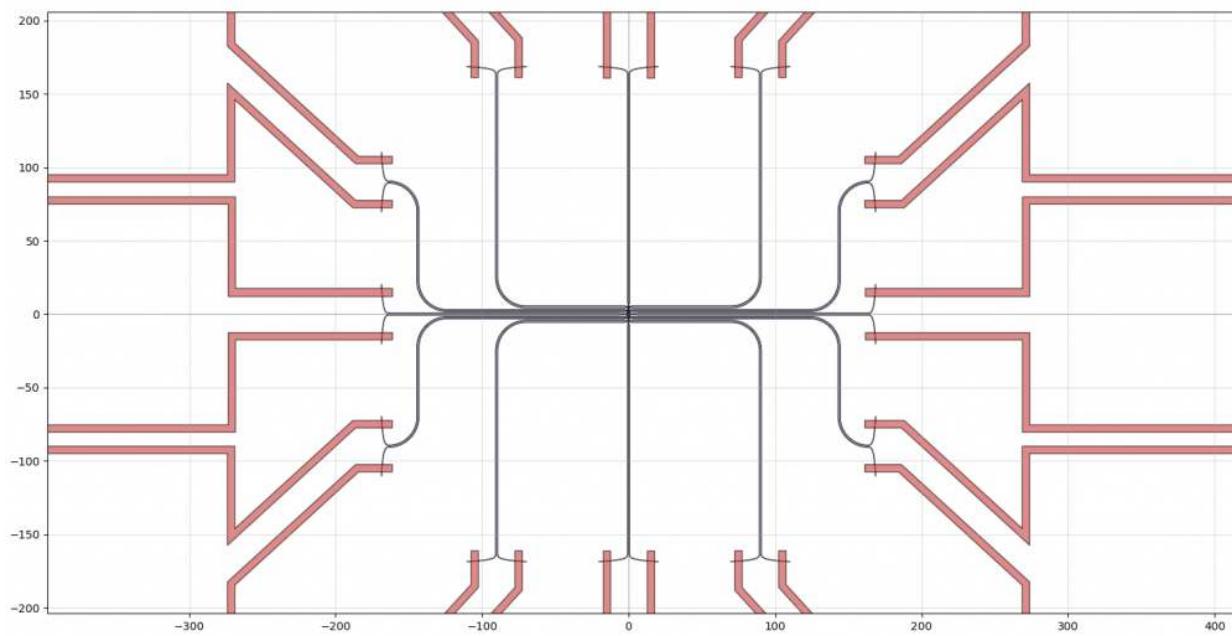
Amplifier with snspd attached.

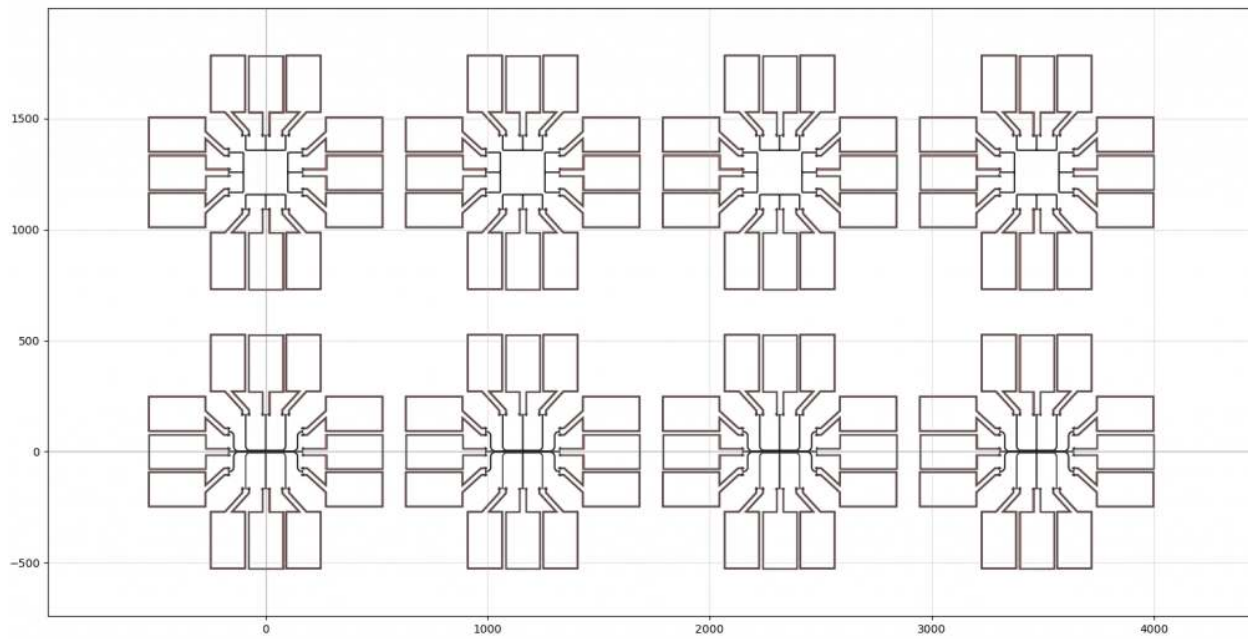




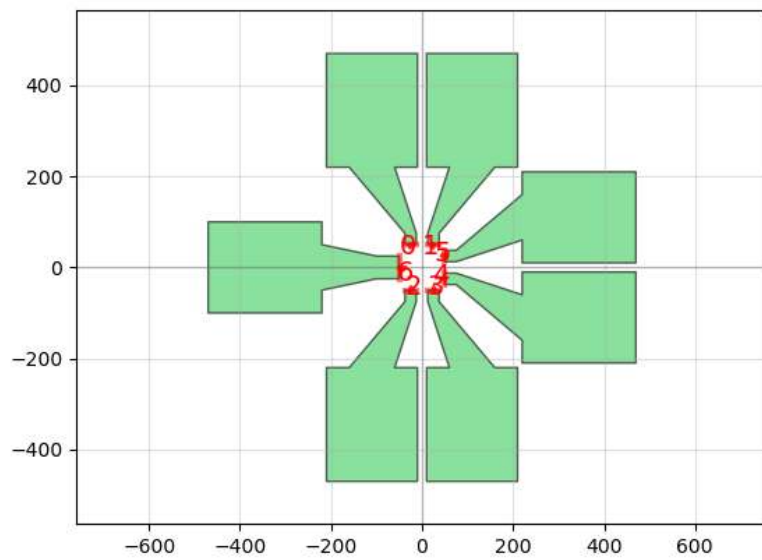
Encoder fanout

Chip Level

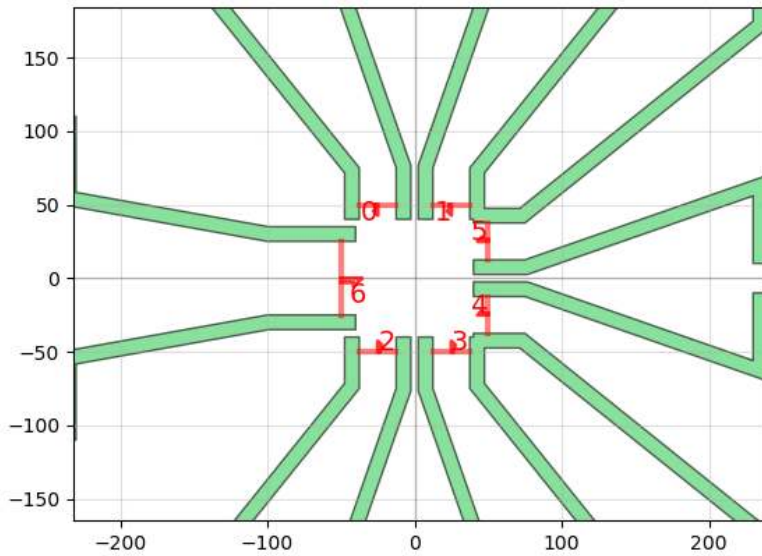
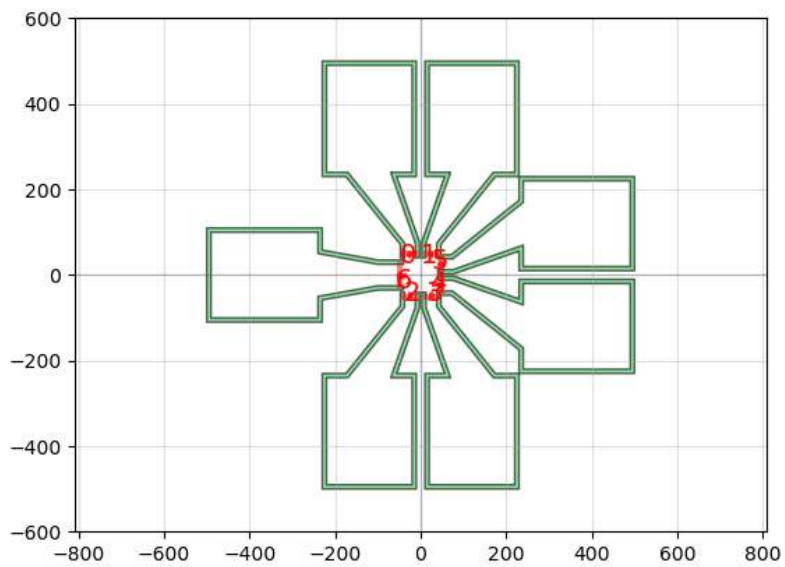




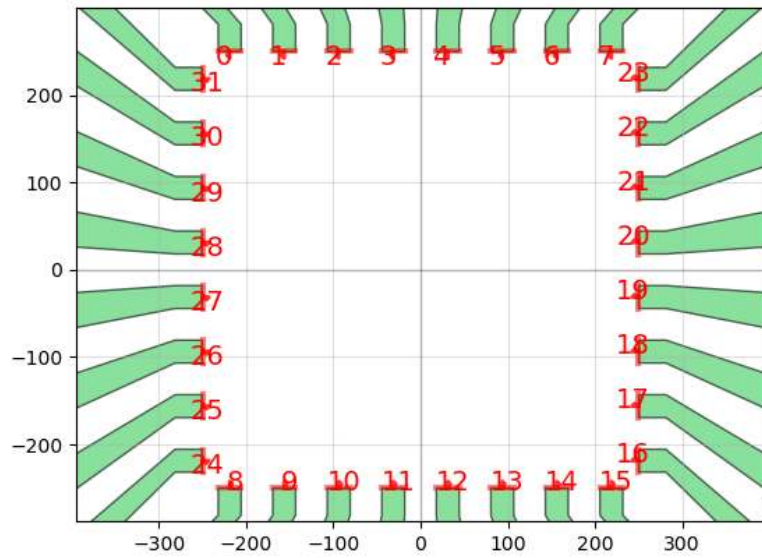
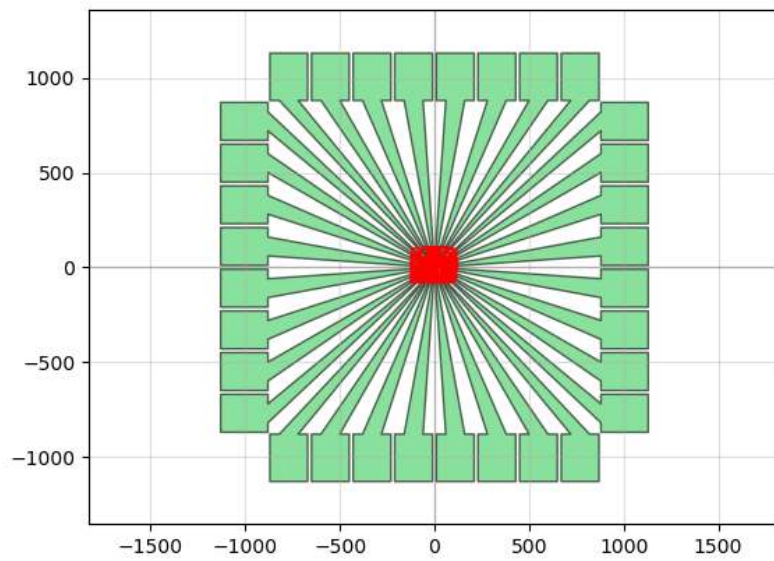
pad_array(7)



pad_array(7, outline=10)



pad_array(32)



ICE PCB with DC lines

December 21, 2020

Categories: Cryostat, Lab, SNSPD, Superconductivity

Designing a new PCB for the ICE that will have both RF and DC connections.

Board thickness of 1.6mm implies core thickness of 1.2mm.

Finished Board Thickness	Core Thickness	Copper thickness
0.6mm	0.2mm	18µm/18µm; 35µm/35µm
0.8mm	0.5mm	18µm/18µm; 35µm/35µm
1.0mm	0.8mm	18µm/18µm; 35µm/35µm; 70µm/70µm;
1.2mm	1.0mm	18µm/18µm; 35µm/35µm; 70µm/70µm;
1.6mm	1.2mm	18µm/18µm; 35µm/35µm; 70µm/70µm;
2.0mm	1.6mm	18µm/18µm; 35µm/35µm; 70µm/70µm;
2.4mm	2.0mm	18µm/18µm; 35µm/35µm; 70µm/70µm;

https://www.pcbway.com/pcb_prototype/Cost_cores_Foil___Prepreg_for_PCBs.html

For a 4 layer board the thickness between the top layer and the core is much thinner. $h=0.11\text{mm}$.

Last updated: October 2020

4-layer PCB standard stackup

Thickness	Copper thick (outer/inner)	Layer No.	StackUp	Laminated chart Thickness
1.6mm±10%	1/1oz	L1		Copper 18 um--plating to 35um
				PP 0.11 mm dielectric constant 4.29
		L2		Core 1.2mm with 1/1 oz Cu
		L3		PP 0.11 mm dielectric constant 4.29
1.6mm±10%	2/1oz	L4		Copper 18 um--plating to 35um
		L1		Copper 50um(±5)um-plating to 70um
				PP 0.11 mm dielectric constant 4.29
		L2		Core 1.2mm with 1/1 oz Cu
1.6mm±10%	2/1.5oz	L3		PP 0.11 mm dielectric constant 4.29
		L4		Copper 50um(±5)um-plating to 70um
		L1		Copper 50um(±5)um-plating to 70um
				PP 0.22 mm dielectric constant 4.29
1.6mm±10%	2/1.5oz	L2		Core 1mm with 1.5/1.5 oz Cu
		L3		PP 0.22 mm dielectric constant 4.29
		L4		Copper 50um(±5)um-plating to 70um

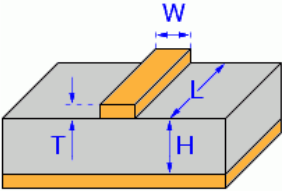
For Reference only, Ended up using a two layer board <https://www.pcbway.com/multi-layer-laminated-structure.html>

PCB Calculator

Regulators Track Width Electrical Spacing TransLine RF Attenuators Color Code Board Classes

Transmission Line Type:

- ☒ Microstrip Line
- ☐ Coplanar wave guide
- ☐ Coplanar wave guide with ground plane
- ☐ Rectangular Waveguide
- ☐ Coaxial Line
- ☐ Coupled Microstrip Line
- ☐ Stripline
- ☐ Twisted Pair



Substrate Parameters:

Er:	4.5	...
TanD:	0.02	...
Rho:	1.72e-08	...
H:	.8	mm
H _t :	1e+20	mm
T:	0.035	mm
Rough:	0	mm
mu Rel S:	1	
mu Rel C:	1	

Physical Parameters:

W:	1.45	mm
L:	0	mm

Analyze Synthesize

Electrical Parameters:

Z0:	50.4714	Ω
Ang. I:	0	Radian

Results:

ErEff: 3.3301
 Conductor Losses: 0 dB
 Dielectric Losses: 0 dB
 Skin Depth: 1.47594 μm

Component Parameters:

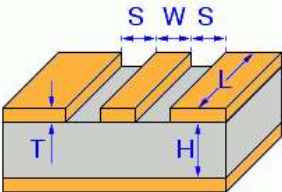
Frequency: 2 GHz

PCB Calculator

Regulators Track Width Electrical Spacing TransLine RF Attenuators Color Code Board Classes

Transmission Line Type:

- ☐ Microstrip Line
- ☐ Coplanar wave guide
- ☒ Coplanar wave guide with ground plane
- ☐ Rectangular Waveguide
- ☐ Coaxial Line
- ☐ Coupled Microstrip Line
- ☐ Stripline
- ☐ Twisted Pair



Substrate Parameters:

Er:	4.5	...
TanD:	0.02	...
Rho:	1.72e-08	...
H:	.8	mm
T:	.035	mm
mu Rel C:	1	

Physical Parameters:

W:	1.3	mm
S:	0.608018	mm
L:	0	mm

Analyze Synthesize

Electrical Parameters:

Z0:	50	Ω
Ang. I:	0	Radian

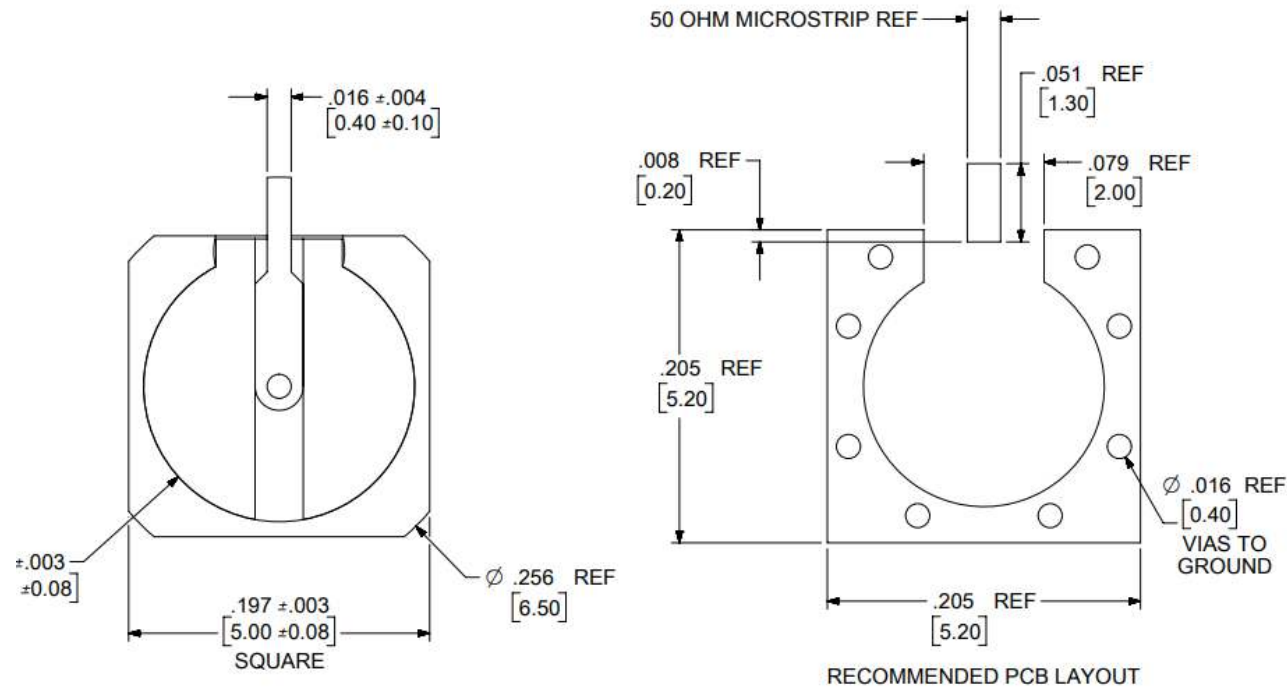
Results:

ErEff: 3.03478
 Conductor Losses: 0 dB
 Dielectric Losses: 0 dB
 Skin Depth: 2.0873 μm

Component Parameters:

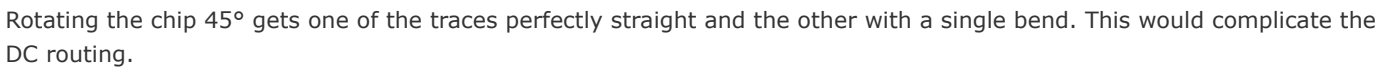
Frequency: 1 GHz

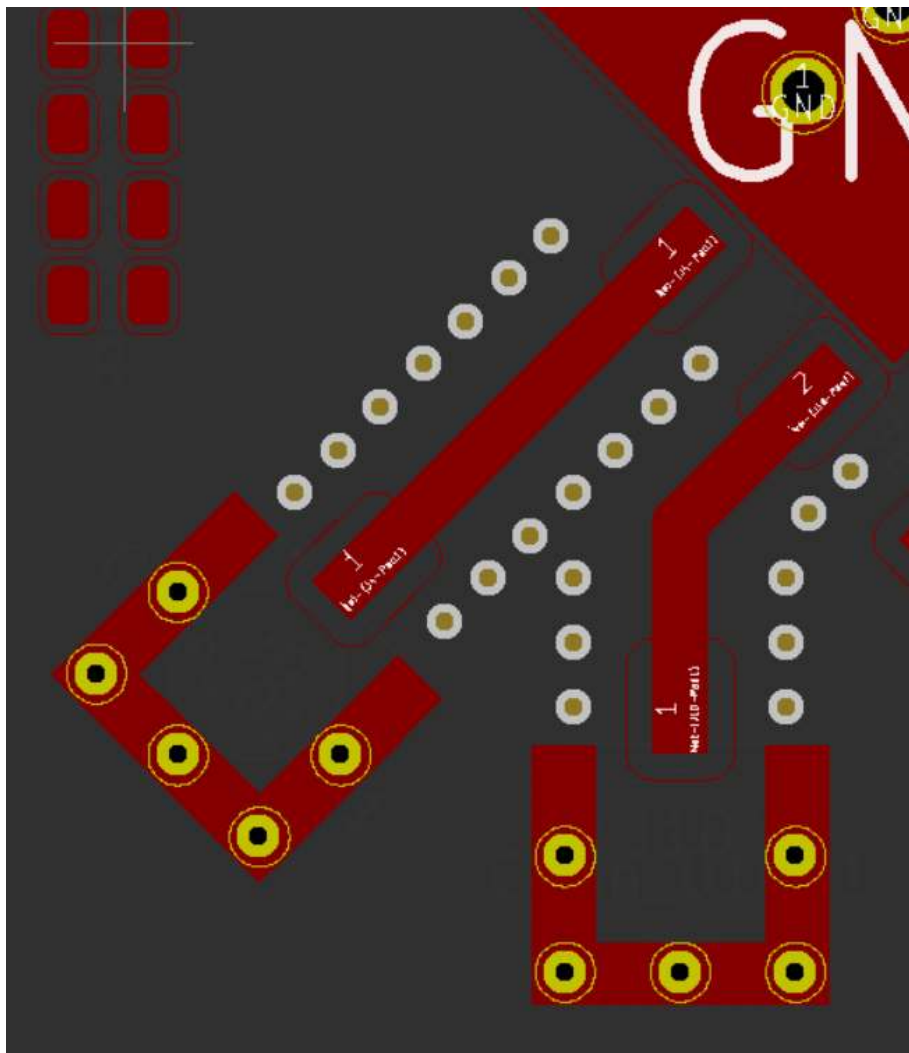
Needs to be a 1mm thick FR4 board (core .8mm)



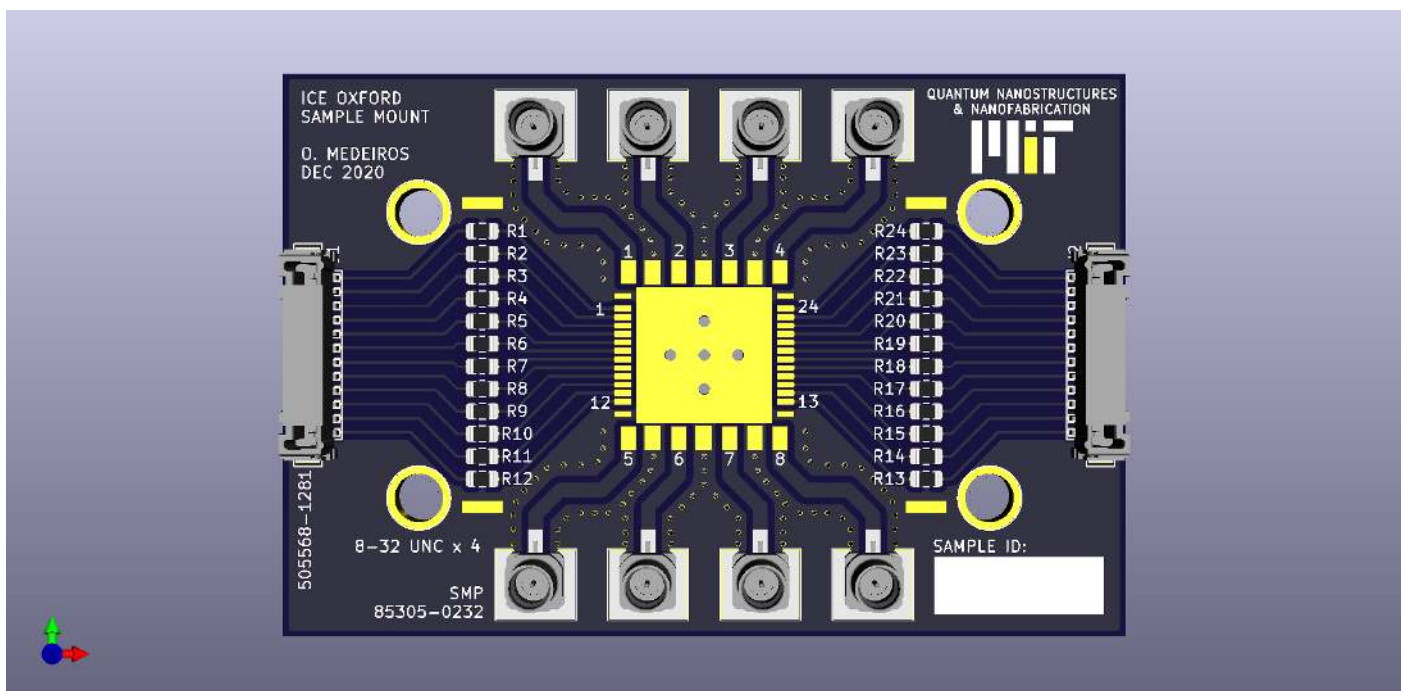
K PER CARTON
K PER CARTON
K PER CARTON
00 PER CARTON
K PER CARTON

THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO MOLEX ELECTRONIC TECHNOLOGIES, LLC AND SHOULD NOT BE USED WITHOUT WRITTEN PERMISSION									
DIMENSION UNITS		SCALE		CURRENT REV DESC:					
INCH/MM		NTS		molex					
GENERAL TOLERANCES (UNLESS SPECIFIED)									
ANGULAR TOL		± 2.0°		SMP, PLUG SMT					
4 PLACES	±			EC NO: 638738		LIMITED DETENT SMP-P/PCB, EWR-11818			
				DRWN: RYEH		2020/05/29			
3 PLACES	±			CHK'D: YCHENG		2020/07/08			
2 PLACES	±	0.25		APPR: YCHENG		2020/07/08			
				PRODUCT CUSTOMER DRAWING					
1 PLACE		±		INITIAL REVISION:		DOCUMENT NUMBER			
0 PLACES		±		DRWN: AROBERTSON		2005/07/29		DOC TYPE	
				APPR: JWIENER		2005/08/01		DOC PART	
DRAFT WHERE APPLICABLE				THIRD ANGLE PROJECTION		DRAWING		REVISION	
								SD-85305-0232	
								PSD	
								001	
								B15	
								MATERIAL NUMBER	
								CUSTOMER	
								SHEET NUMBER	

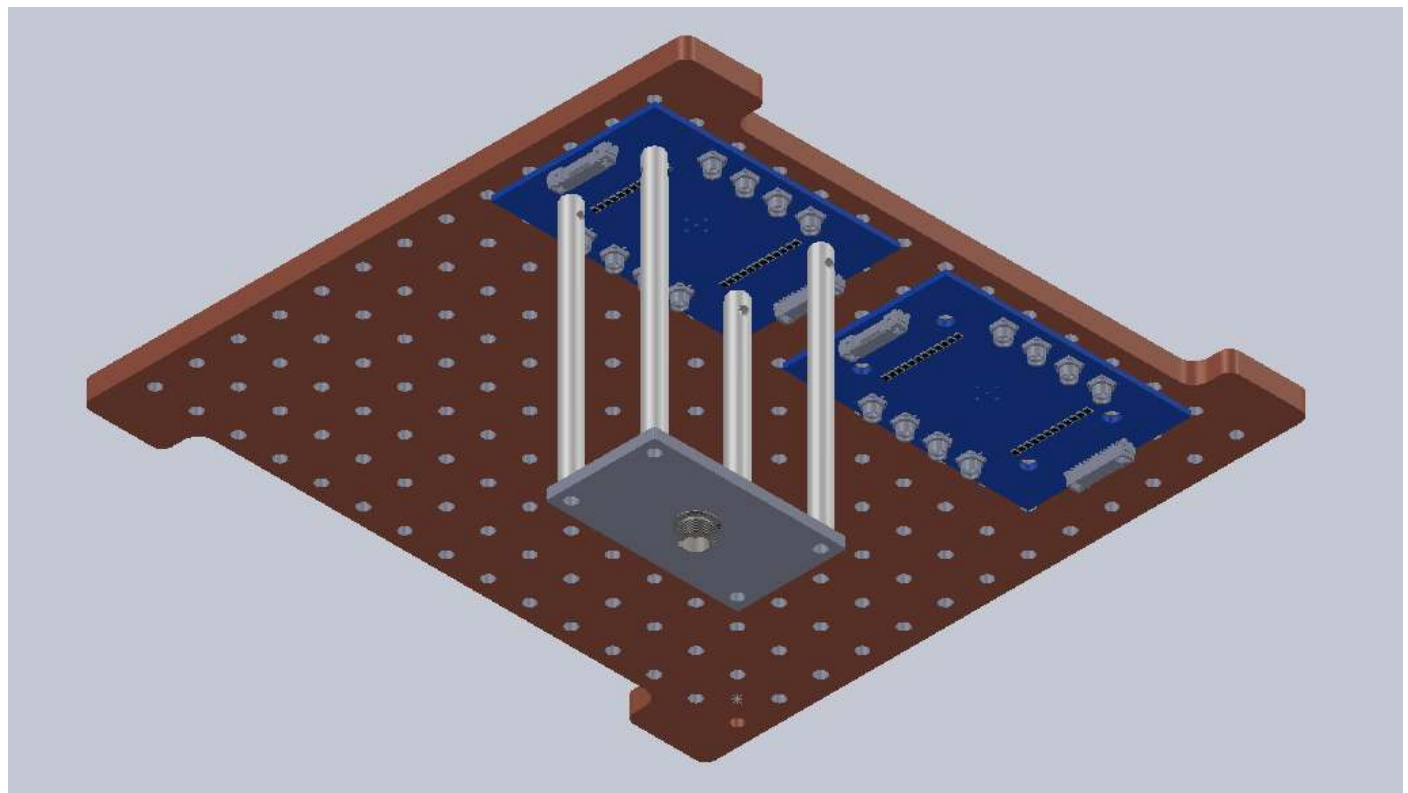
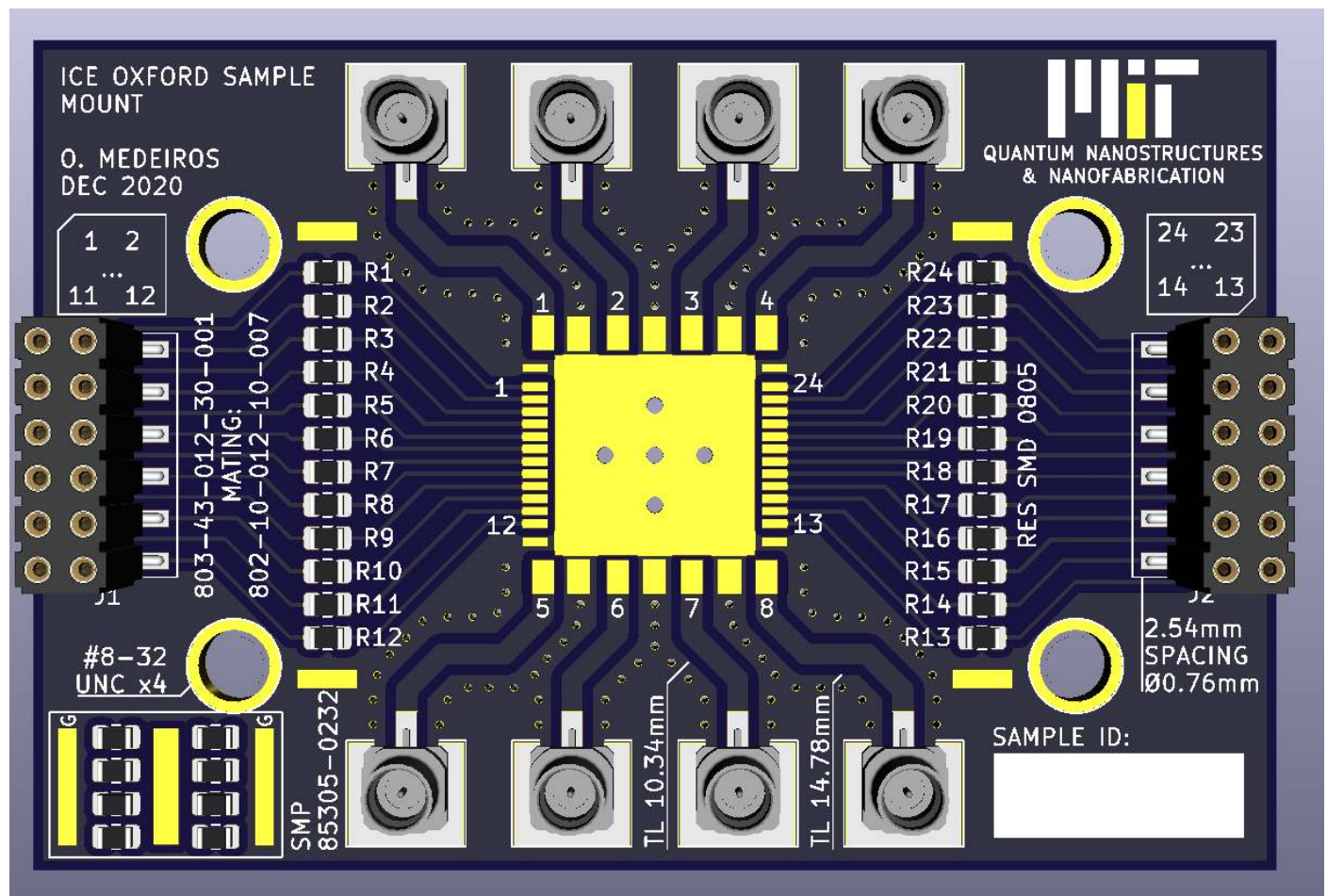


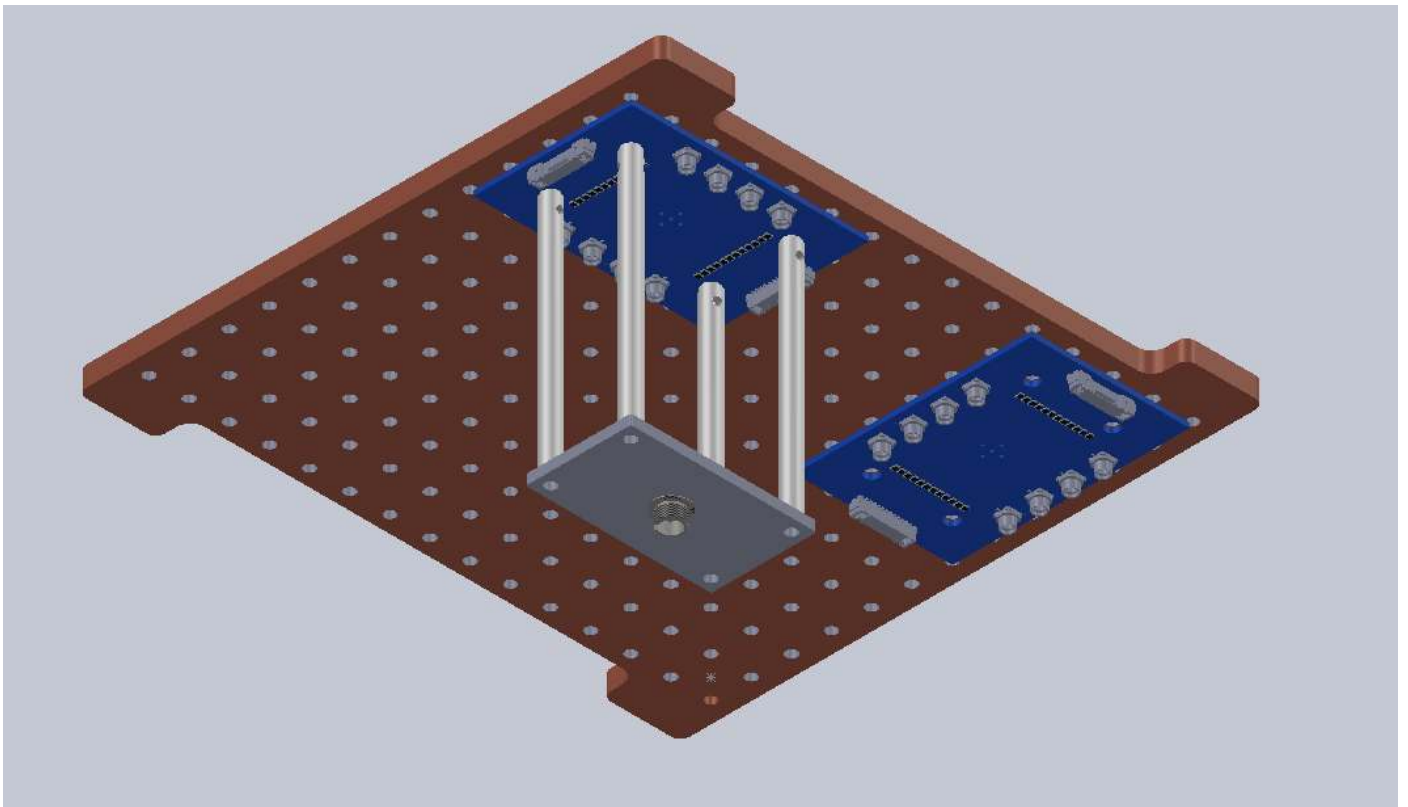


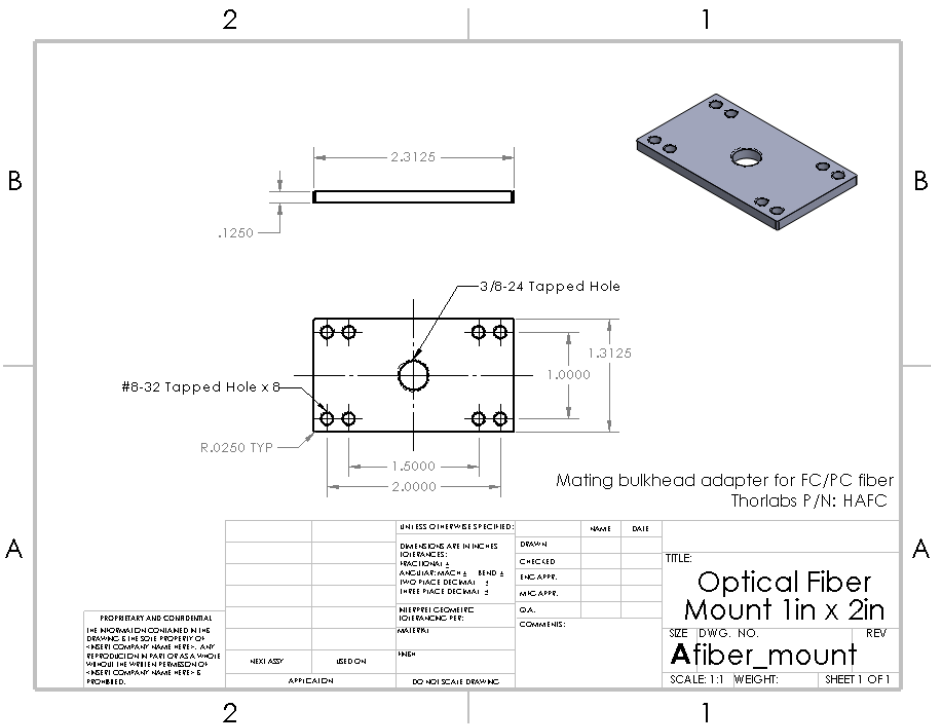
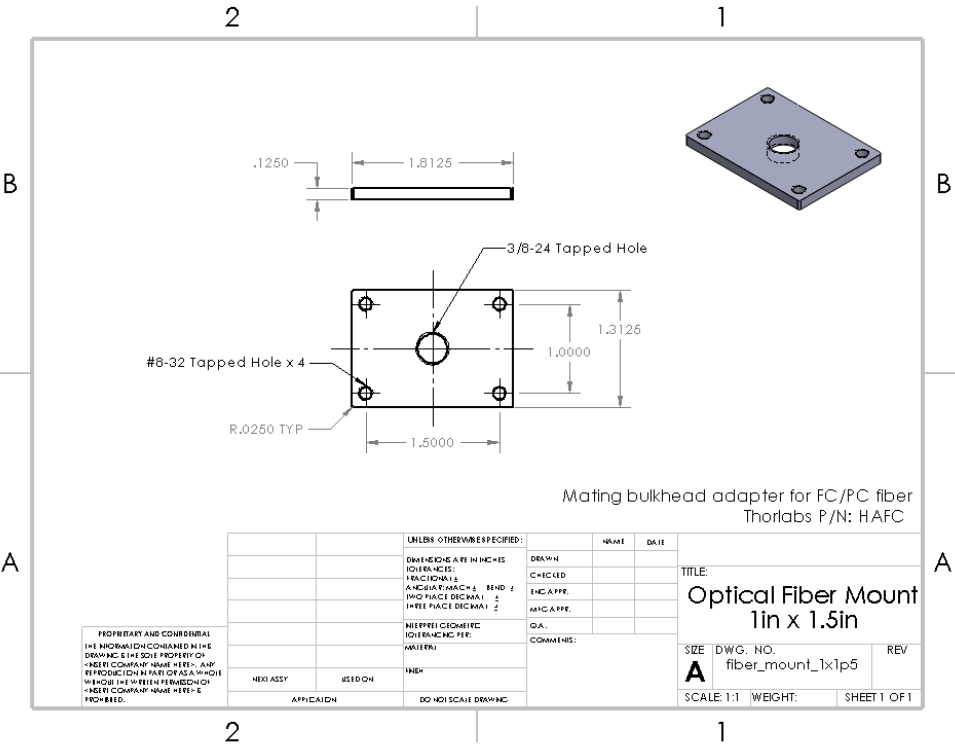
RF traces are 1.3mm wide with a space of .608mm of either side. Board is 1mm (0.8mm core) thick.



If we want to use machined connectors we could use these Mill-Max headers and use the soldercup configuration of the mating connector.







Parameter Information :

Board type :	Single pieces	Panel Way :	
Different Design in Panel:	1	X-out Allowance in Panel :	
Size :	75 x 50 mm	Quantity :	10
Layer :	2 Layers	Material :	FR-4: TG130
Thickness :	1 mm	Min Track/Spacing :	6/6mil
Min Hole Size :	0.3mm ↑	Solder Mask :	Blue
Silkscreen :	White	Gold fingers :	No
Surface Finish :	Immersion gold(ENIG) (2U")	"HASL" to "ENIG"	No
Via Process :	Tenting vias	Finished Copper :	1 oz Cu
Extra pcb product number :	Not to add extra pcb product number on board (extra+\$3)	Additional Options :	UL Marking:None,
PO No. :		Manufacturing :	
			Total: US \$82.00

Via process is ignored

HAFCFC/PC Bulkhead Adapter, Wide Key (2.2 mm)

MS3R Mini-Series Optical Post, Ø6 mm, L = 3"

HAFC2 – FC/PC Bulkhead Adapter, Narrow Key (2.0 mm)

Alternate Mill-Max Components

SMD sockets

Solder Cup pins

Cryogenic heat shrink

cryo_stage.zip Solidworks model

ice_pcb_2020.zip Kicad model

W122192ASP7_gerber_files (1).zip gerber files

Free Space Cryostat Upgrades

December 21, 2020

Categories: General

Problems

1. Electrical

1. Heater does not function
2. SMA-SMP connectors are not all suitable for cryo. Some are not long enough.
3. Rigid cables have had issues in the past, check that everything functions properly.

2. Fiber Optics

1. Replace internal fiber interconnects. The fibers are very old and potentially damaged due to years of thermal cycling. Replace existing fiber mount with the update ICE design (see [ICE PCB blog post](#)).
2. Create fiber bank feedthru

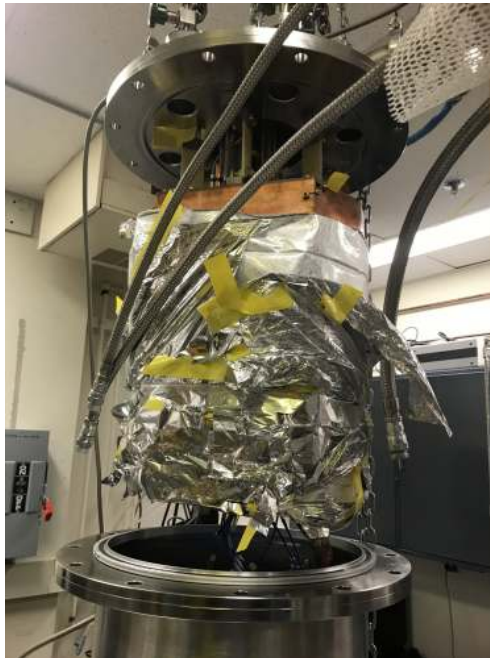
3. Thermal

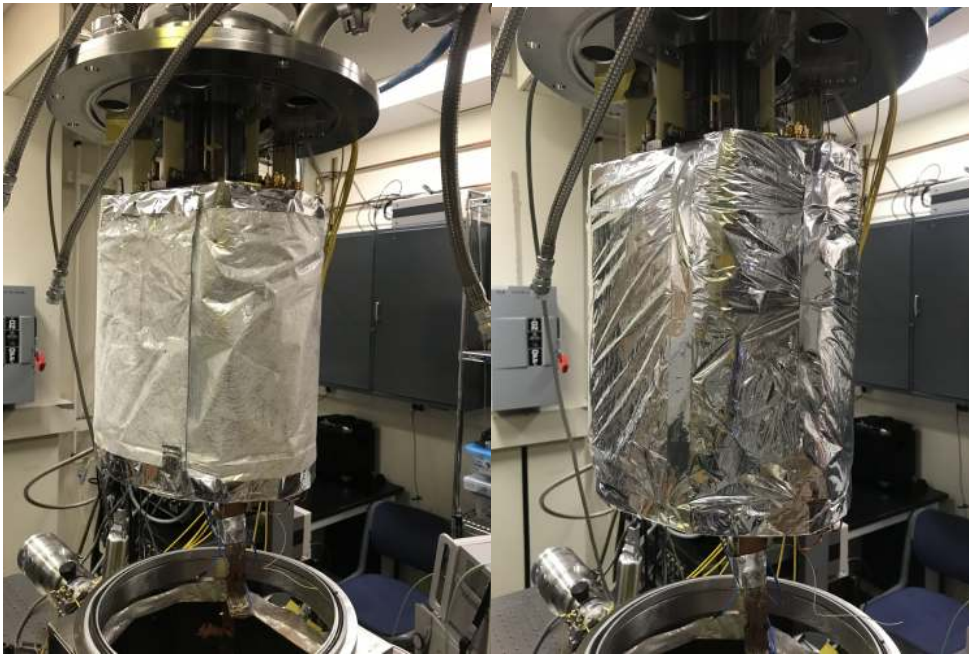
1. Rad shield could be replaced with top down mount like other cryostats. Would replace fabric and bottom mount panels. Marco C: the bottom mount was supposedly used reduce vibrations between the sample mount and the optics table (ie if the table moves, the sample stage would move with it). But there is little mechanical connection between the bottom rad shield and the top, so there is likely drift between the table and the sample mount. Top mount would make operation easier, more conventional, and better thermally isolated from the outermost shield.
2. **COOLCAT Multi-Layer Insulation RUAG**

4. Mechanical

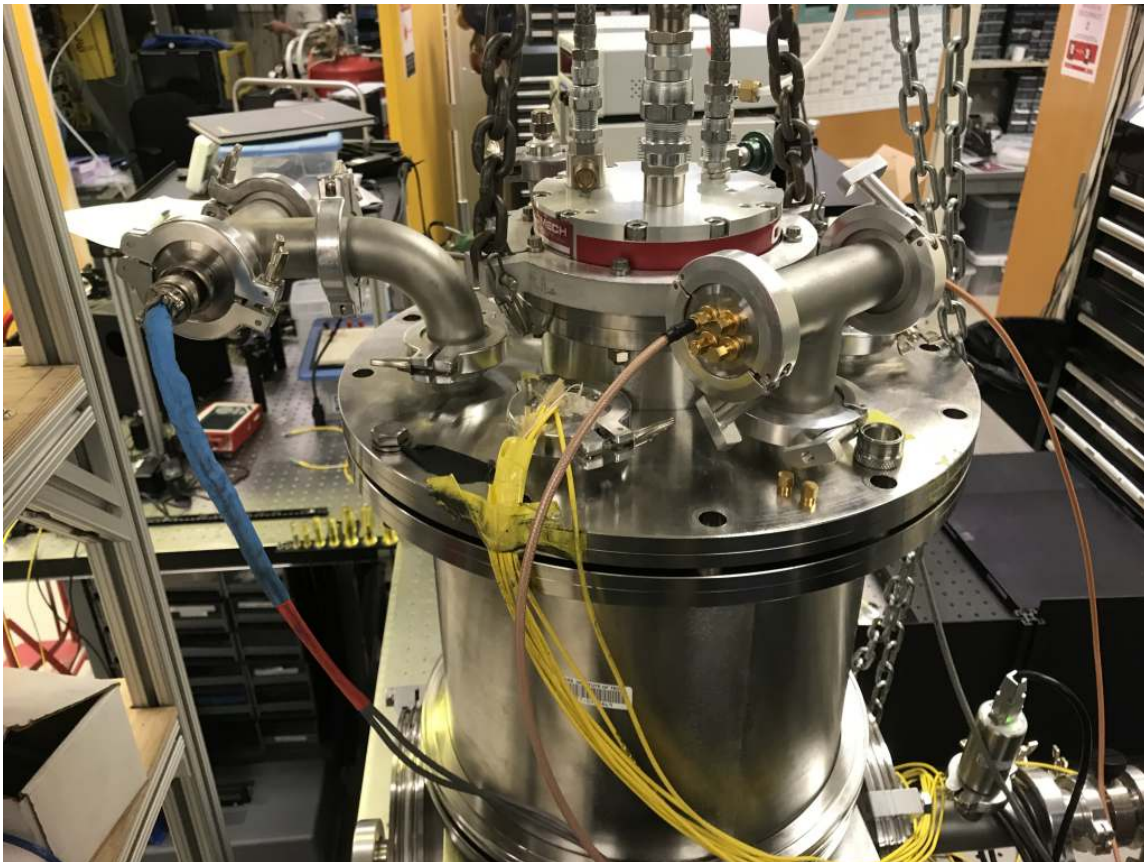
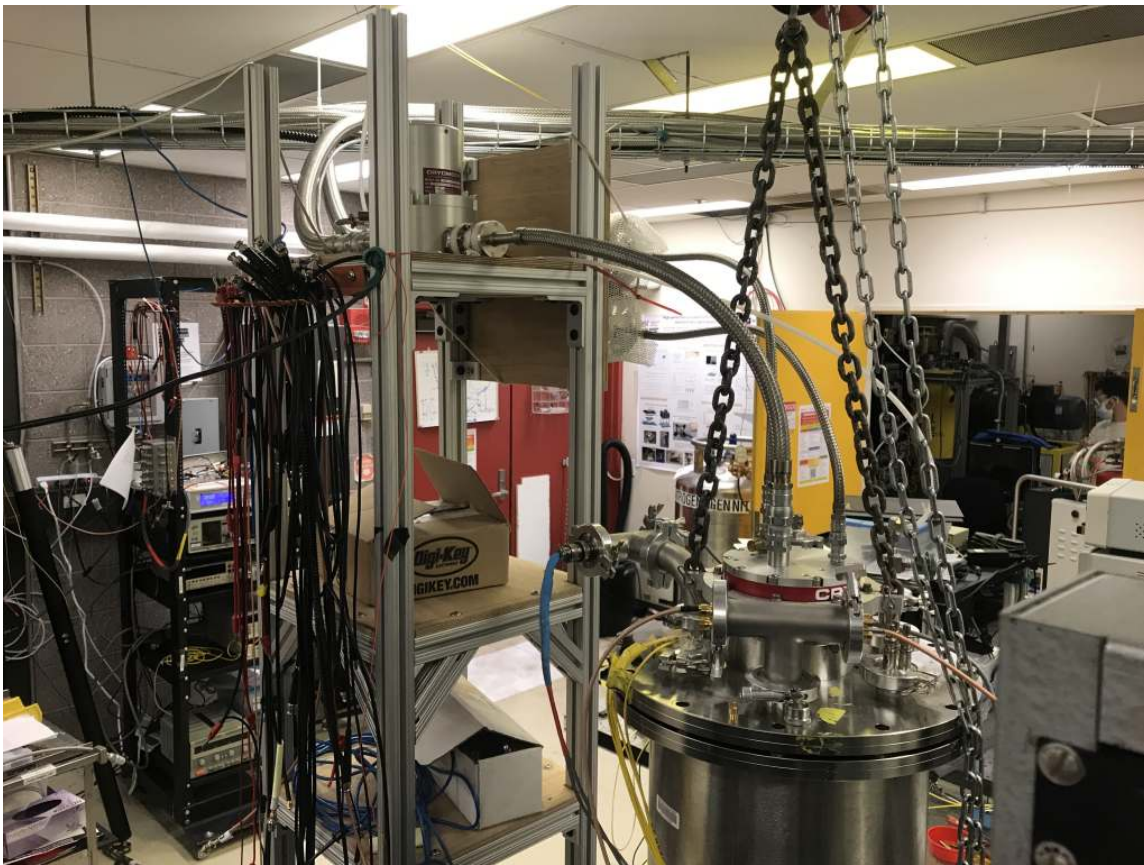
1. Pulse tube motor is in a fixed location and the lines to the cold head need to be detached everytime the cryostat is opened. Disconnecting the lines causes some helium to leak out and potentially introduces contaminants.
2. We could buy line extensions, this might be difficult to find with the correct fittings on each end. Alternatively, we could mount the pulse tube motor on an adjustable platform. The motor could be raised and lowered according to the cryostat by attaching **rollers** to the platform to the 80/20 frame then hoisted up when opening.
3. Sample stage – some holes are stripped, components are haphazardly mounted, difficult to reach. Best to redesign so that it is compatible with the ICE.
4. **No working model of internal components.**

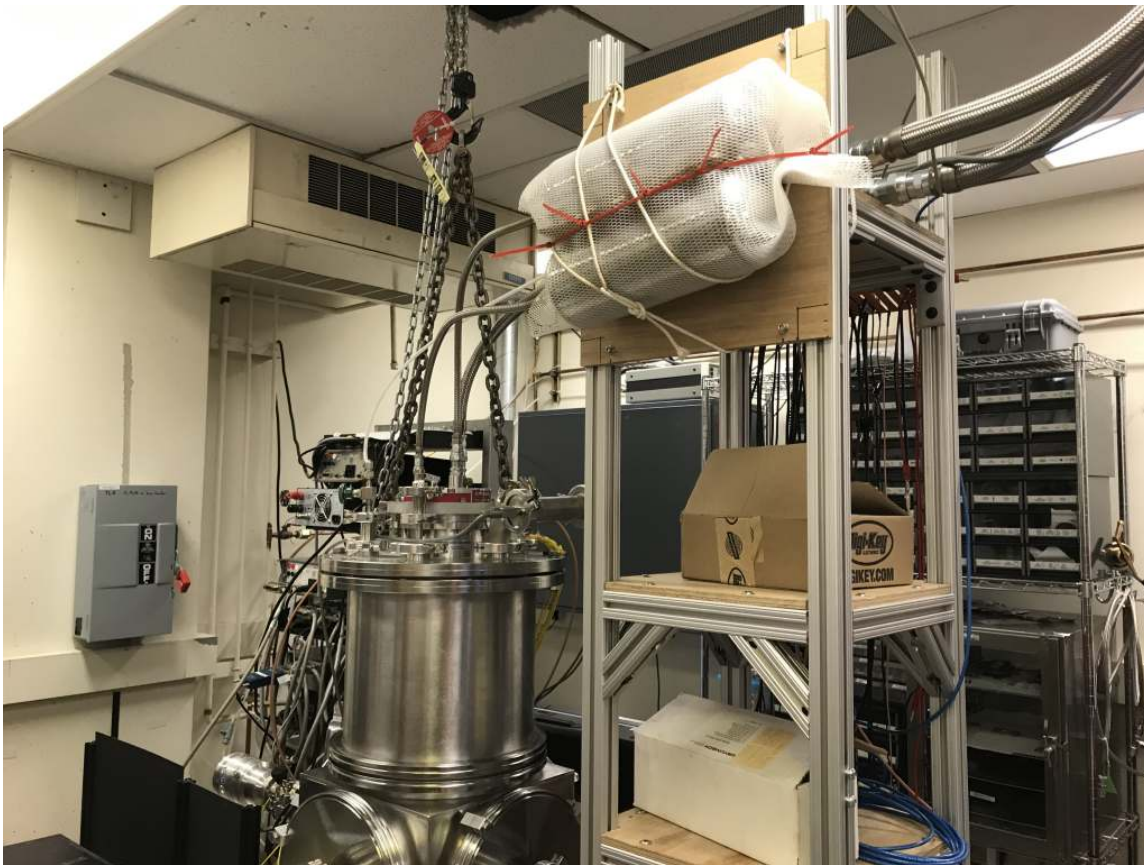
Images











Brainstorm

Appendix

[Thermal Insulation Products.pdf](#)

[ruag_thermal_insulation_quote.pdf](#)

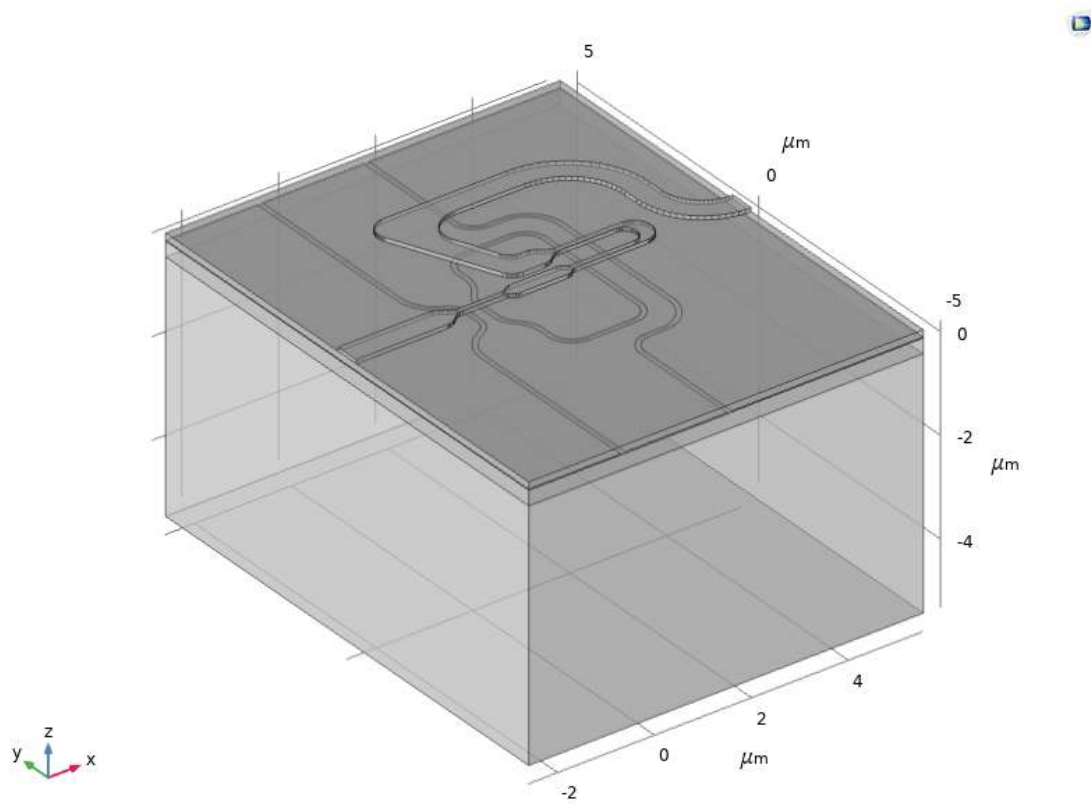
nMem Comsol Simulation

January 18, 2021

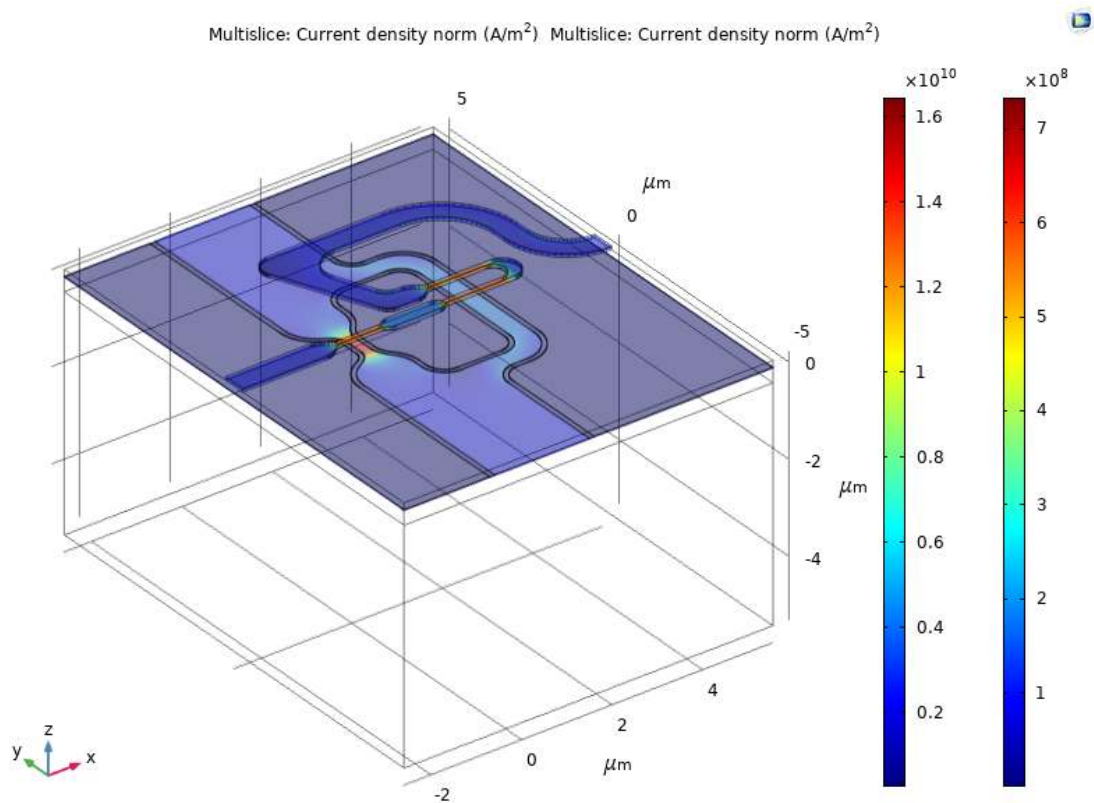
Categories: General

Tags: comsol

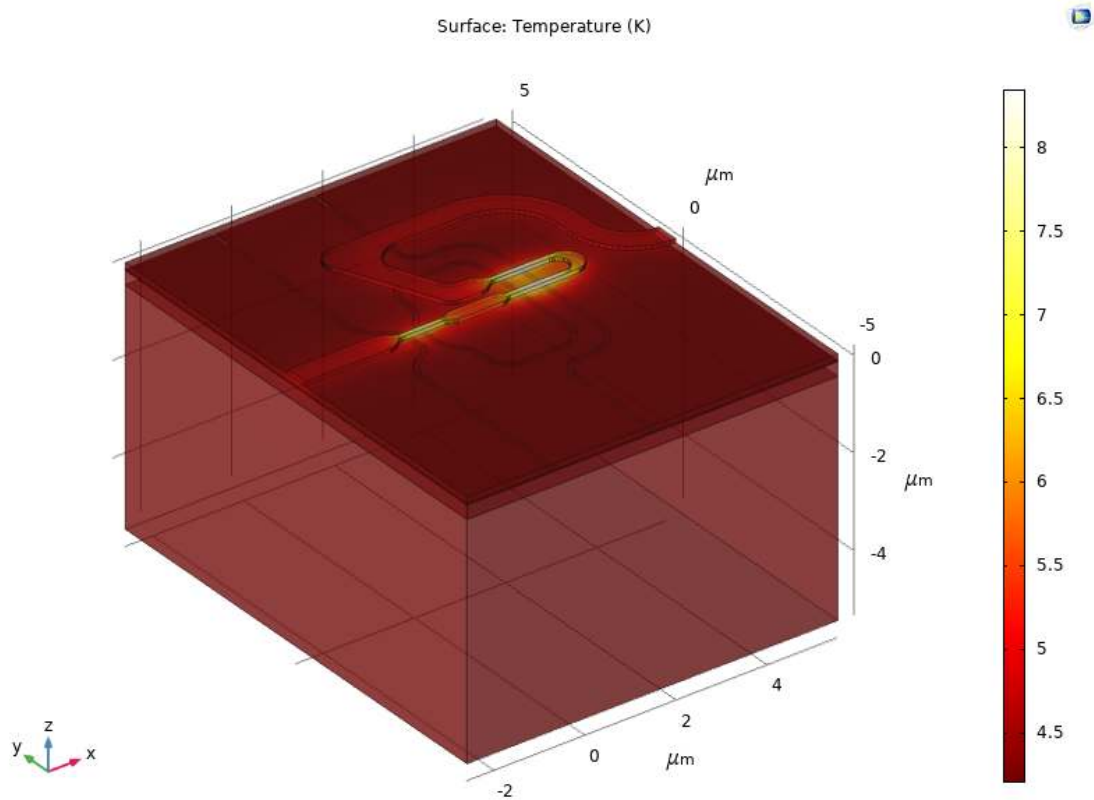
Joule Heating



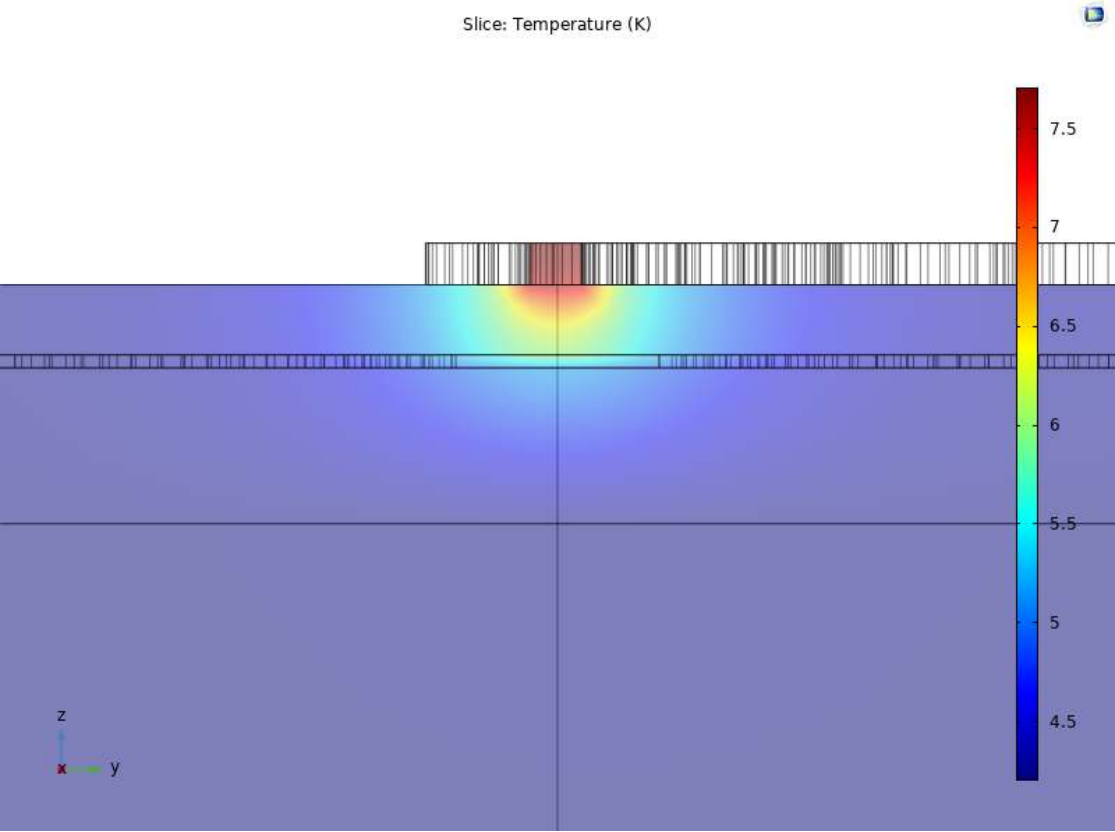
Model geometry



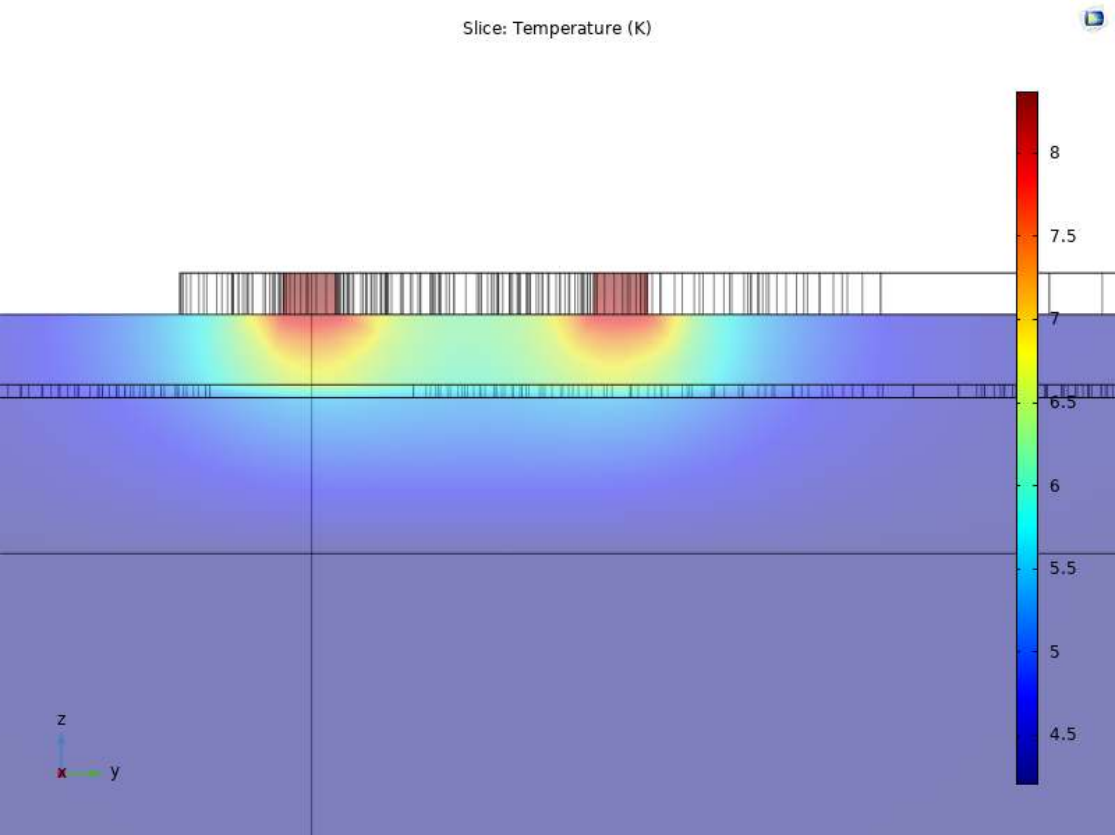
Heater bias= $100\text{e-}6$, channel bias= $5\text{e-}6$



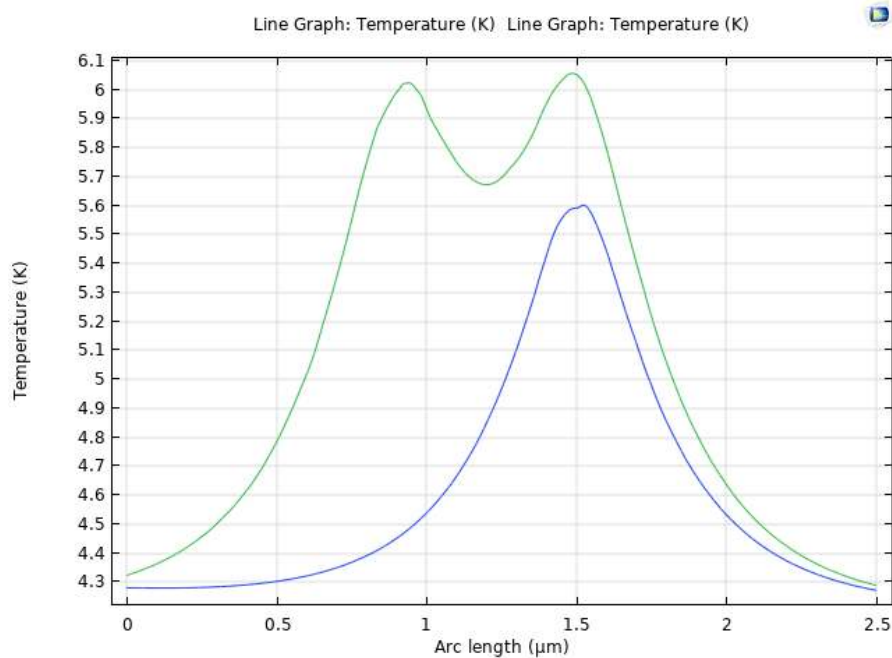
Joule heating. Bottom of Si substrate was set to 4.2K



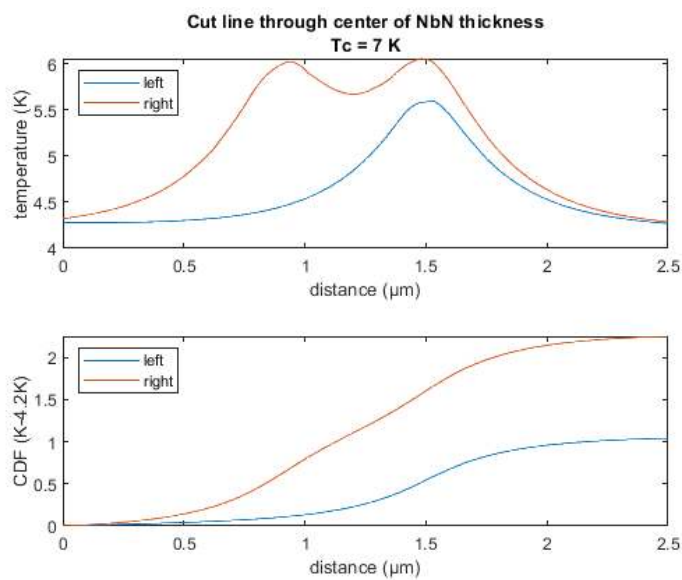
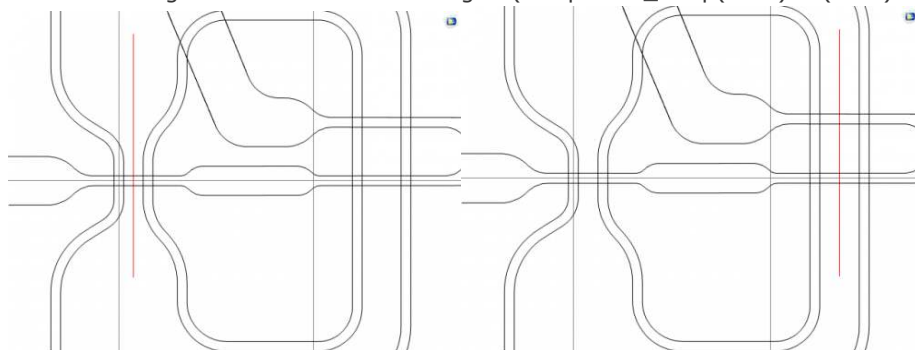
Slice through left channel.



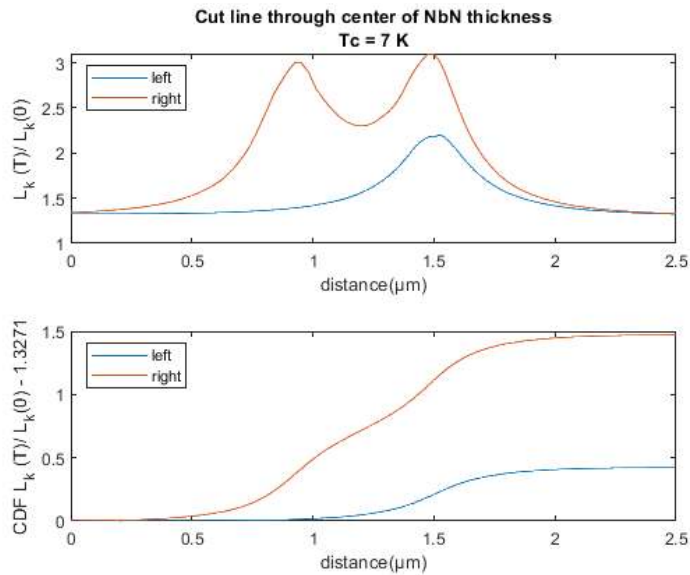
Slice through right channel



Absolute Integral := $m \cdot K$. Relative Integral (Temp-base_temp(4.2K) = ($m \cdot K$))



With two wires we cumulatively get 2x increase in temperature.



Calculating the increase in inductance we get a $\sim 3\times$ cumulative increase.

Using:

J. Appl. Phys. **119**, 234302 (2016)

$$\frac{L_K(T)}{L_K(0)} = \frac{\Delta(0)}{\Delta(T) \tanh\left(\frac{\Delta(T)}{2kT}\right)}. \quad (3)$$

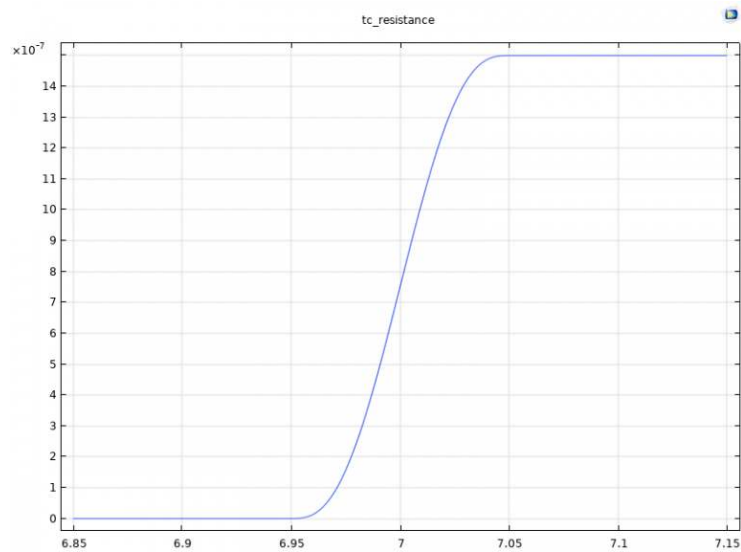
$$\Delta(T) \approx 1.76 k_B T_c \tanh\left(1.74 \sqrt{\frac{T_c}{T} - 1}\right) = \Delta_0 \tanh\left(1.74 \sqrt{\frac{T_c}{T} - 1}\right)$$

```
function Lk = inductance_temp(T, Tc)
    kb = 1.380649e-23;
    d0 = 1.76*kb*Tc;
    gap = d0*tanh(1.74*sqrt(Tc/T - 1));
    Lk = d0/(gap*tanh(gap/(2*kb*T)));
end
```

[data.zip](#)

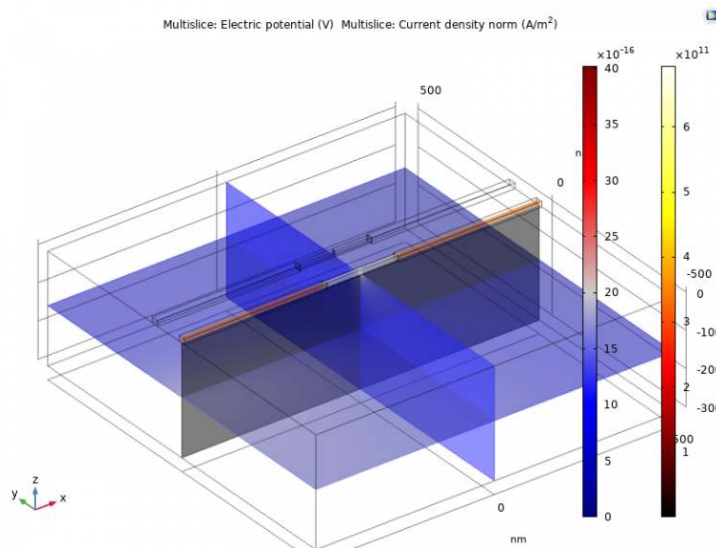
Superconducting properties

Trying to impose superconducting material properties to determine switching margins.

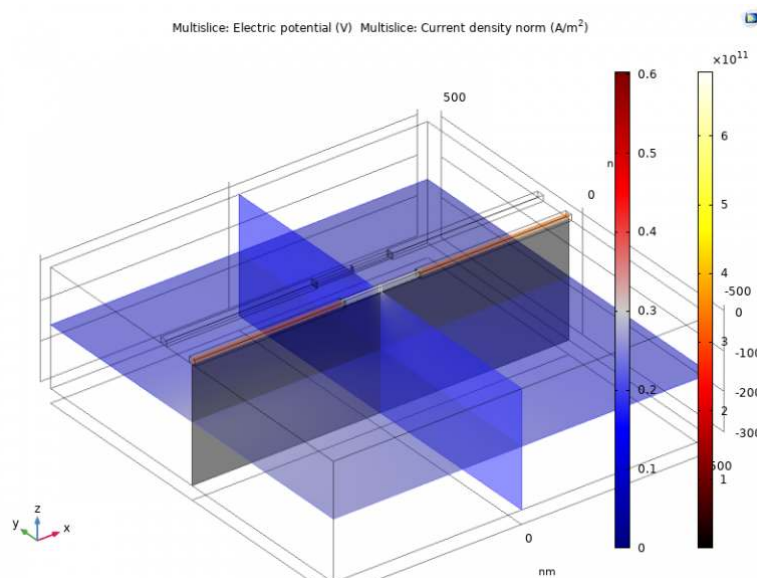


X axis – Temperature. Yaxis – Resistivity. $T_c = 7K$

Below I created a simple planar hTron geometry and set the bath temperature to 4.2K, and 8K. The top wire is Ti and has zero bias, the bottom wire is NbN biased at $100\mu A$. At 4.2K we can see the voltage is $1e-16V$, ie superconducting, and at 8K 0.6V, ie normal.

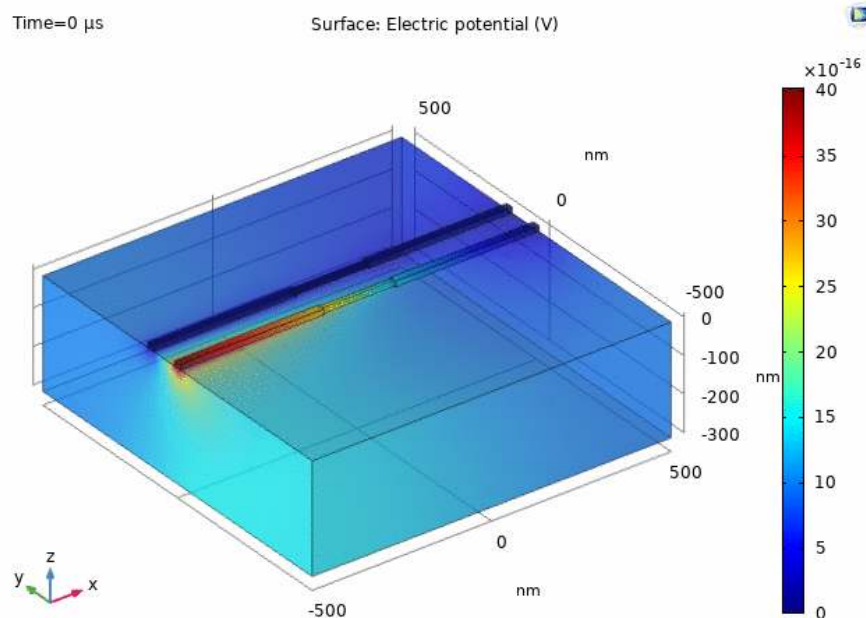


4.2K

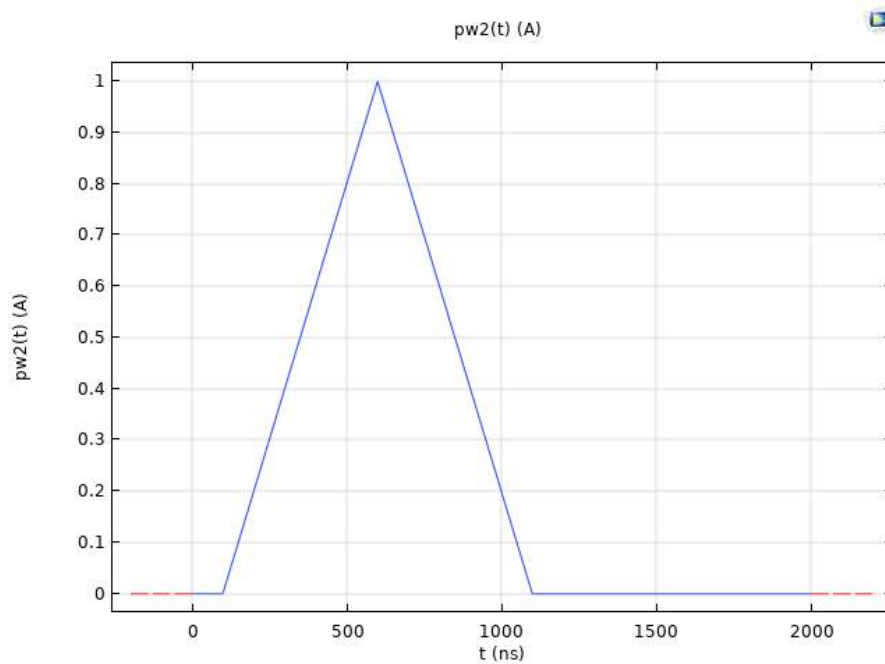


8K

Time dependent simulation showing the NbN wire latch.



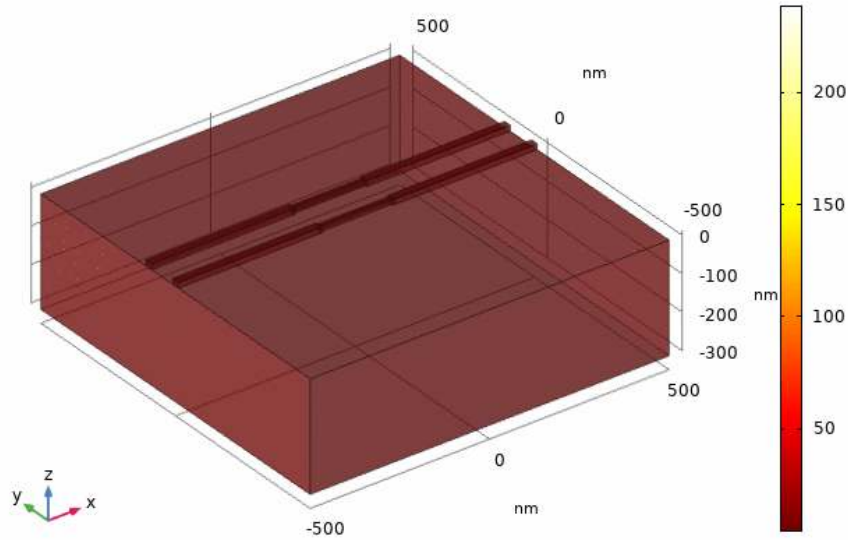
First frame $t=0$ note that the voltage on the NbN wire is $1\text{e-}16$. Once the pulse to the Ti wire turns on the scale increases to $\sim 1.4\text{V}$. After the pulse the persistent voltage on the NbN wire is 0.2V .



Input pulse on the Ti (top) wire. Scaled to 1mA in simulation

Time=0 μ s

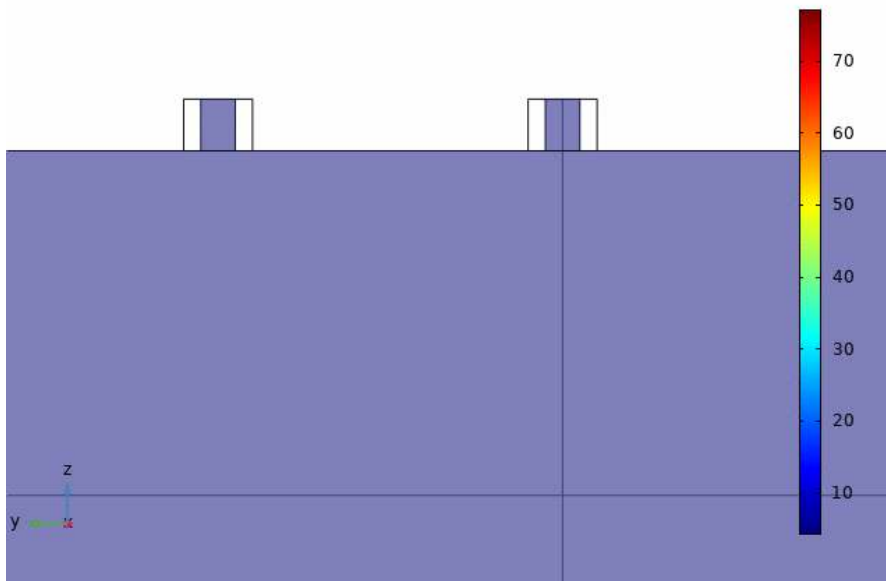
Surface: Temperature (K)



Temp is pretty high. Overall not addressing realistic thermal properties at this stage. This does show how heating one wire, heats up the second until it becomes resistive.

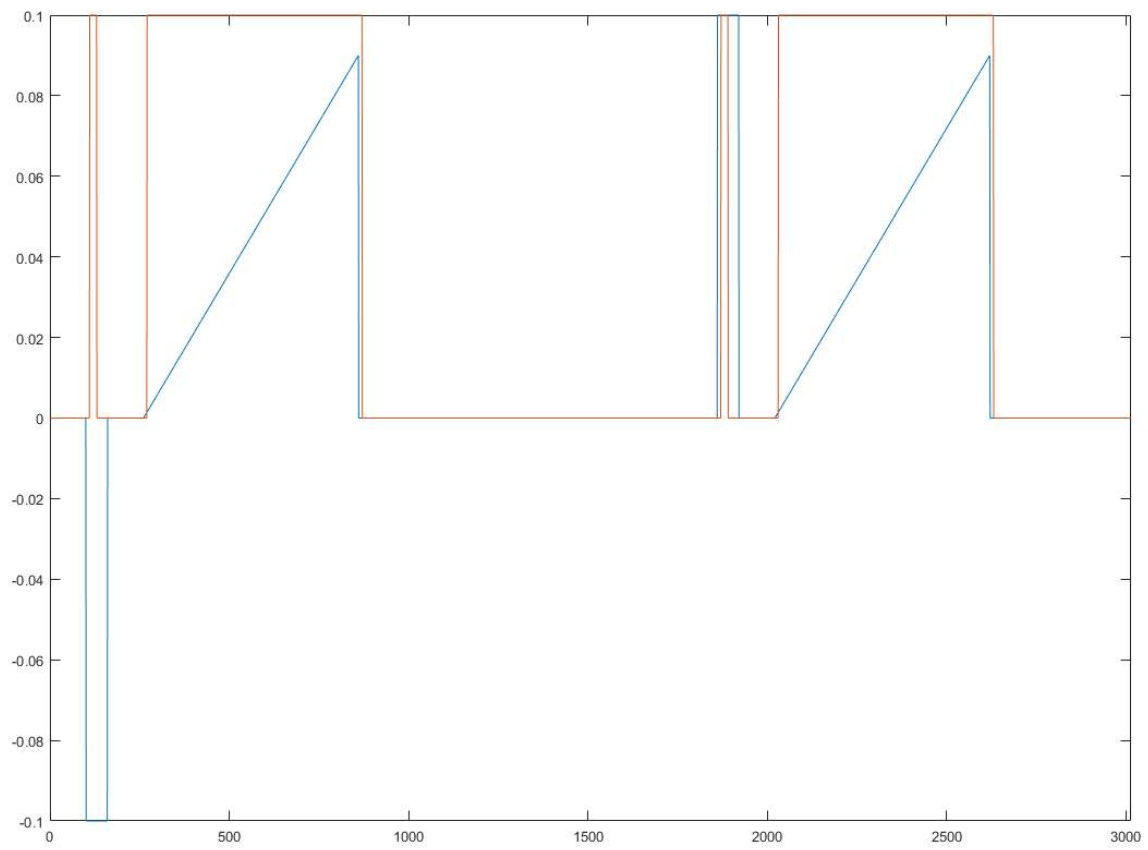
Time=0 μ s

Slice: Temperature (K)



Zoom in slice (also range is capped at 77K) to show that the heat does indeed travel through the substrate.

[joule_heating_example_superconductor.mph](#)

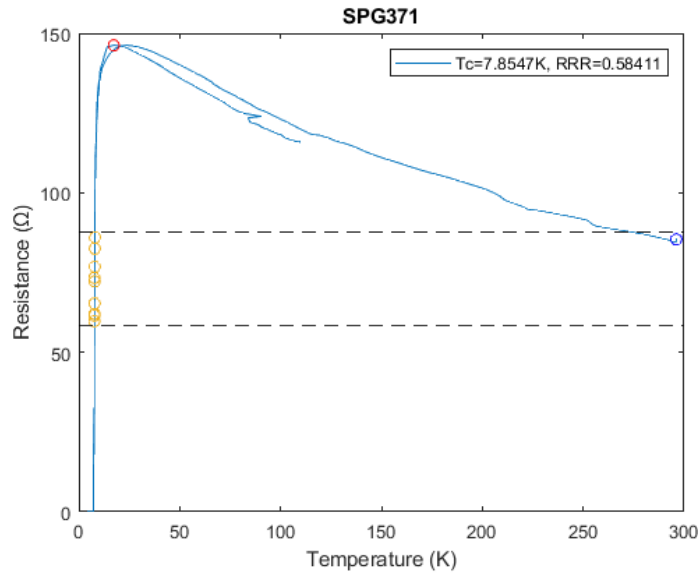


SPG371 – wide wire snspd NbN

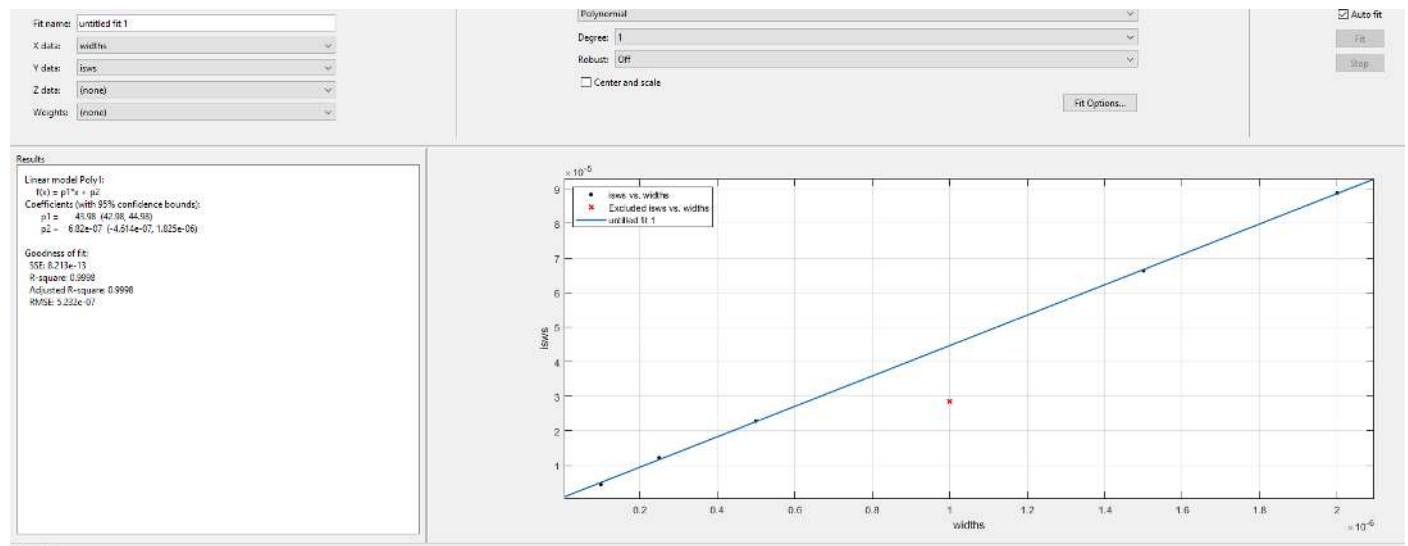
January 20, 2021

Categories: NbN deposition, SNSPD, Superconductivity

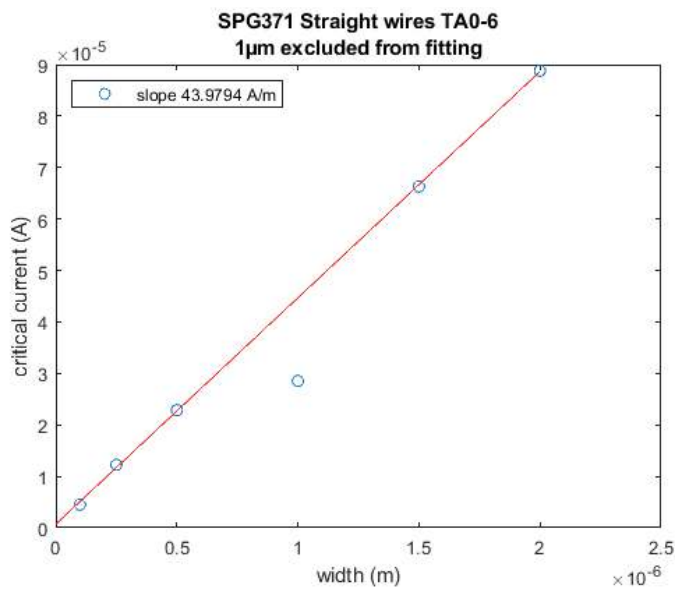
SPG371



Critical Current

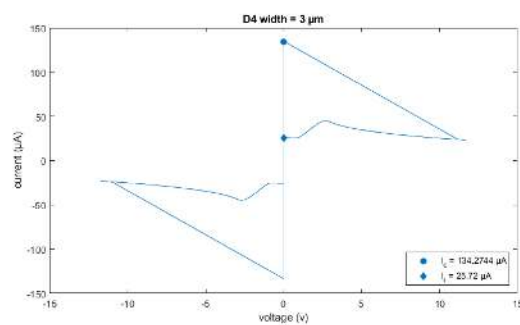
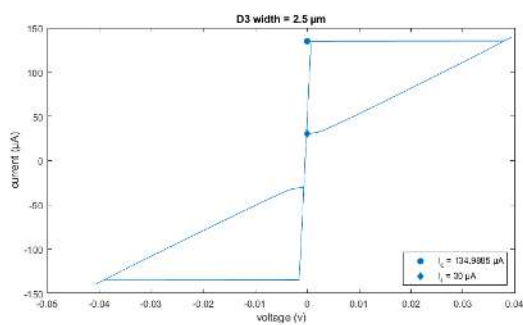
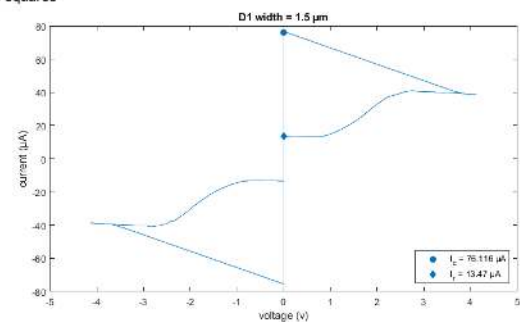
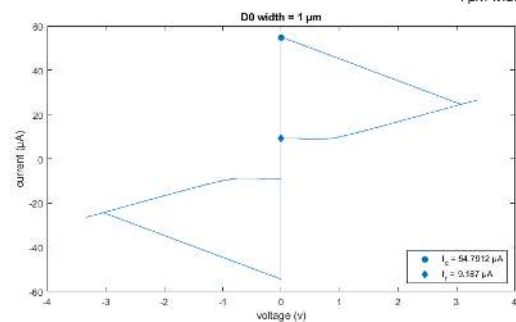


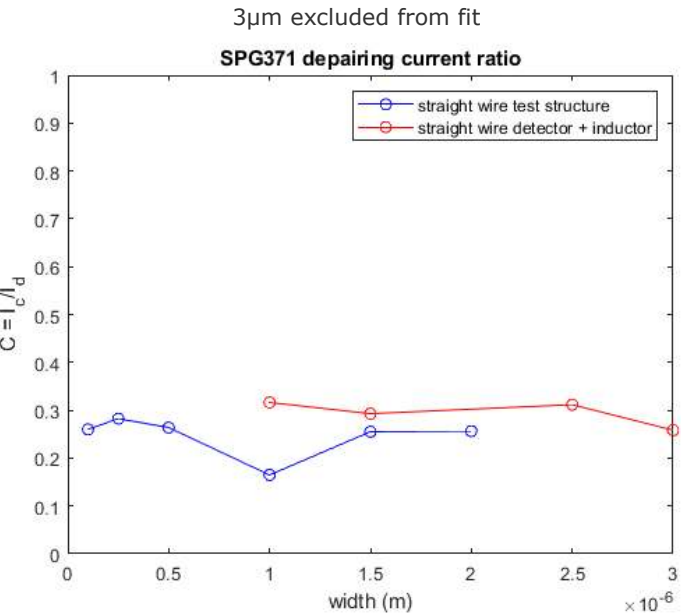
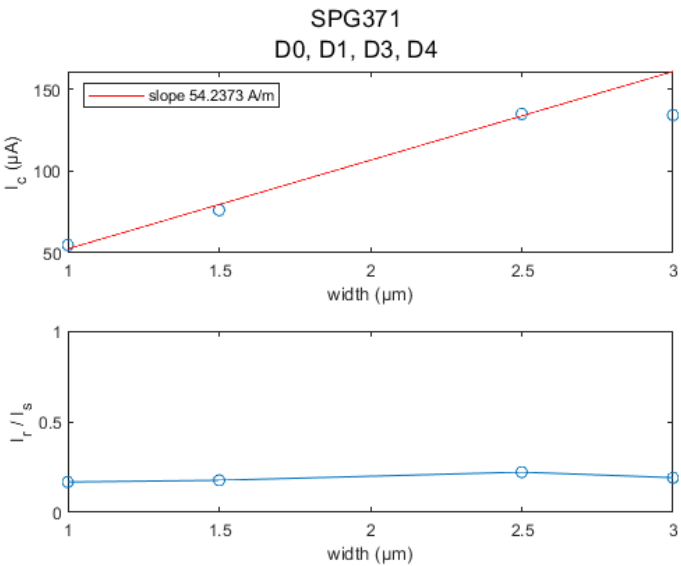
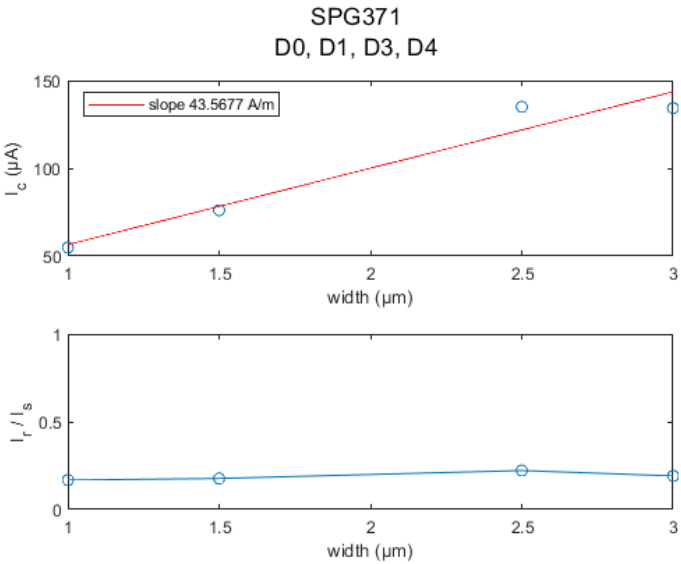
Jc fitting to TA0 TA1 TA2 TA5 TA6. TA4(1 μ m) was excluded. Slope is 43.98 A/m. Thickness is 3.8nm. $J_c = 1.15e10 A/m^2 = 11.5 GA/m^2 = 1.15 MA/cm^2$



$$43.97 \text{ (A/m)} / (4.37 \times 10^{-9} \text{ m}) = 1.0062 \times 10^{10} \text{ (A/m}^2\text{)} = 1.0062 \text{ MA/cm}^2$$

SPG371 60 μ m long straight snspds
7 μ m wide inductor 1500 squares

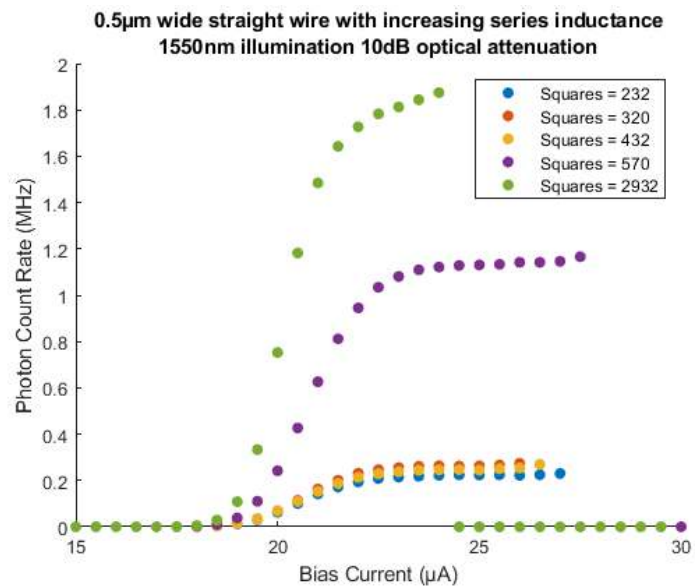


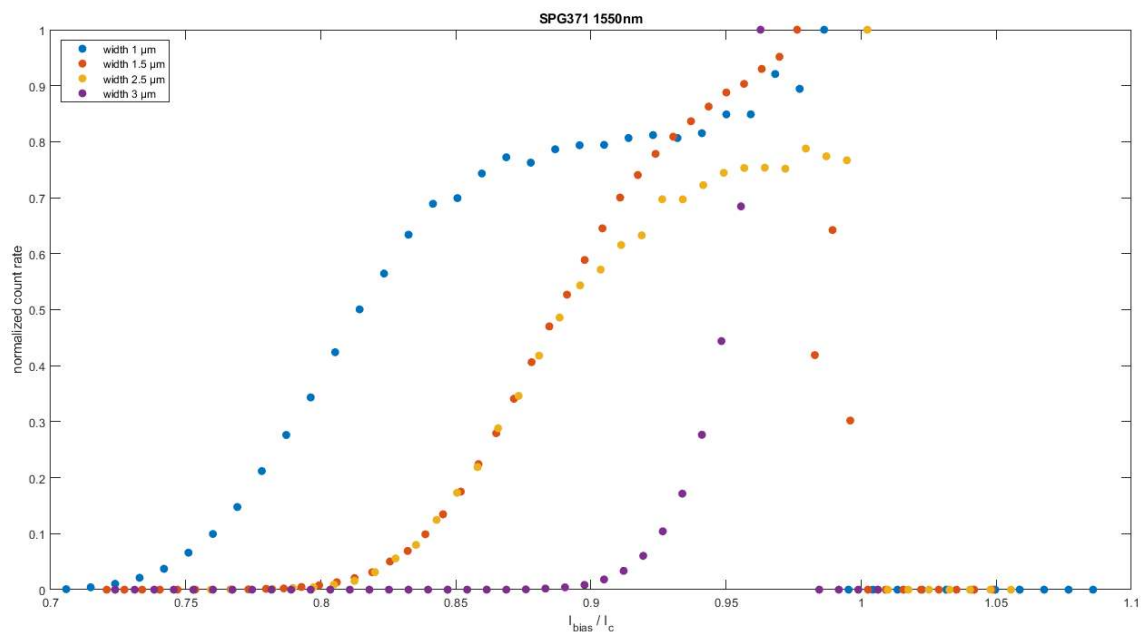
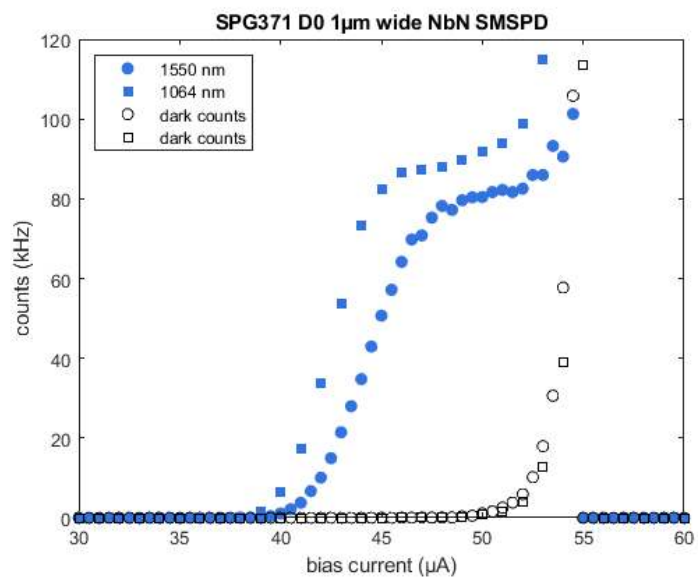


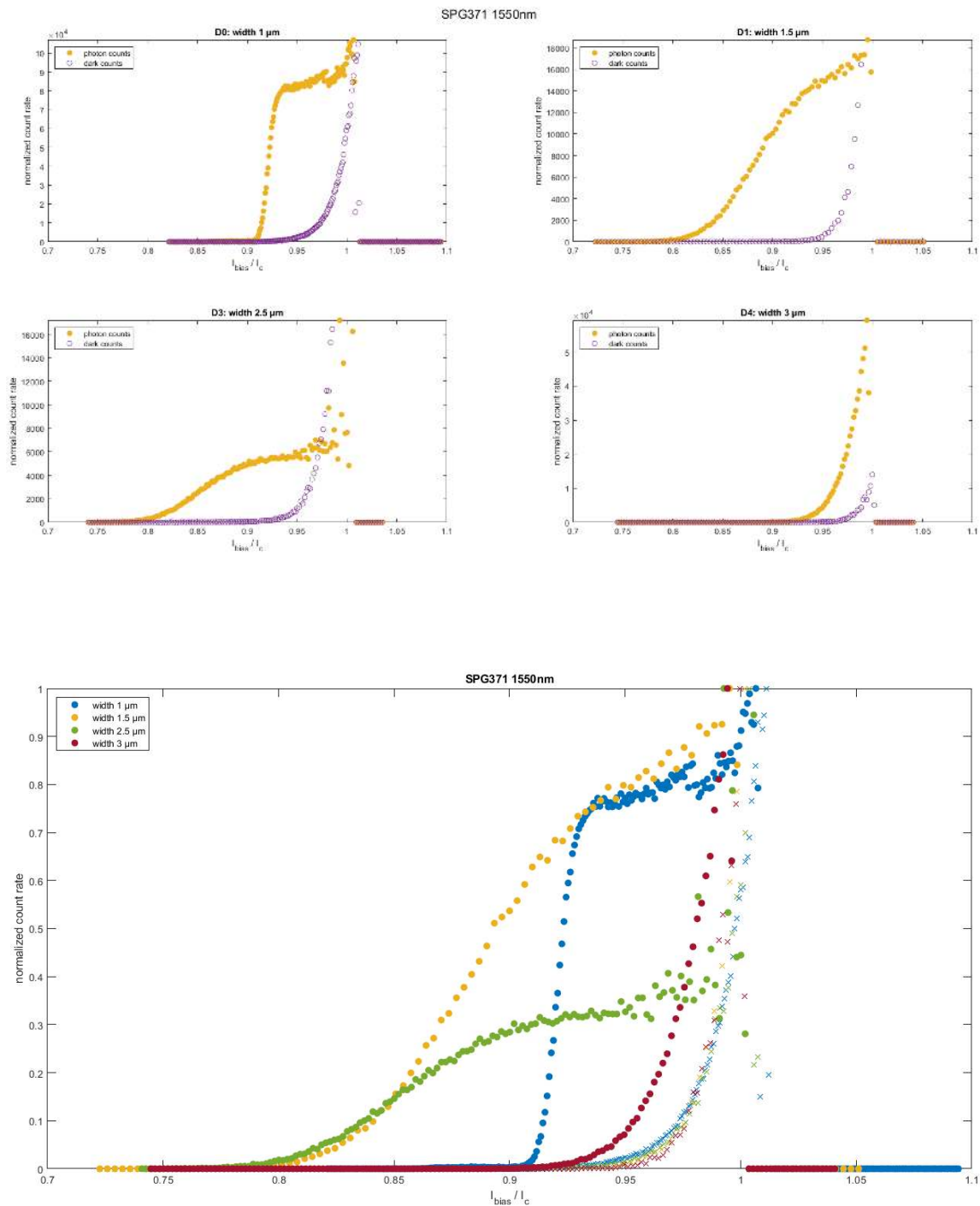
Depairing current calculated using the KL method with $R_s=R_{max}$

Photon Counting

0.5 μ m



$1\mu\text{m}$ 



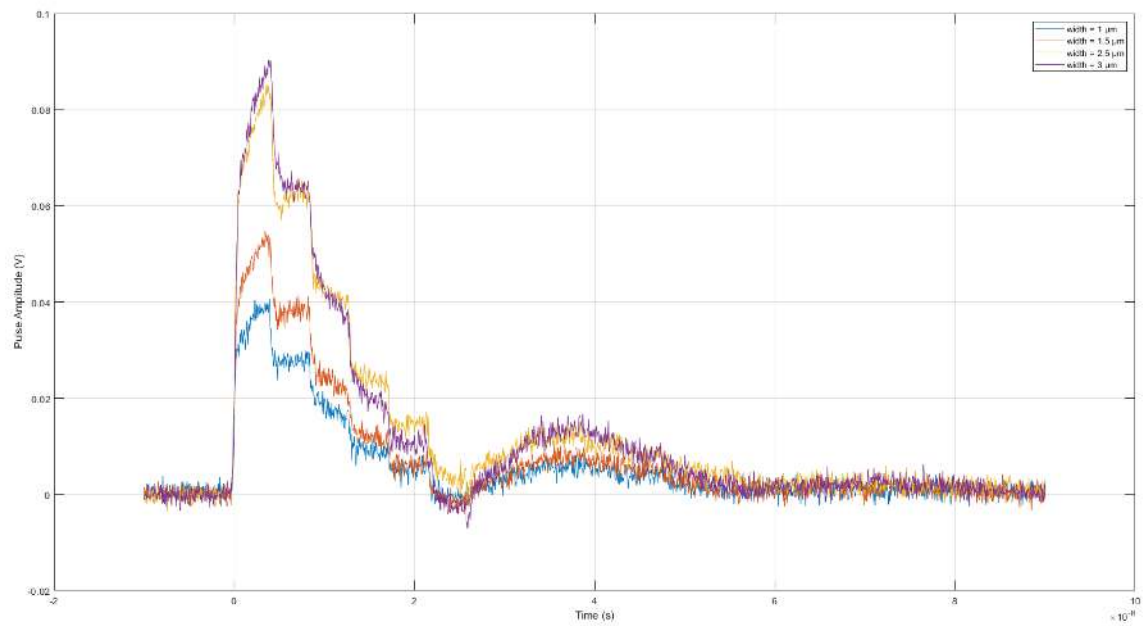
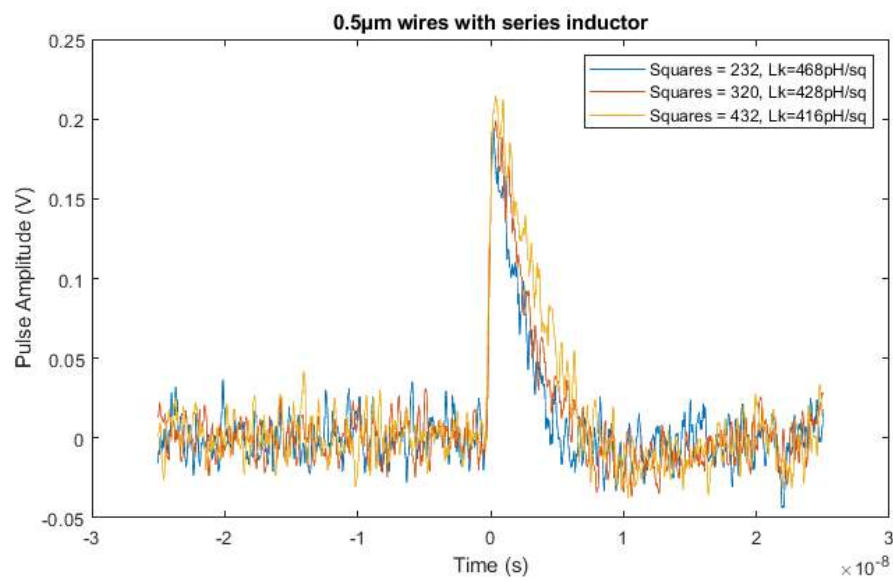
Pulse Analysis

fitting equation: $y = a \cdot \exp(-b \cdot x) + c$

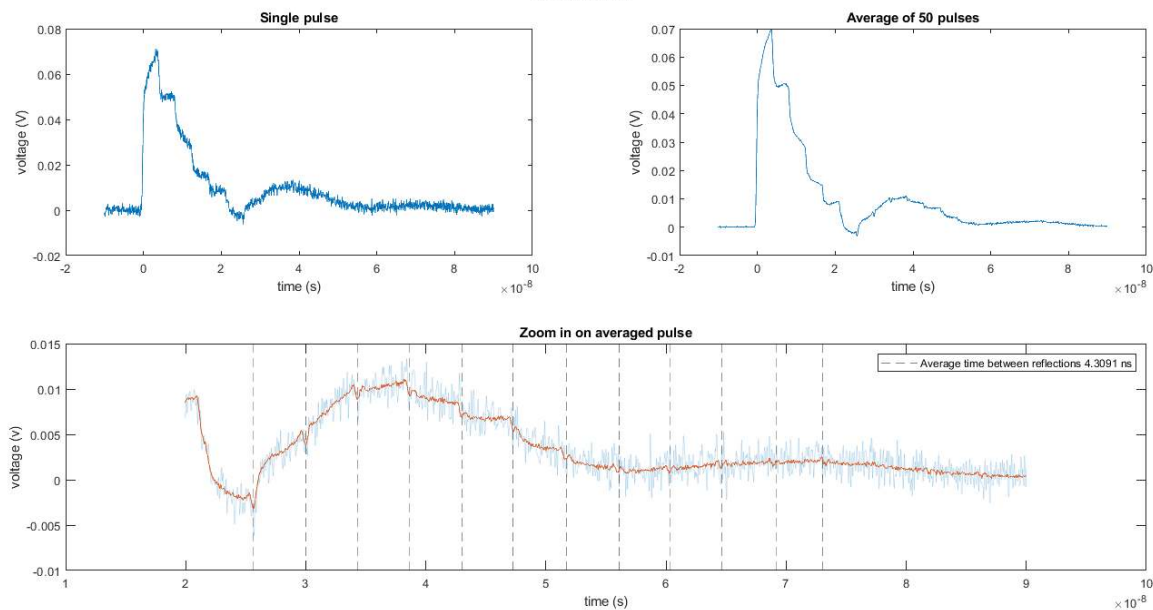
```
function Lk = kinetic_inductance(obj, b)
    %Returns kinetic inductance in pH
    tau = 1/b;
    Lk = tau*50 * 1e12;
end
```

B0_squares = 232;

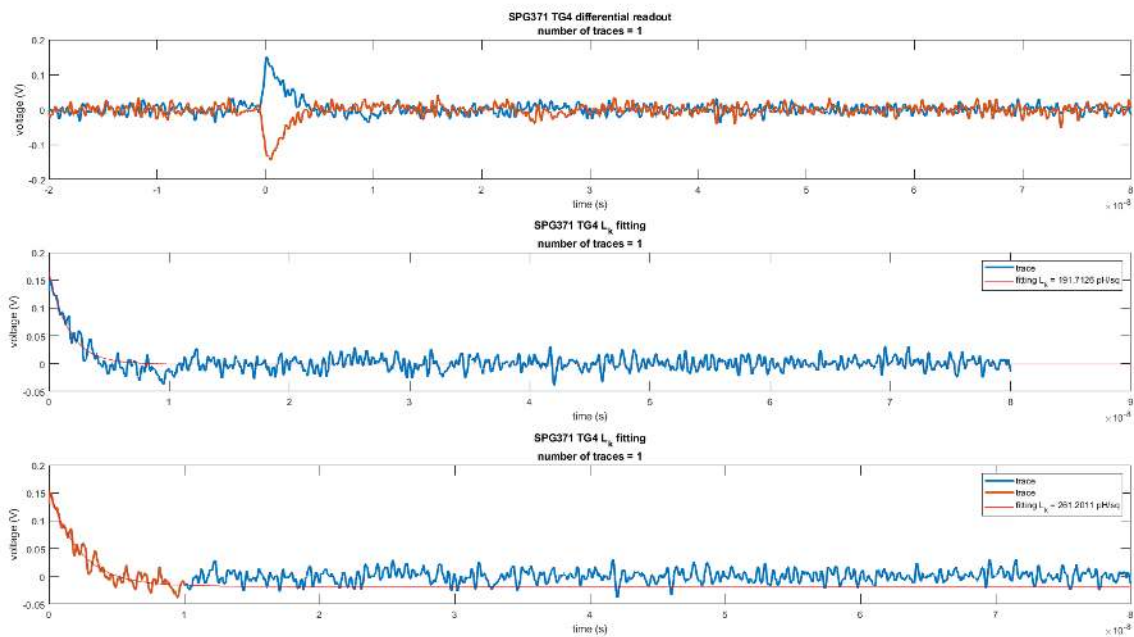
B0_Lk = qf.kinetic_inductance(b=4.607e8)/B0_squares

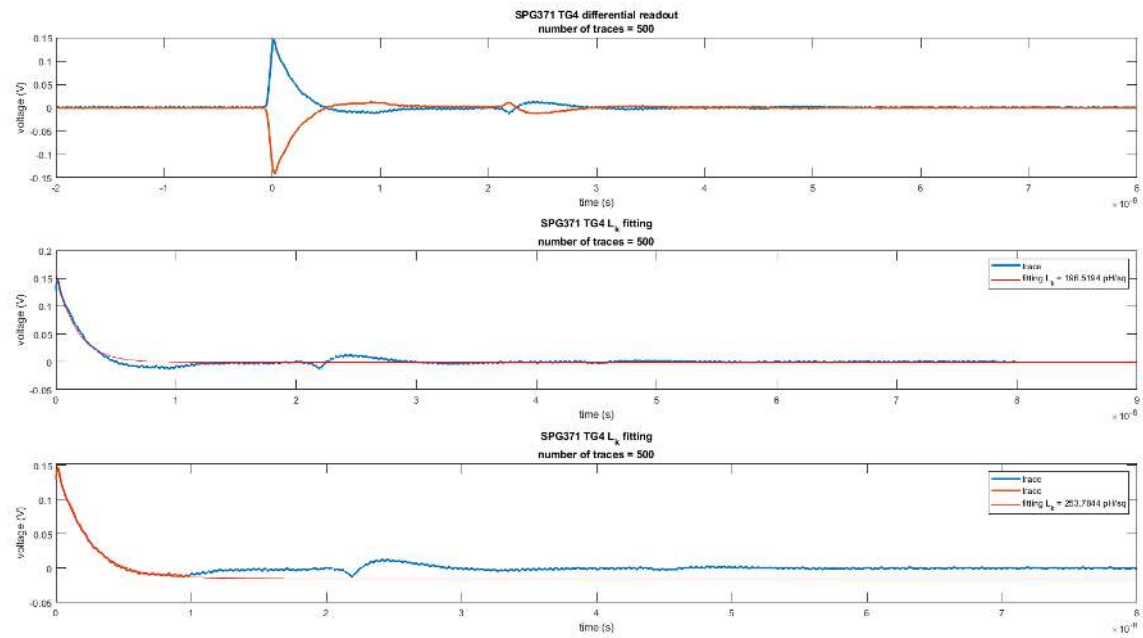


SPG371 D3

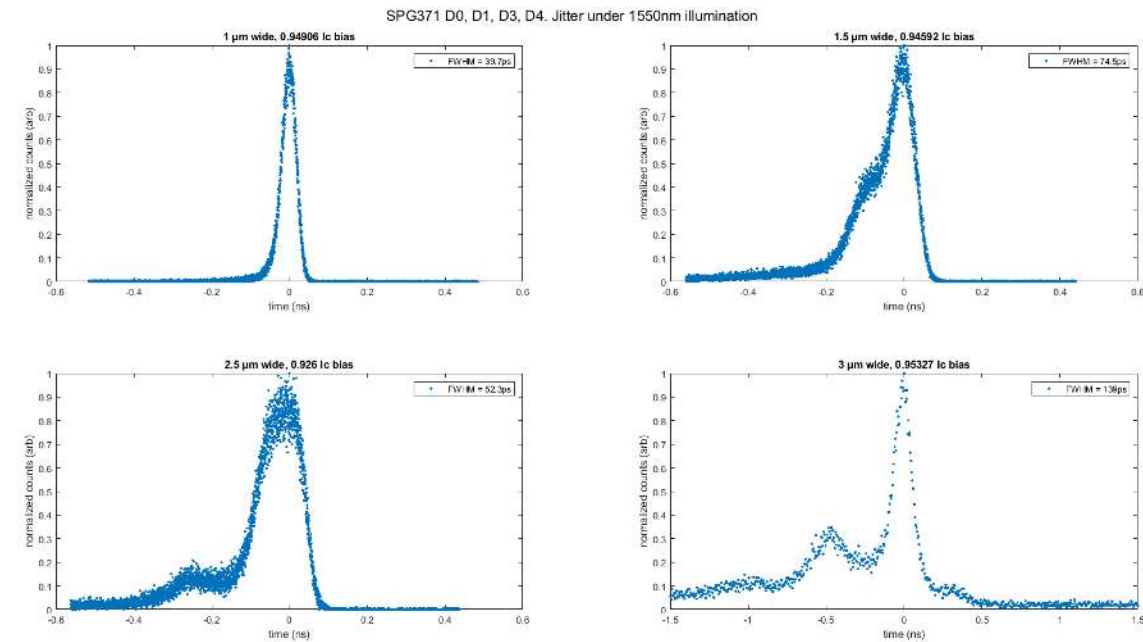


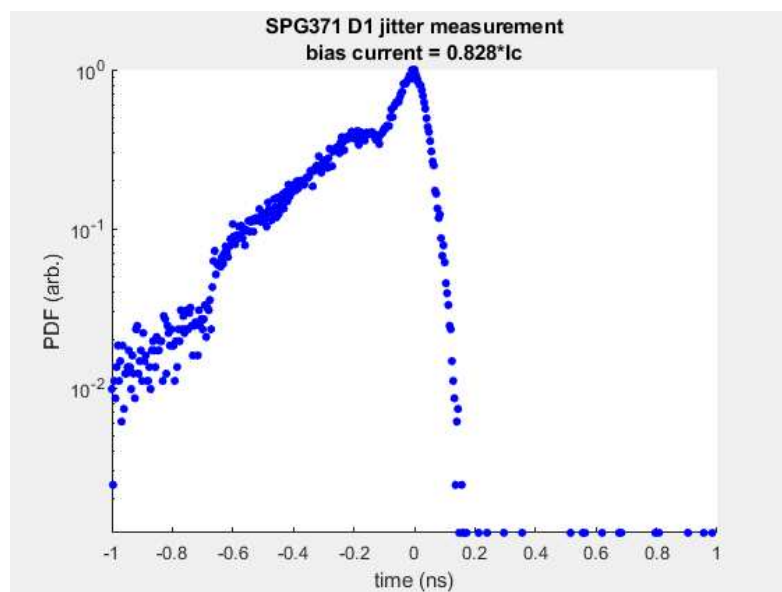
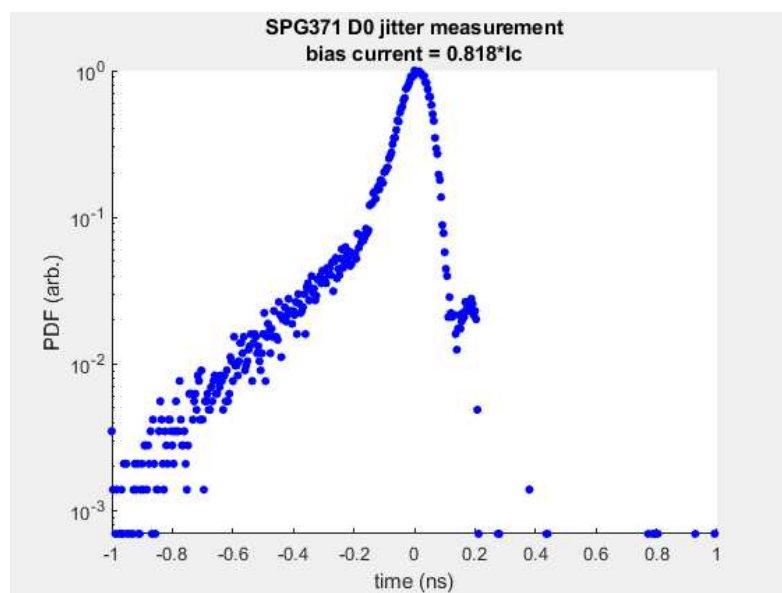
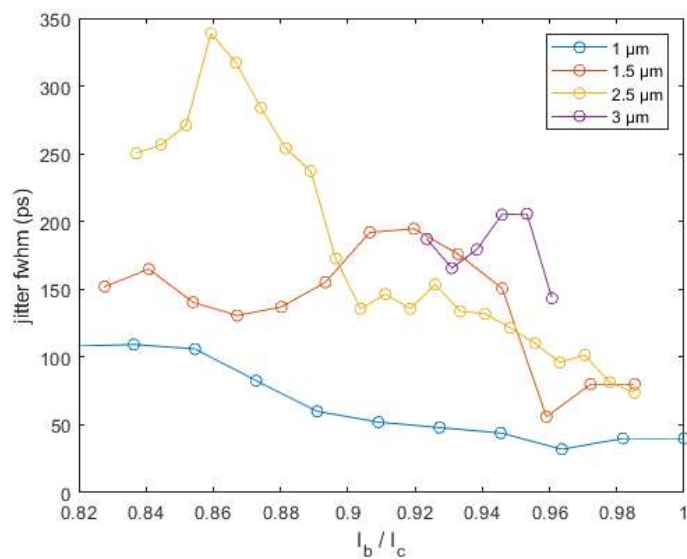
reflections are from cables. $6c \text{ (m/s)} * = 0.77\text{m}$

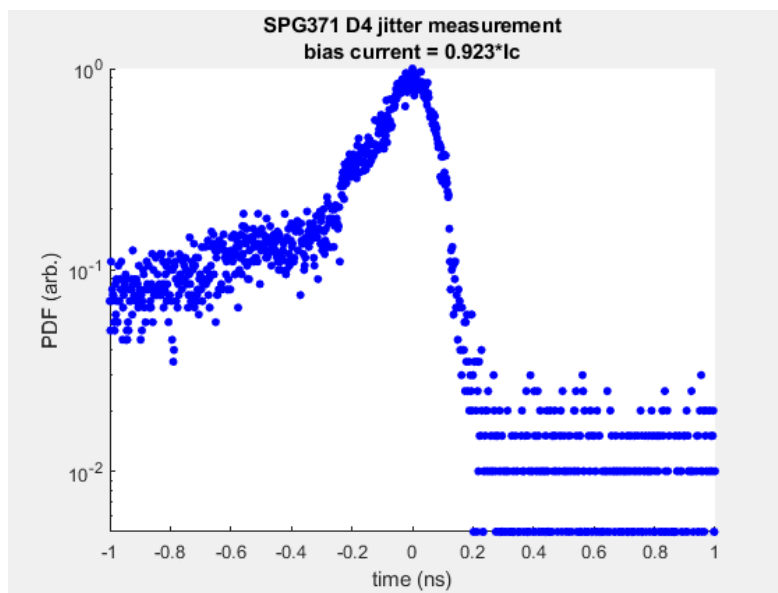
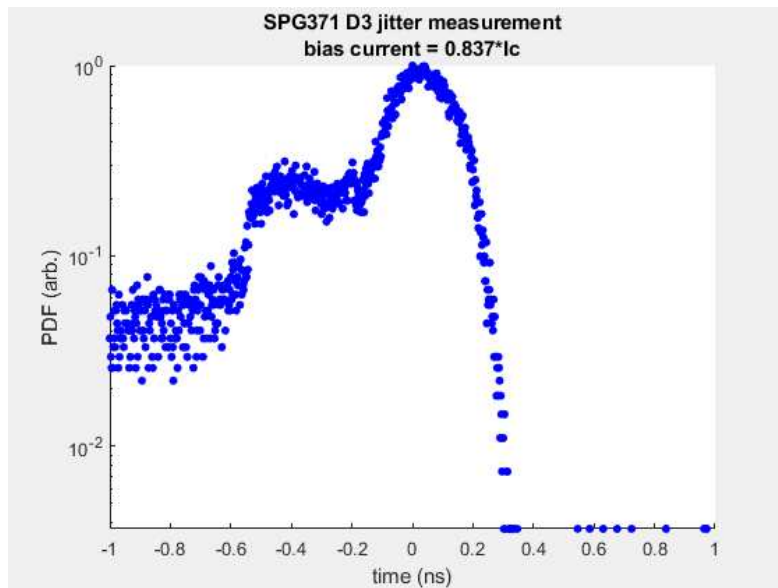


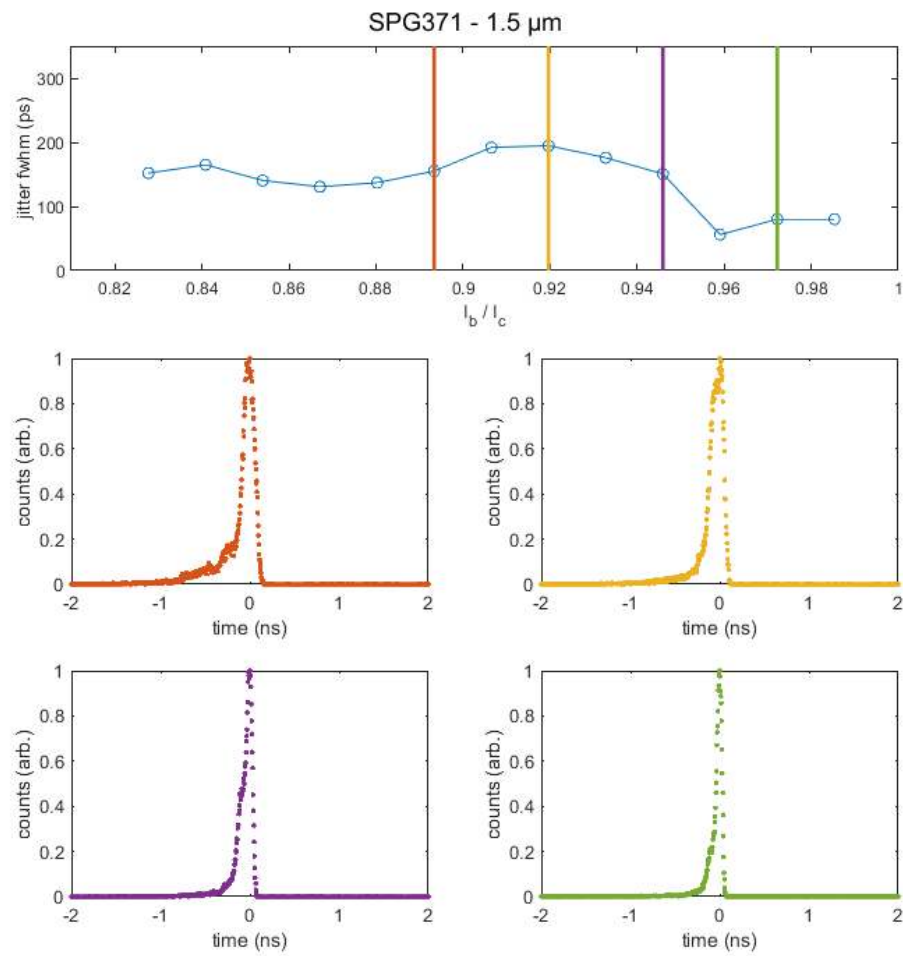


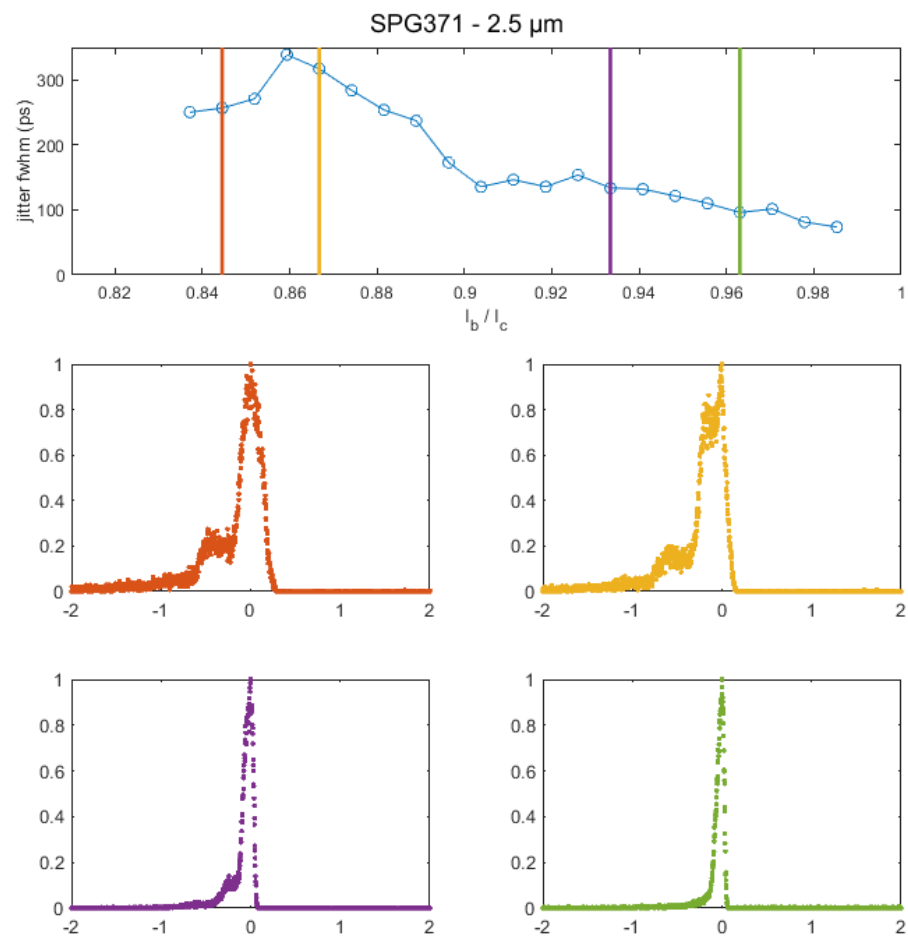
Jitter

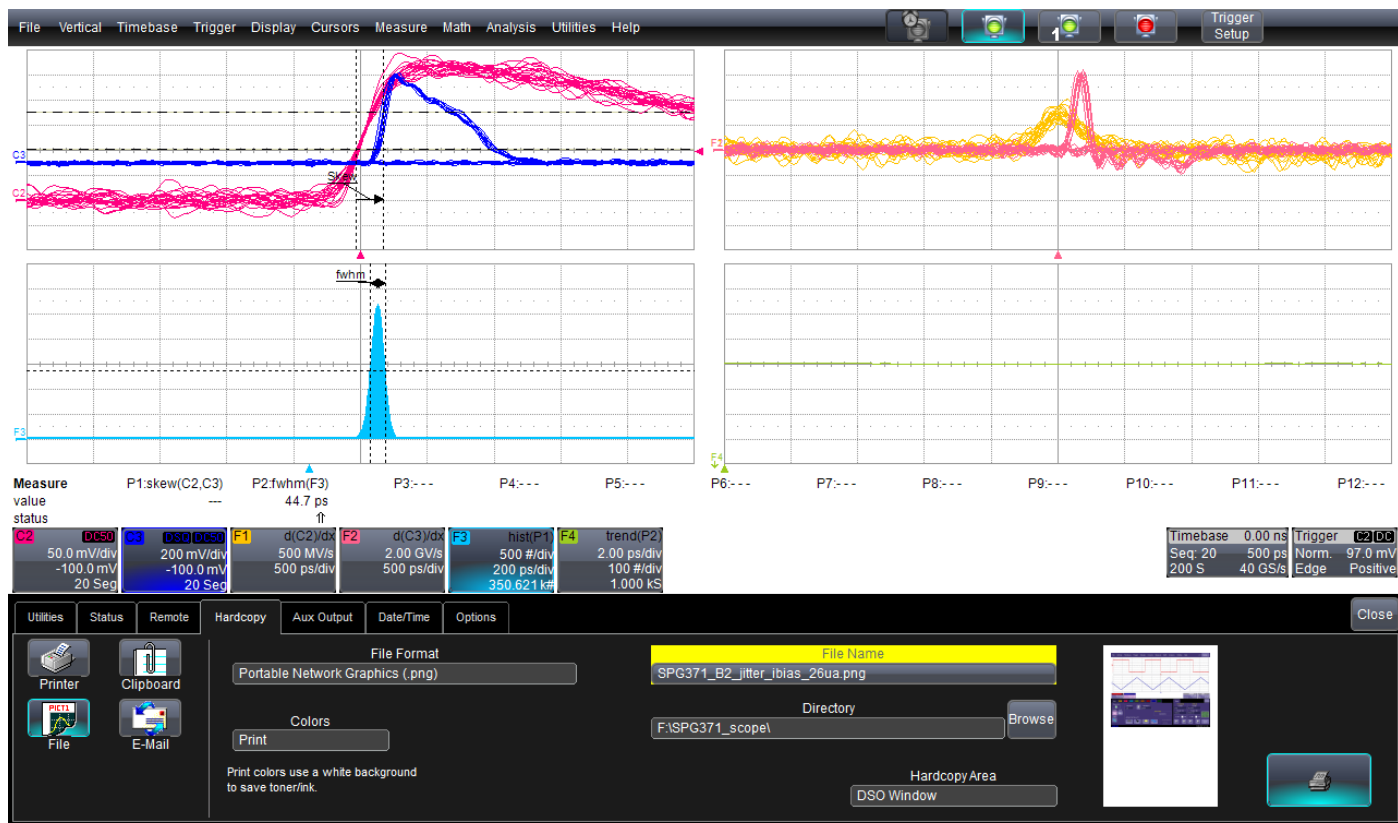












Jitter measurements on B2. FWHM = 44.7 ps. The skew was measured from a single ended readout and the SYNC port of the CALMAR laser (which is not as good as the InGaAs photodiode). The bias current was 26 μ A.

Film Characterization

Model: (not saved)

Model SettingsManage

MULTI-SAMPLE Analysis Mode

Layer #2: n&k

Thick(nm).2:

4.45

☒

0

60

10

☐ hide parms

57.51

☒

23.55

☒

8.63

☒

n(466nm).2:

2.2392

☒

0

6

0

n(522nm).2:

2.3736

n(598nm).2:

2.6092

n(638nm).2:

2.9048

k(466nm).2:

2.2641

☒

0

6

0

k(522nm).2:

2.7803

k(598nm).2:

3.1677

k(638nm).2:

3.387

Layer #1: SiO2

Thick(nm).1:

295.98

☒

280

320

0

Substrate: Si

Angle:

66.338

☒

0.0

0.0

0.0

Fit Data

Generate

Simulate

Sim. vs. Parm.

Model Validator

Fit Diff. = 0.01711

S = sin2Ψ sinΔ

0.7847

0.3158

0.3557

0.8506

N = cos2Ψ

☐ Show Data Values

Graph Type: S vs. N

☒ Zoom

Multi-Sample Files:

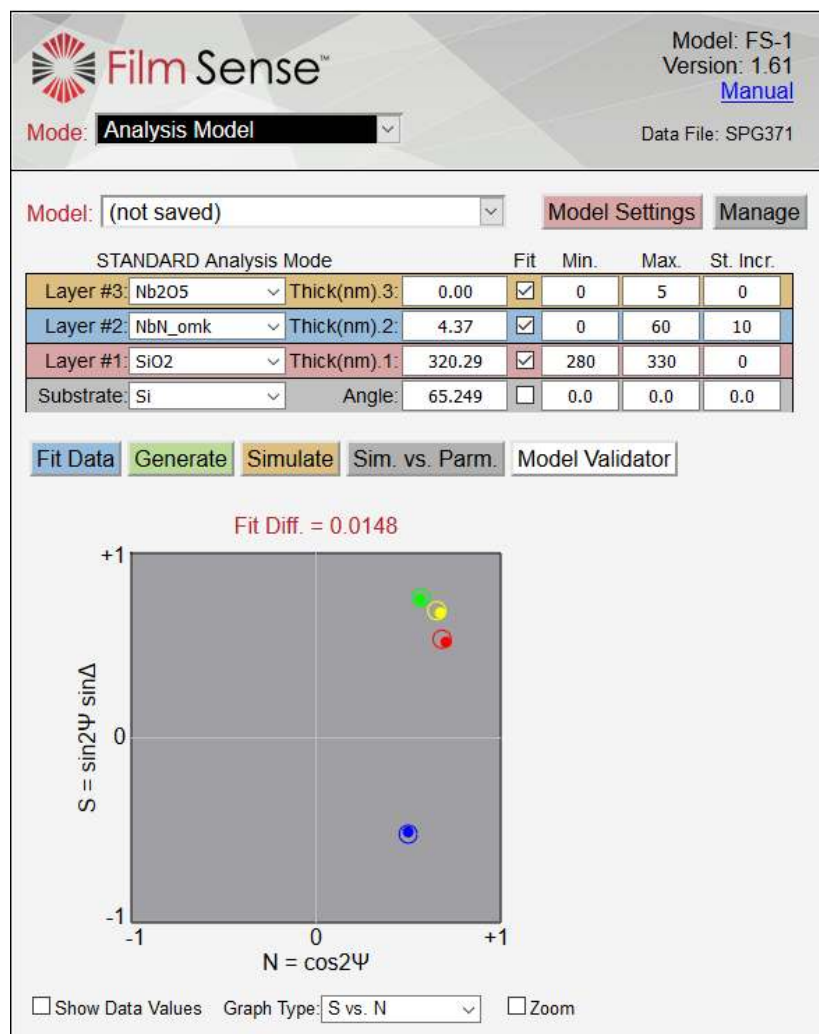
SPG395

SPG394

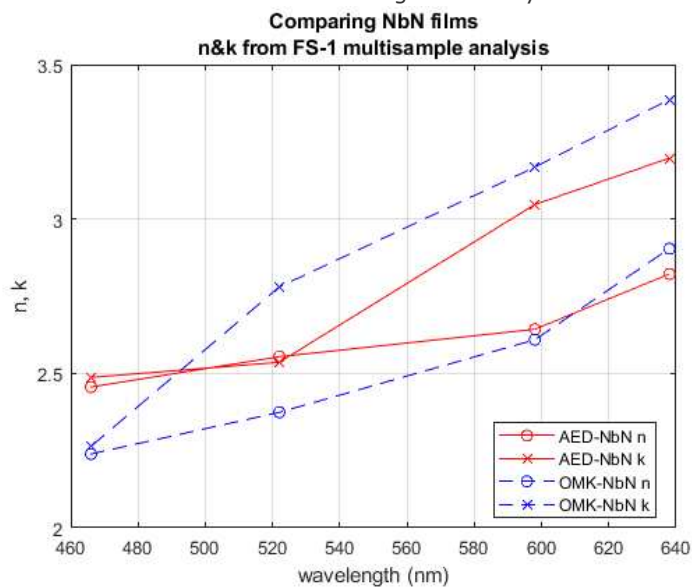
SPG393

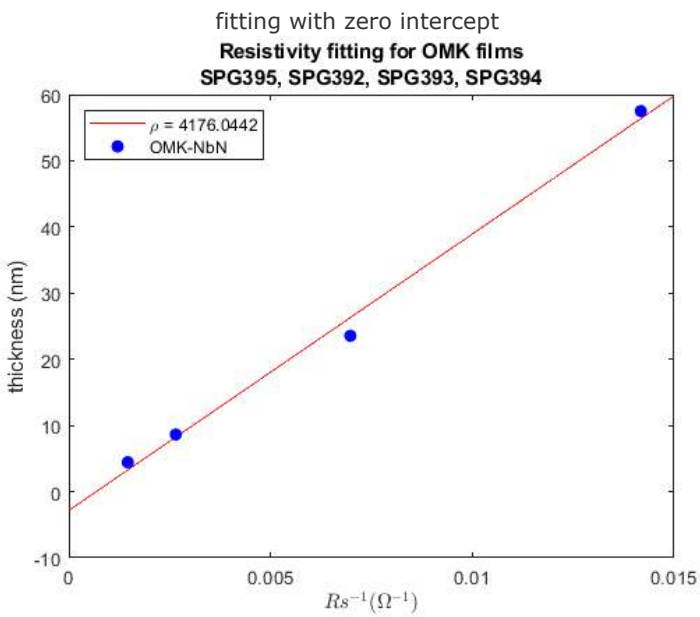
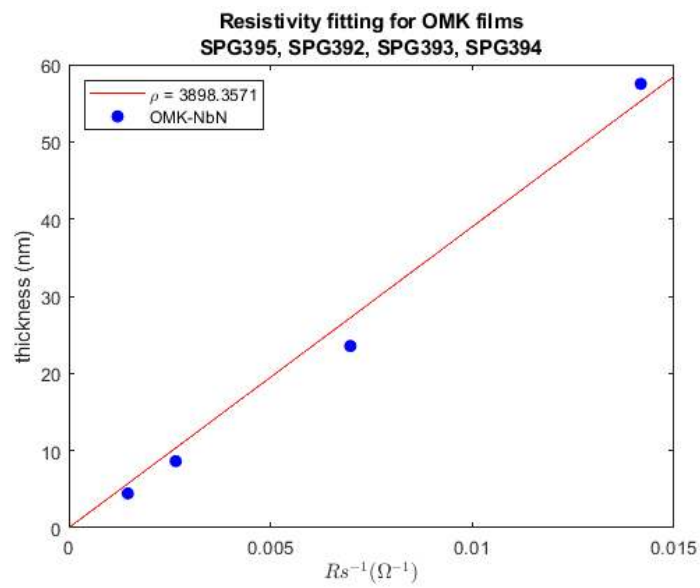
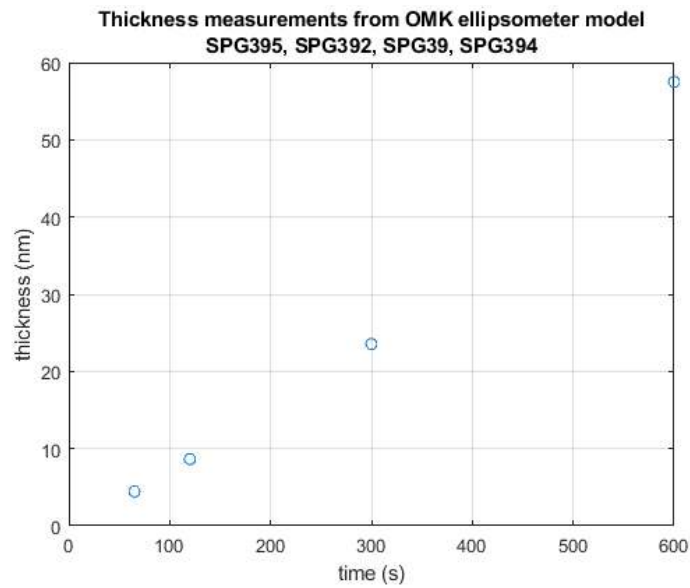
SPG392

Assemble Data

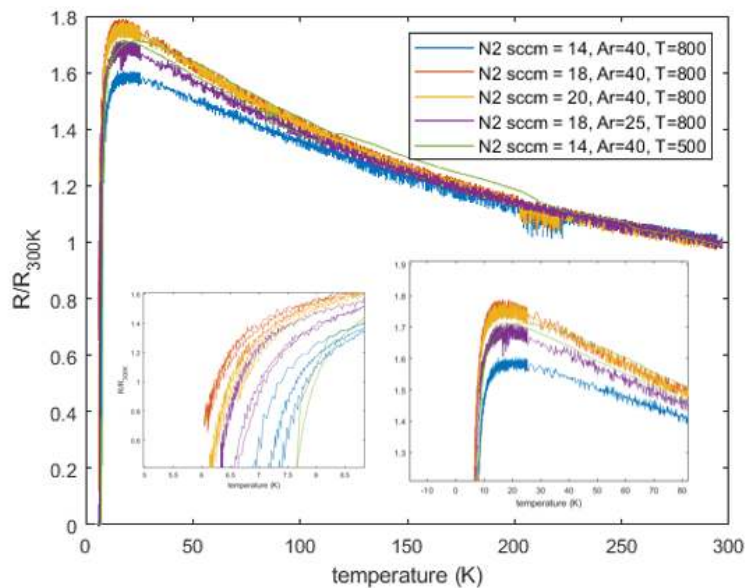


This thickness still results in a $\sim 240 \mu\Omega\text{-cm}$ resistivity. But the film was on a different substrate: high resistivity SiO₂ on Si





fitting with non-zero intercept b= -2.8445



G:\My Drive\...

Projects_snsdpd\wide_wires\SPG261\DepairingCurrent\calculation.m

Appendix

S:\SC\Measurements\SPG371

[SPG371_device_doc.txt](#)

[SPG371_2020-11-19 10-05-34.gds](#)

[SPG371-Data.zip](#)

Multipoint DC probes

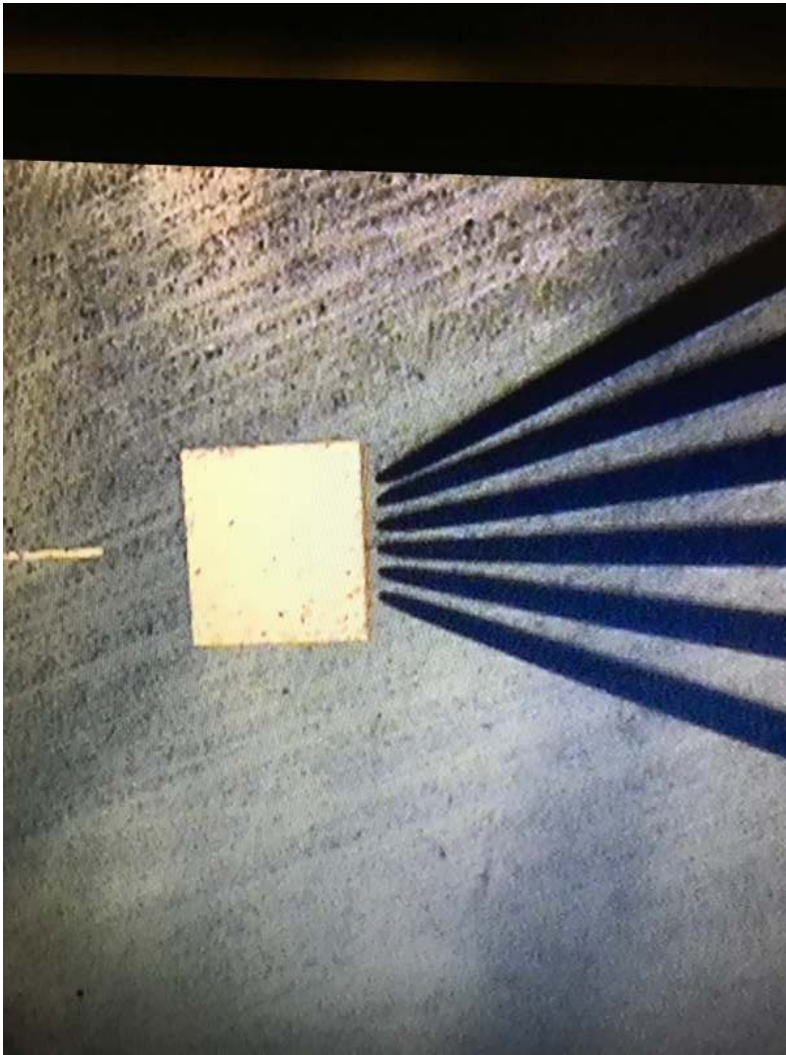
January 31, 2021

Categories: General

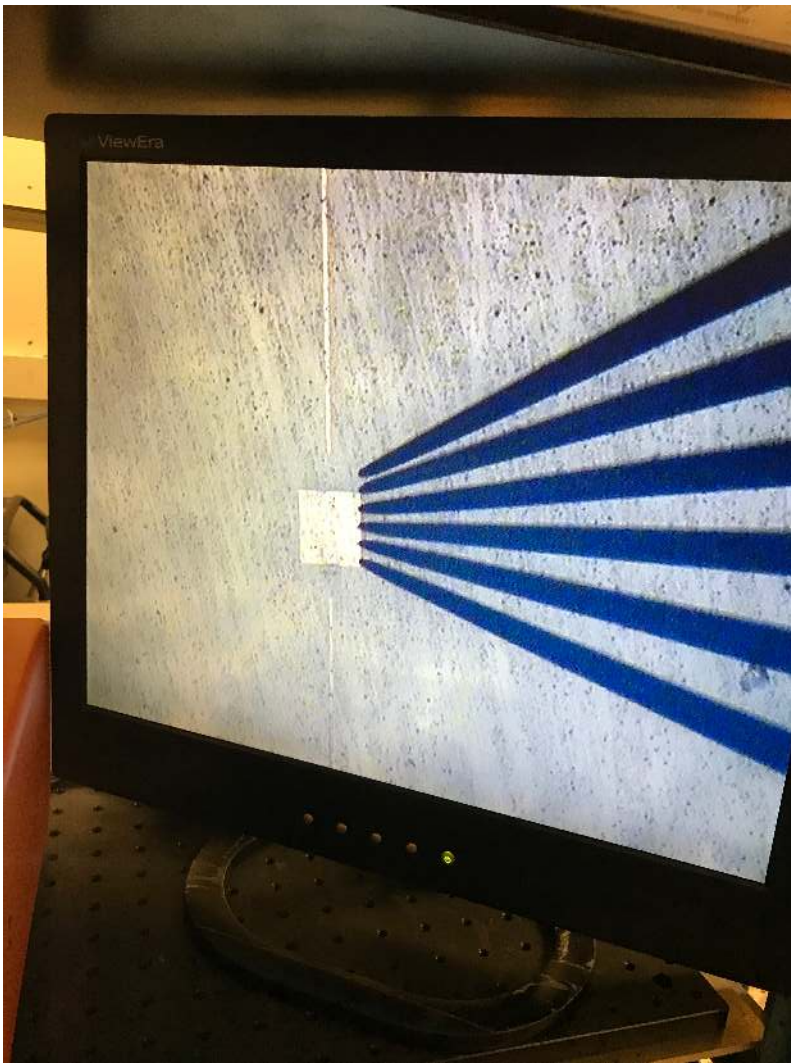
PicoProbe MCW-22-9909-3 S/N: 31770



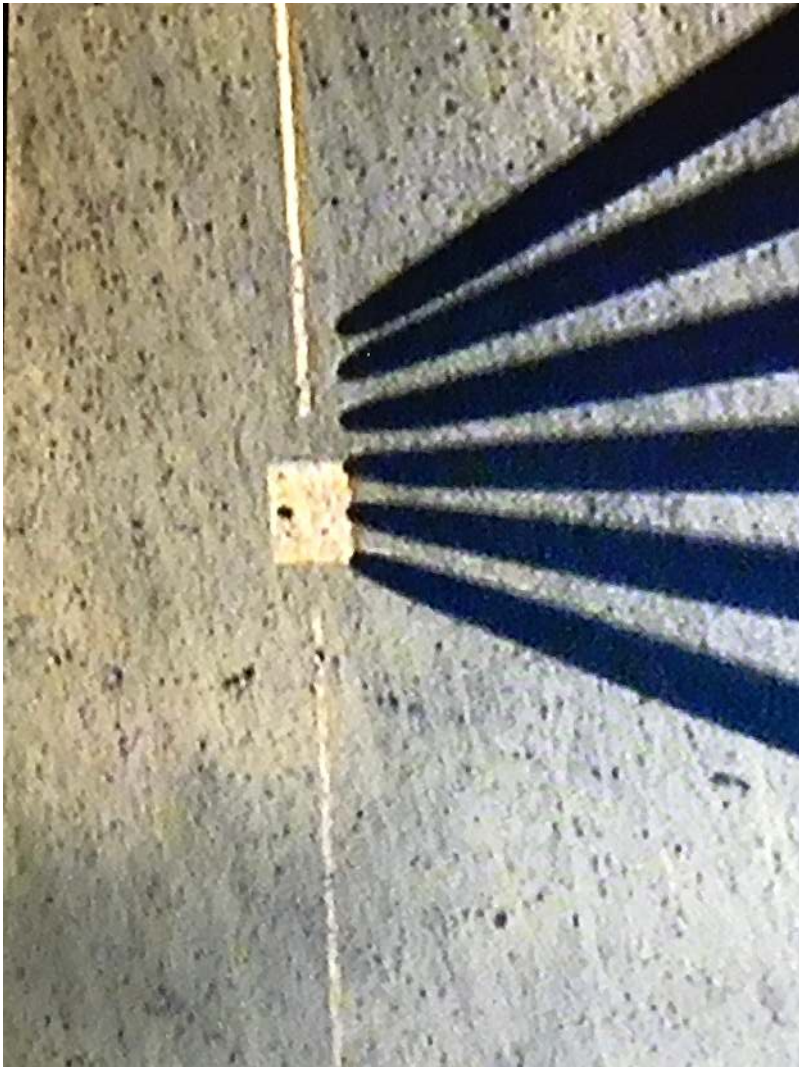
Using RAM Optical Instrumentation Calibration card to estimate probe pitch. The smallest marked square is 0.064 inches. The width of the square decreases by half each step. Below are the three squares below the 0.064square.



0.032in square



0.016in square

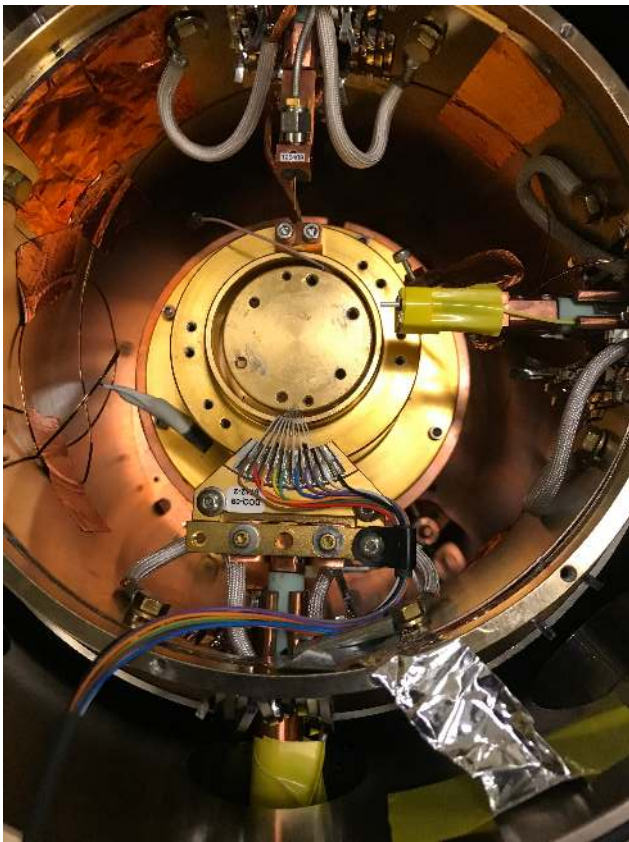


0.008in square

Probe pitch is 100 μ m

Cascade Microtech DCQ-09

Looks damaged.

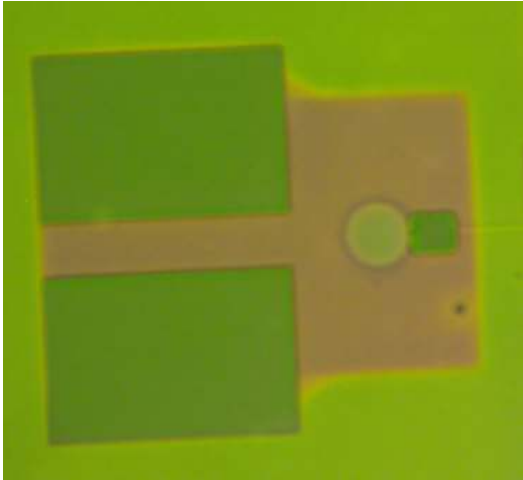


Tri-layer resonator, filter, bias tee, fabrication problems

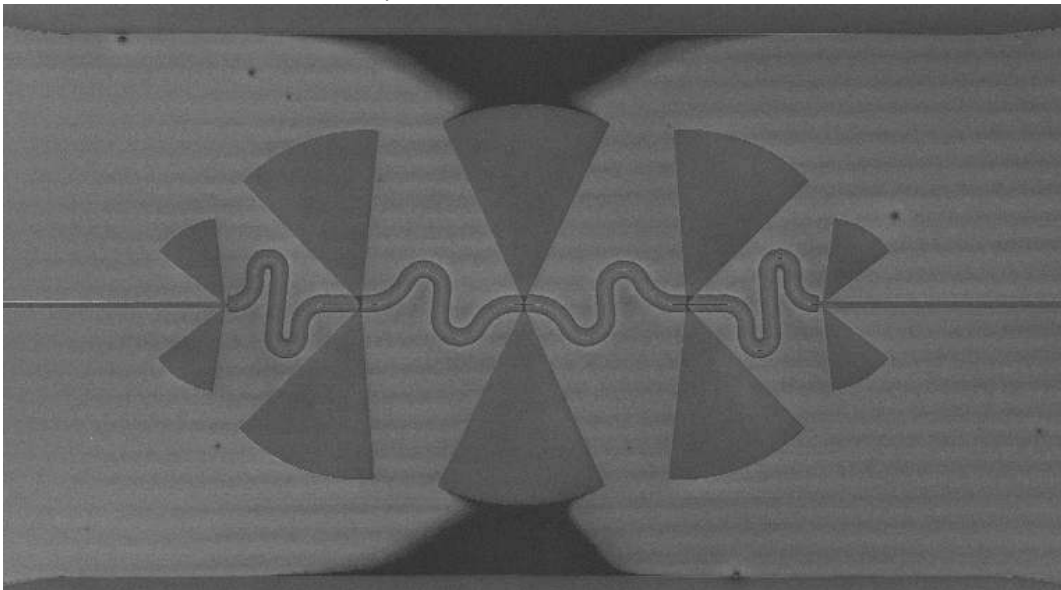
March 2, 2021

Categories: Electronics, Fabrication, Superconductivity

Without PEC

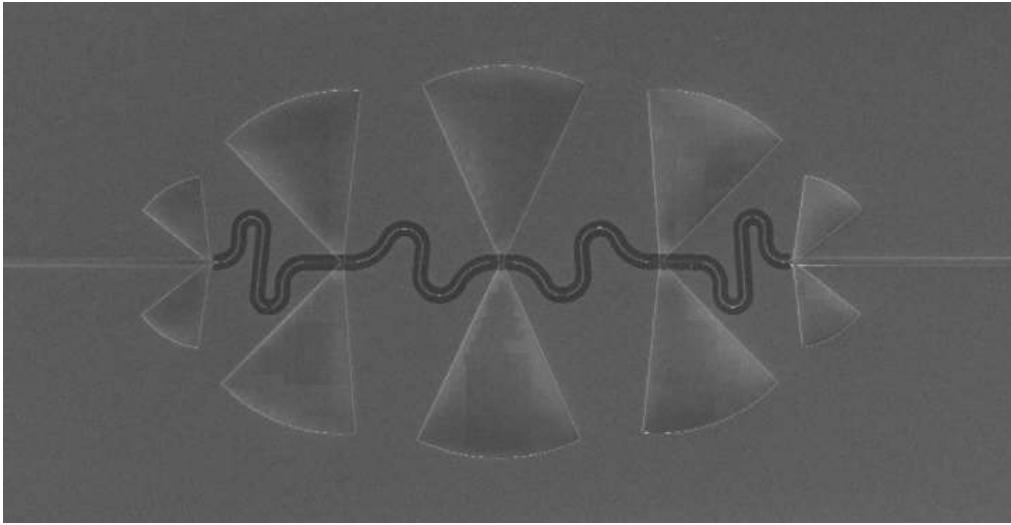


Internal corners are over exposed.

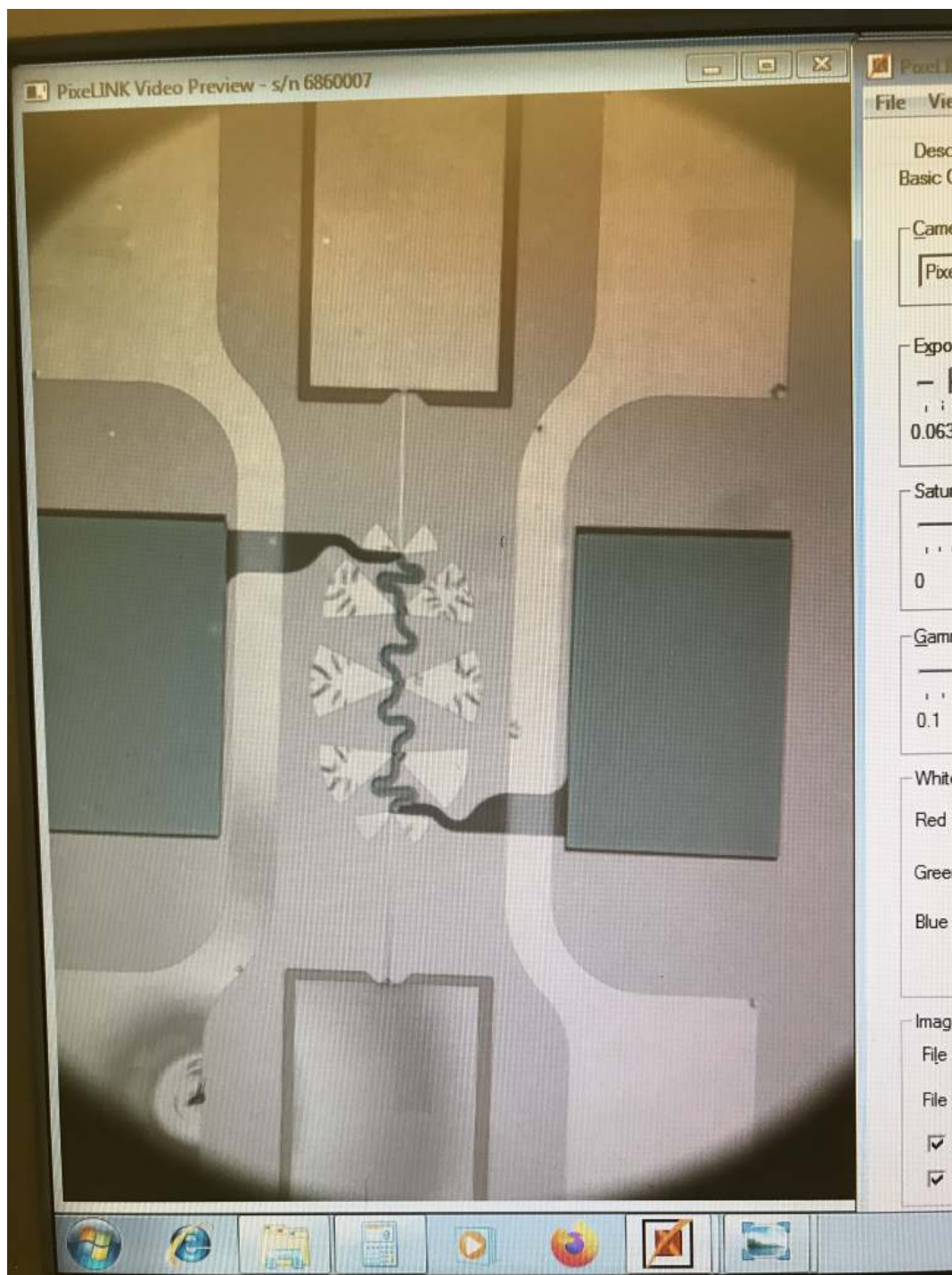


thin spacer is exposed by the device layer step

With PEC



Other problems



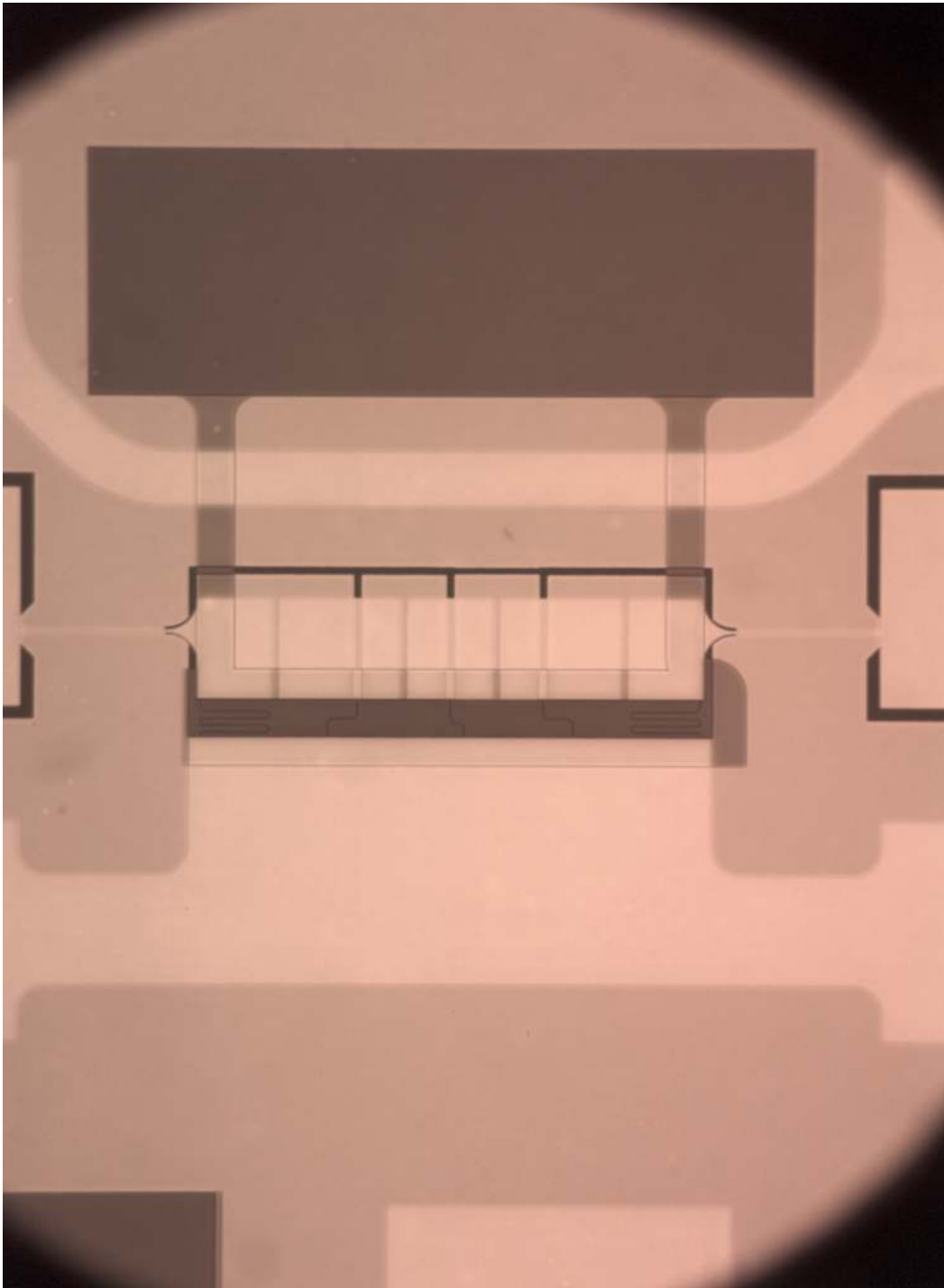
Cracking under NbN device. This appears during the heater process. I suspect it is due to unevaporated MIBK within the 2% HSQ spacer layer. As the film is baked (for ZEP exposure) the MIBK bubbles up through the NbN film. MIBK has a boiling point of 117°C

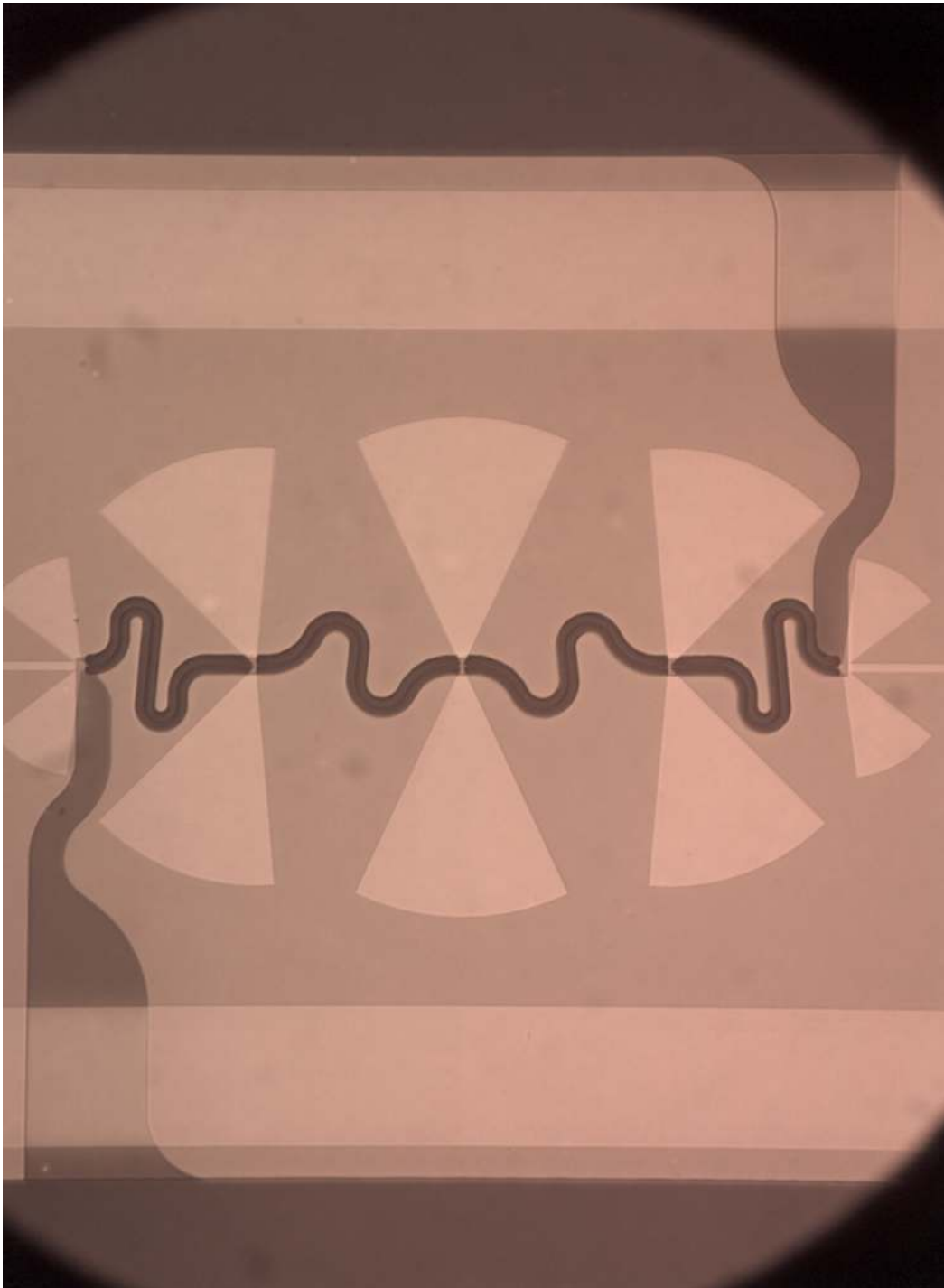


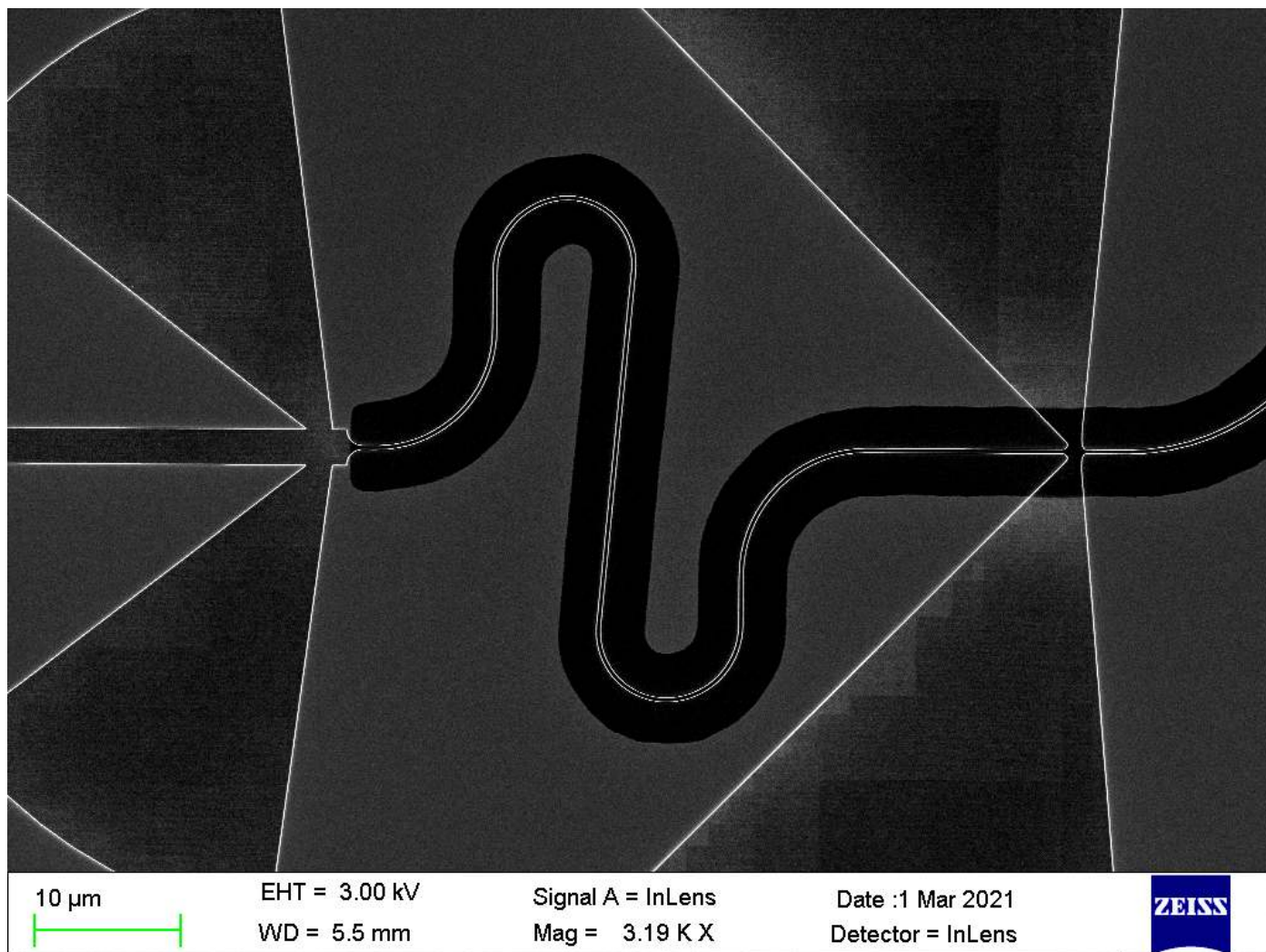
This image is taken after spinning and baking ZEP520 . It is interesting that the bubbles appear primarily in regions where there is large NbN-HSQ-NbN sandwiches. If it is the same stackup but the area of the local region is limited (ie. the smaller bowtie compared to the big one, or the straight sections of the ground Thru compared to the pads) the chance of forming bubbles is reduced.

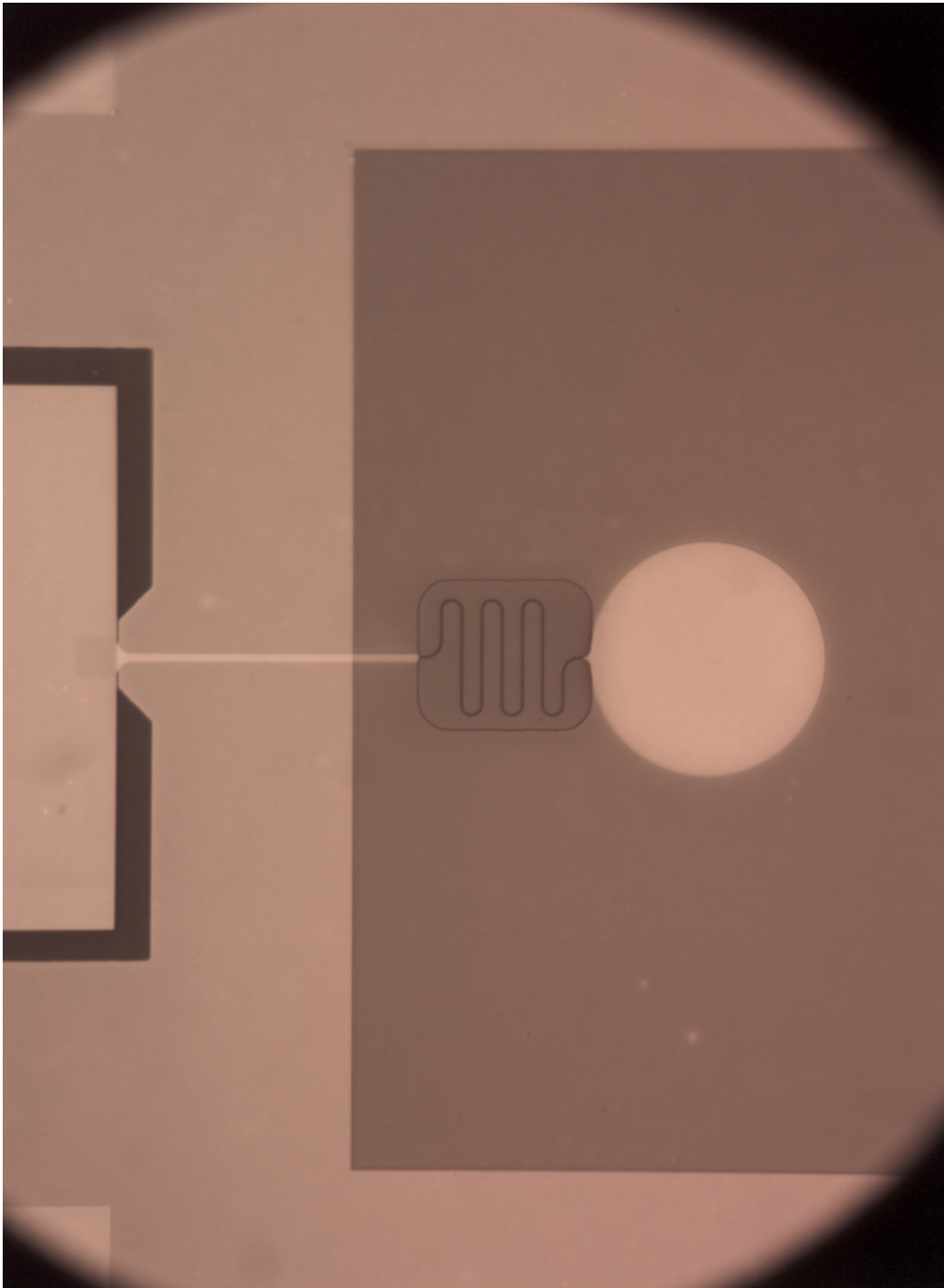
March 2021

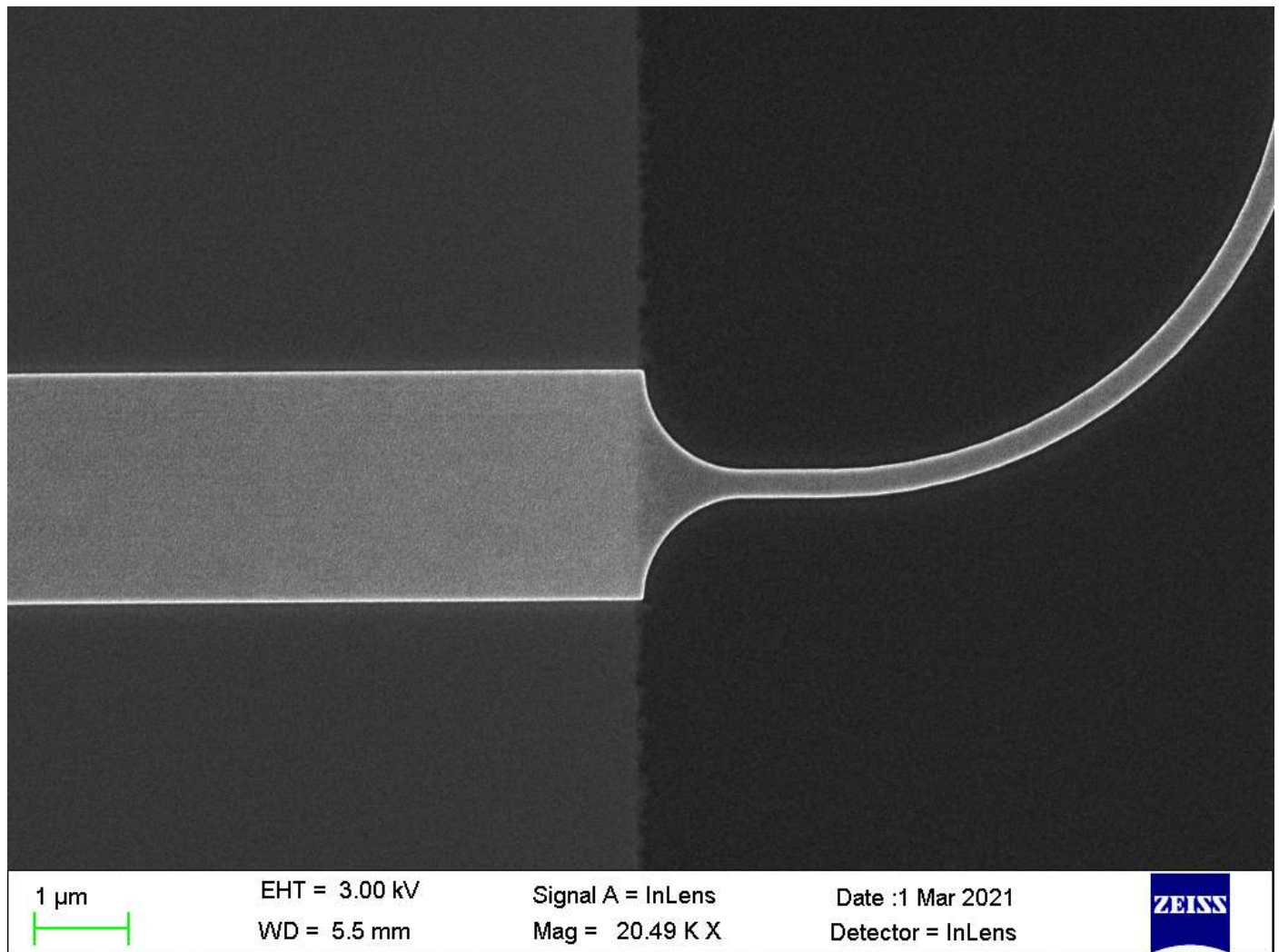
Images taken prior to last ebeam exposure. Everything looking clean. 6% HSQ has been behaving, very few particulates.











Joint between 500hm trace and the inductor in the resonator circuit above.

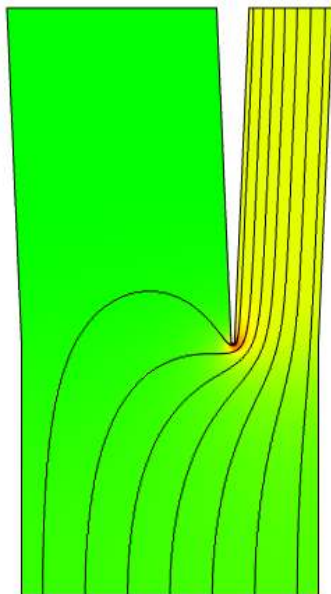
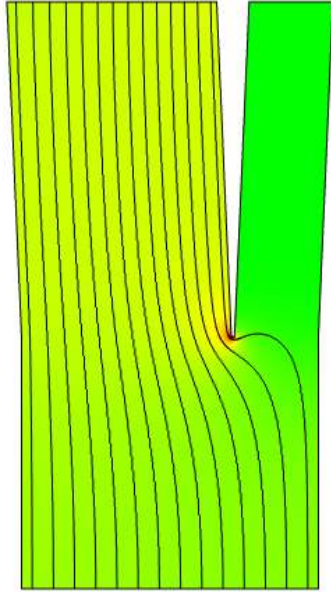
Last Spin of ZEP was a harrowing experience

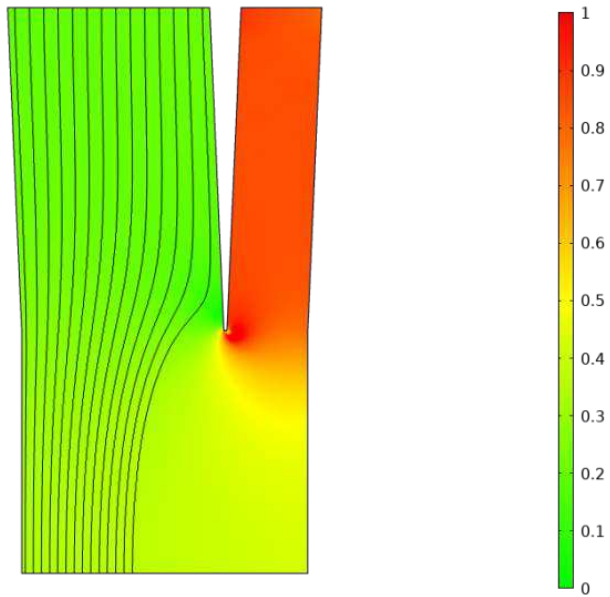
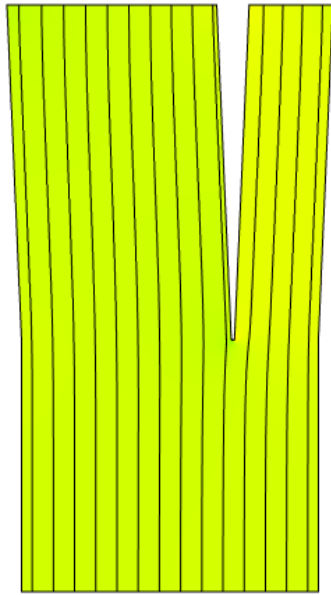
yTron Comsol simulations

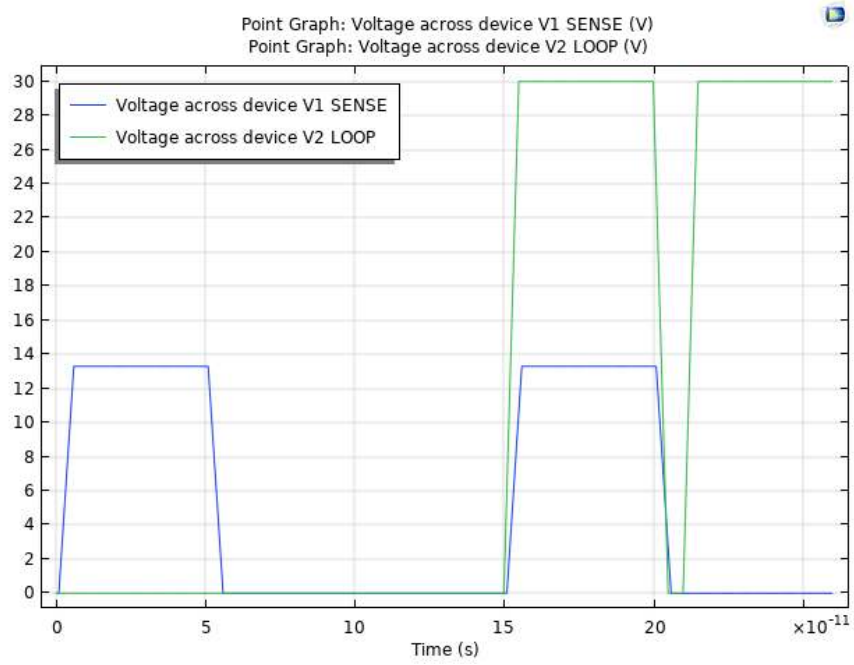
March 24, 2021

Categories: Comsol, Electronics, yTron

Geometry made with phidl. >>pg.ytron_round(rho=0.02, source_length=3, arm_lengths=(4, 4), arm_widths=(2.5, 1))







om_ytron.mph

om_ytron_switching.mph

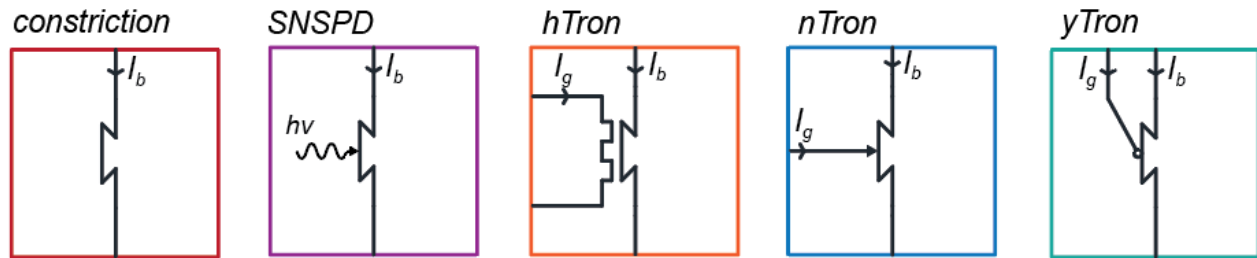
nanowire devices .ai file

March 25, 2021

Categories: General, nMem, nTron, SNSPD, Superconductivity, yTron

illustrator drawings of nanowire devices

constriction, snspsd, hTron, nTron, yTron



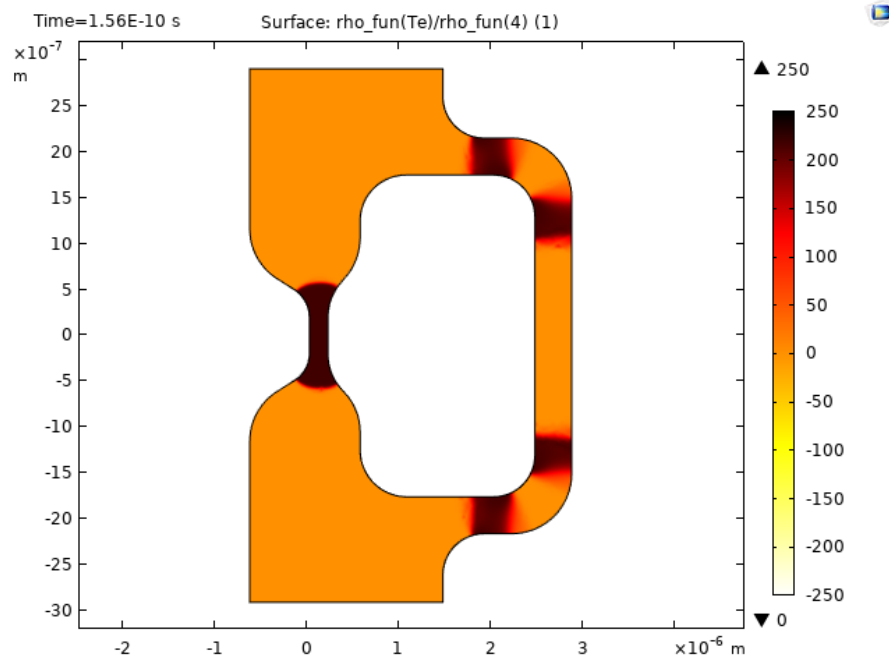
nanowire_devices.zip

nMem comsol simulations: two-temperature model

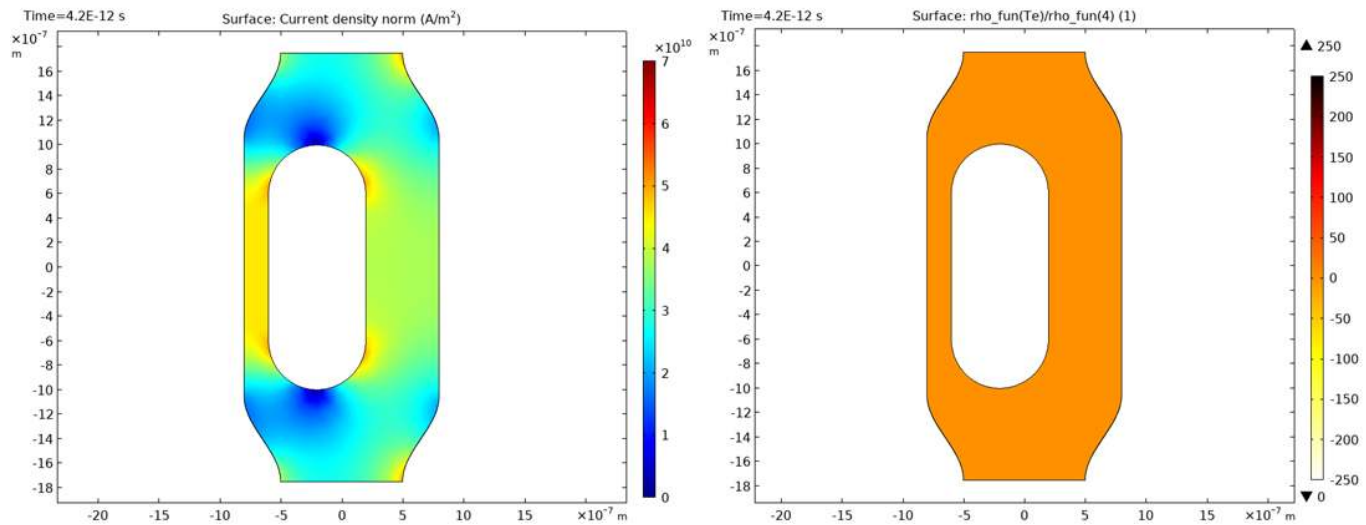
March 28, 2021

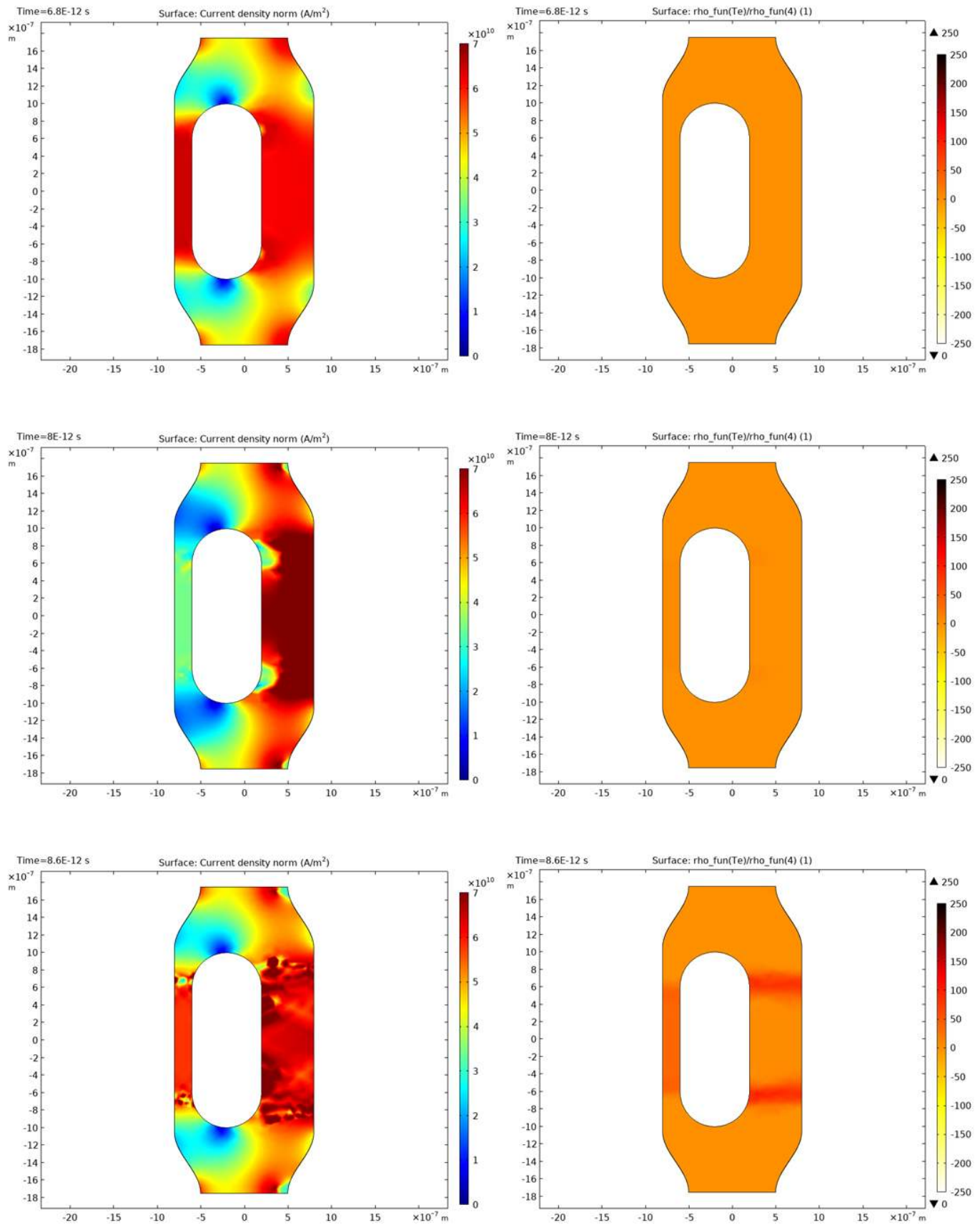
Categories: Comsol, Electronics, nMem

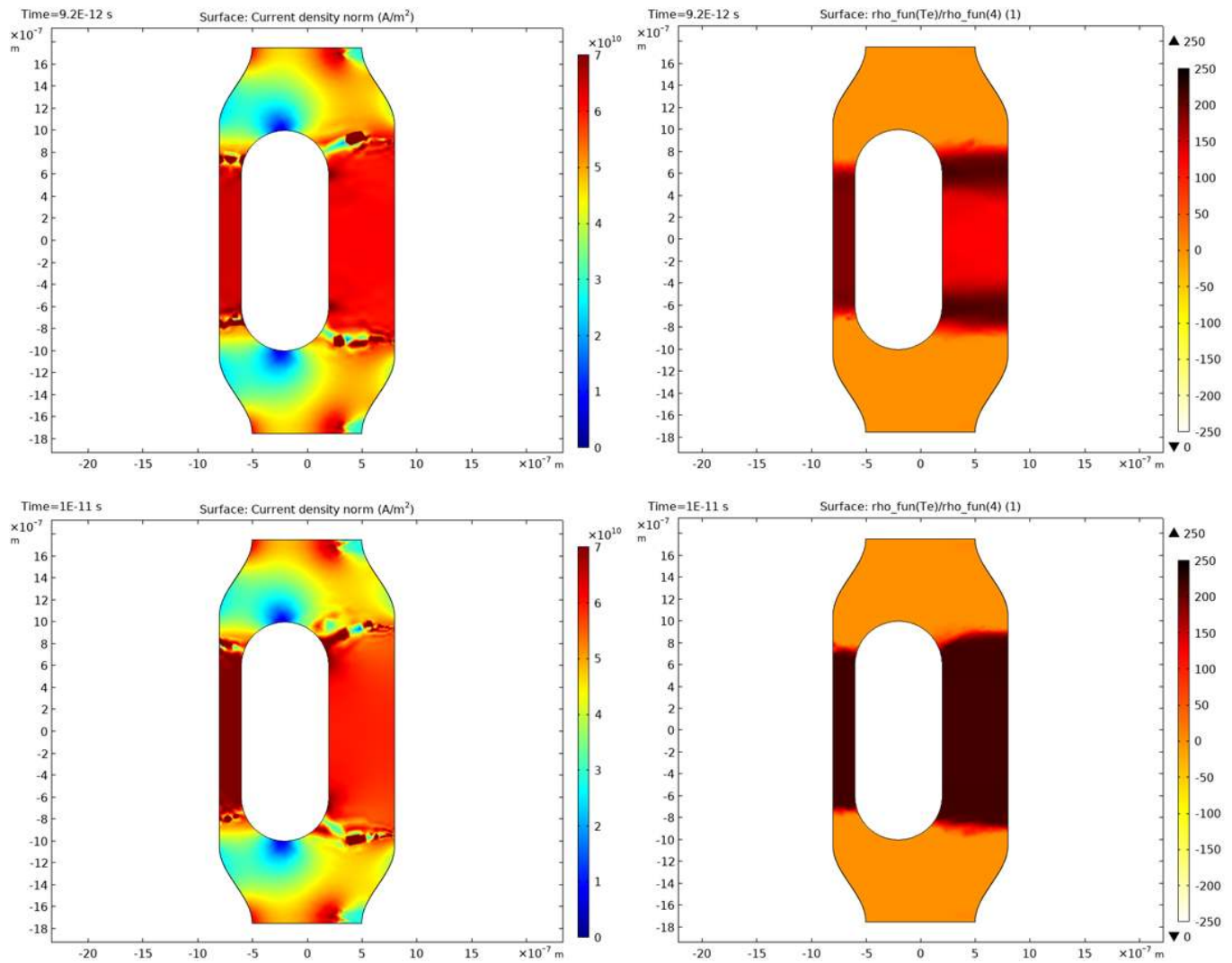
Old cell has corners switching, which makes analysis difficult. I will create a new geometry.



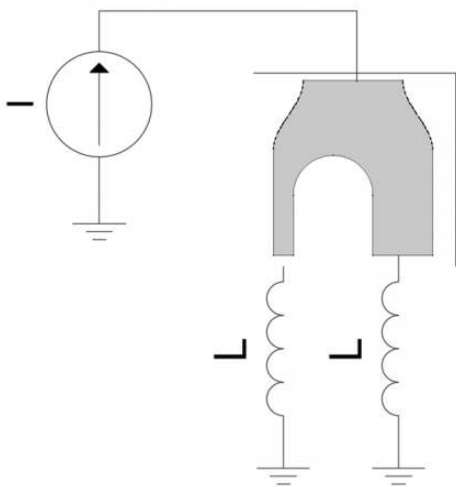
new design switched at 1.8e-11 seconds. That was at the plateau of the input pulse of 50V.







It is interesting to see that the current jumps to the right side before any switching occurs. But the main problem here is that there is no inductive splitting.



The above geometry did not work. Likely because my L/R time constant was too big.

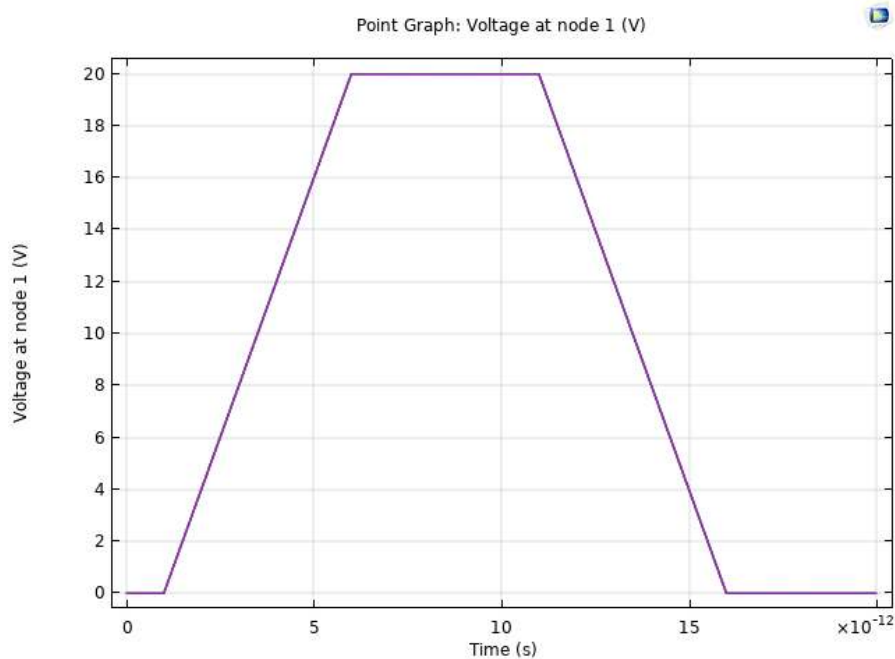
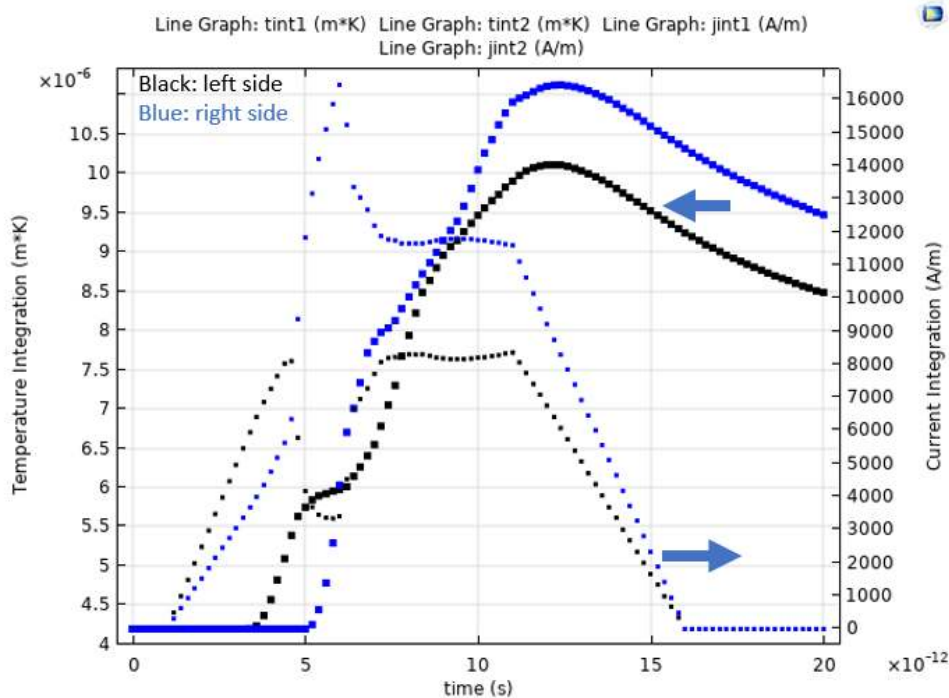
<https://www.comsol.com/forum/thread/48629/inductive-sheet-impedance-in-transient-simulation>

<https://www.comsol.com/forum/thread/230792/kinetic-inductance>

<https://www.comsol.com/paper/understanding-the-magnetic-field-penetration-in-mesoscopic-superconductors-via-c-18481>

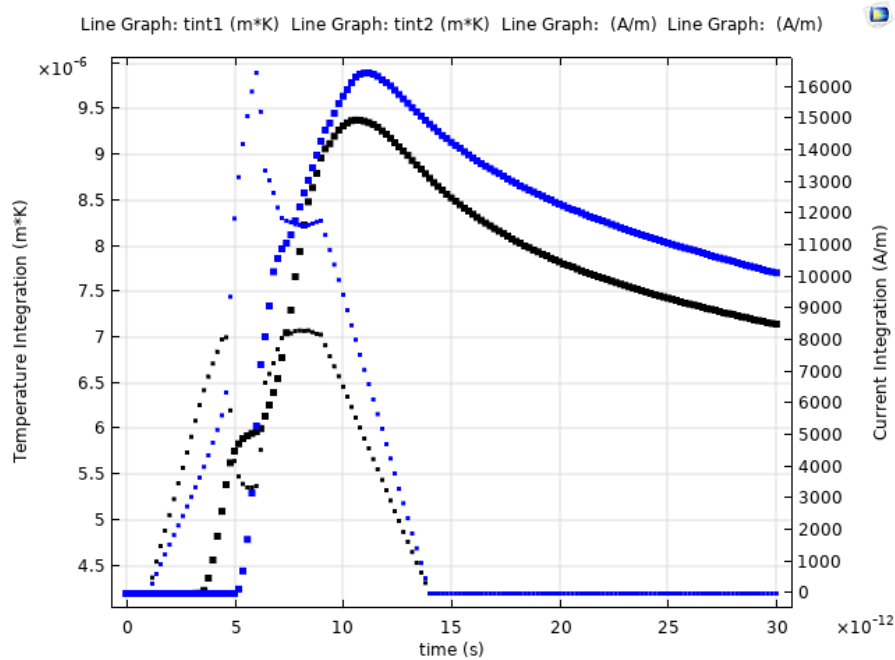
<https://aip.scitation.org/doi/10.1063/1.4848015>

New geometry... again. This time I wanted to make sure that the switching event was confined as possible. The plot below shows the spatially integrated electron temperature and current density. The colors distinguish the left and right branch of the memory. For the temperature integration, a line was drawn through the center of the branch. For the current integration, the integration was performed over the cross section of the branch. Each line used for the integration is visible in the animation below.

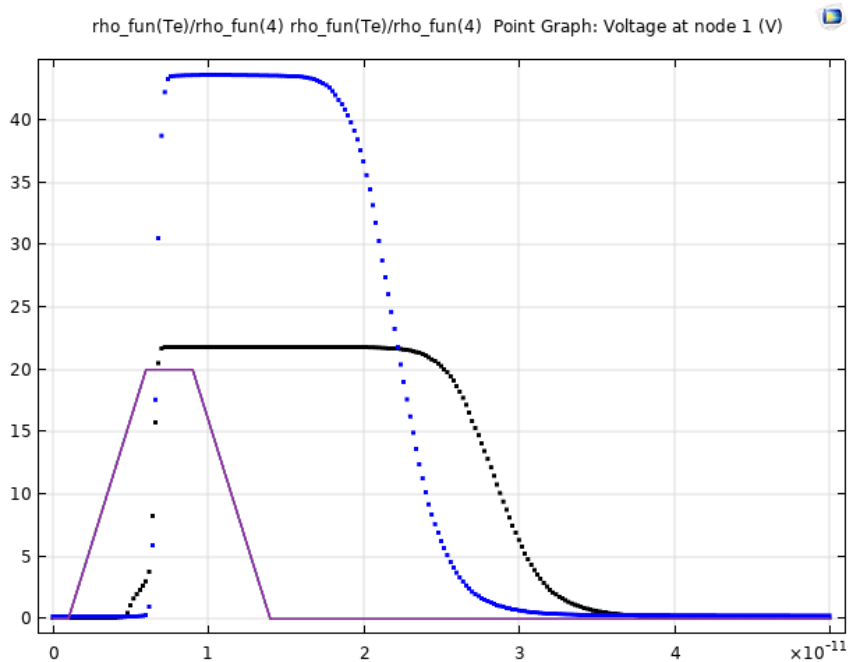


Some current splitting is visible in the simulation above. Likely because of the longer path from branch to branch, the slight increase in resistance is enough to divert the current, unlike the previous geometry that had similar path lengths from left to right.

I used the same settings but ran the simulation a bit longer to see how the temperature decayed. Looks like the electron temp is still quite high despite the device returning to a superconducting state.

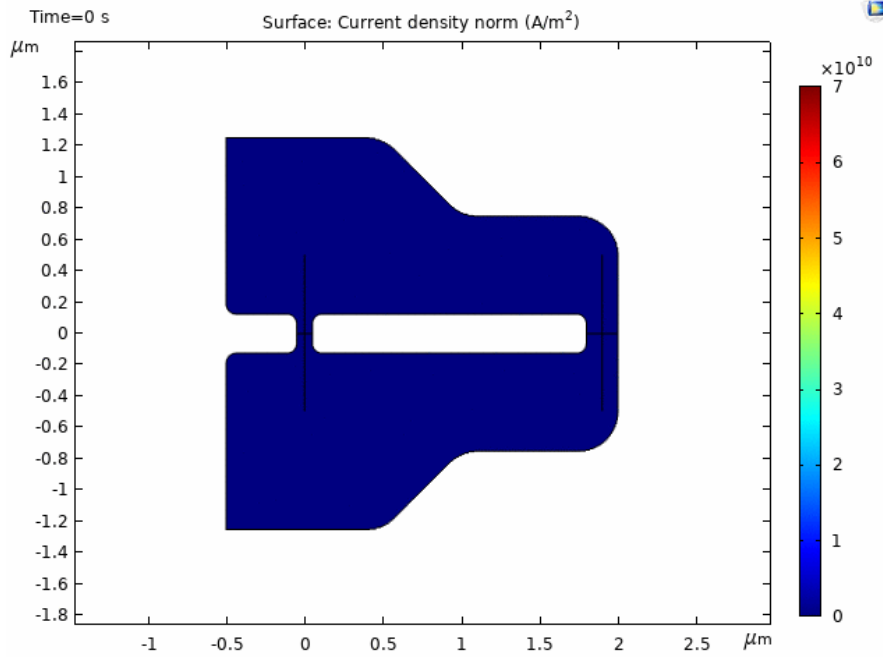


The plot below shows that the devices reset even though the temperature is still quite high. If it returns to a superconducting state it needs to dissipate heat much faster I would think.



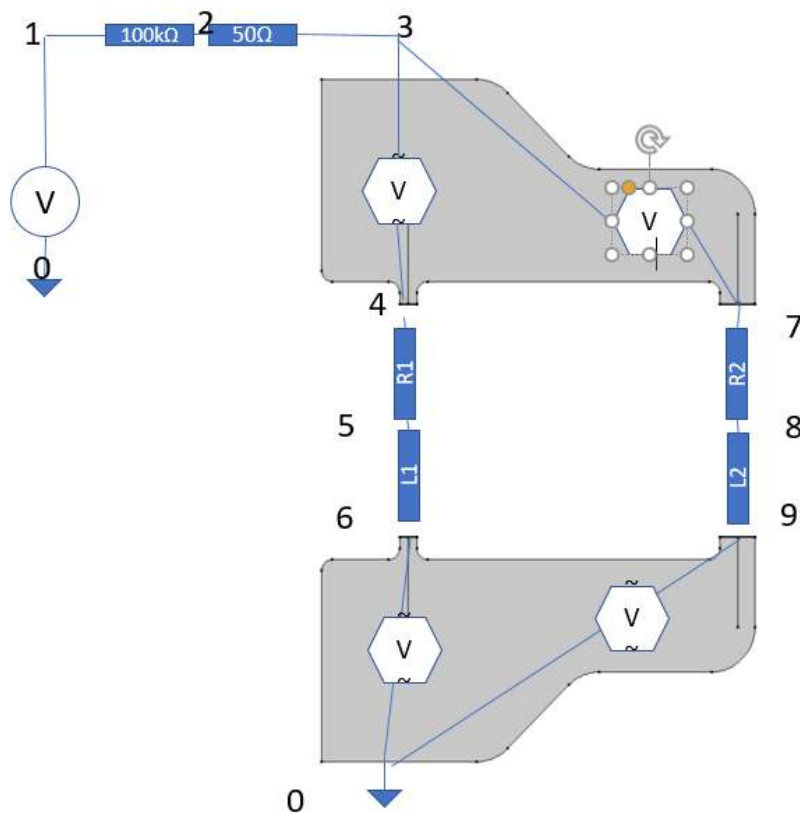
Tried to improve thermal dissipation into the substrate by creating a 3D model. I was unable to get the model to converge in a reasonable period.

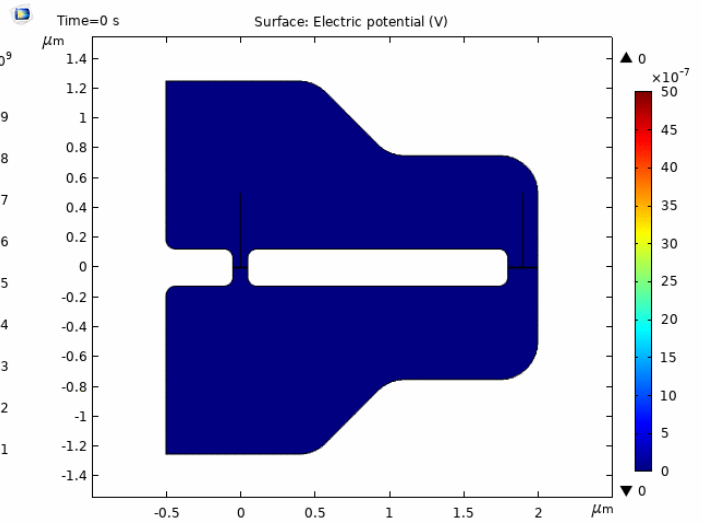
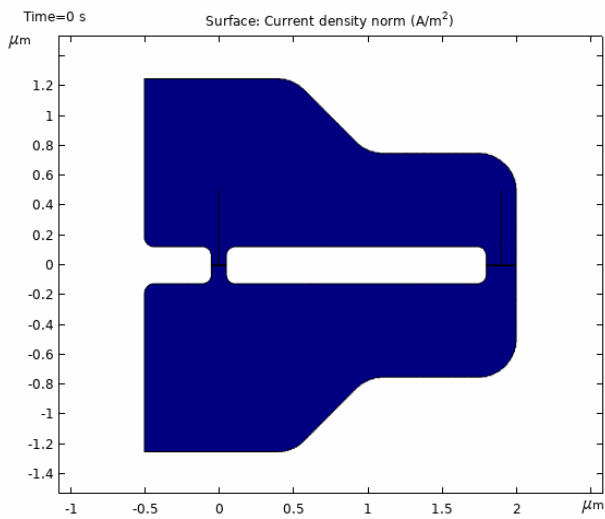
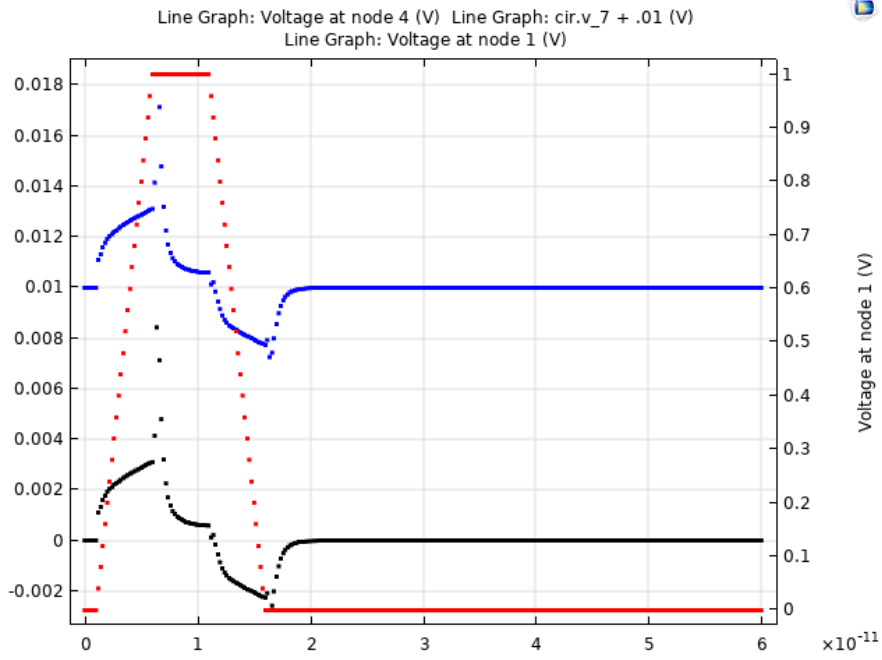
[nMem_thermal_cell_param_20210328.mph](#)



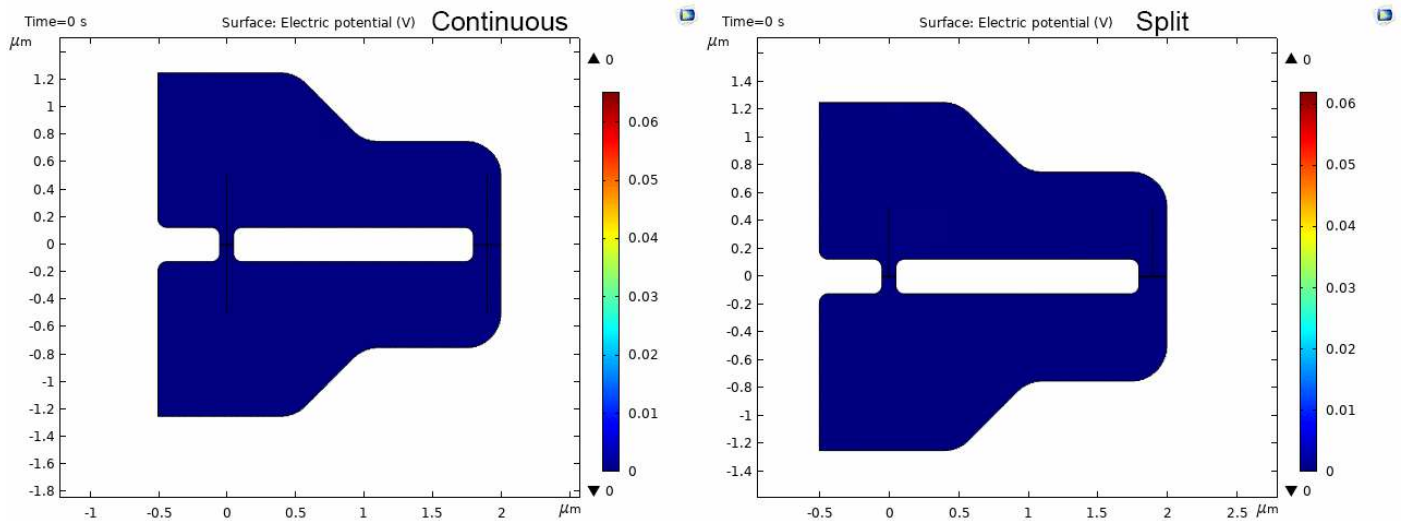
In order to get the inductive splitting I added two spice "nanowires" inbetween the branch and set the R, L values to

calculated values based on classical film properties.





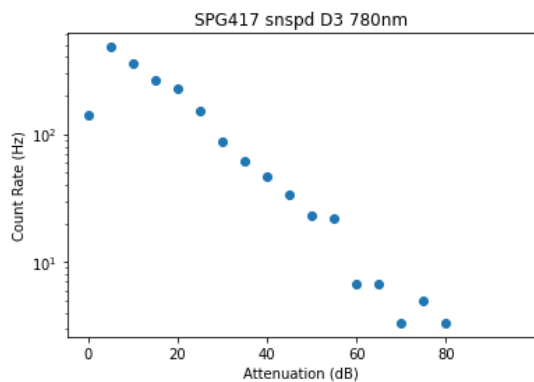
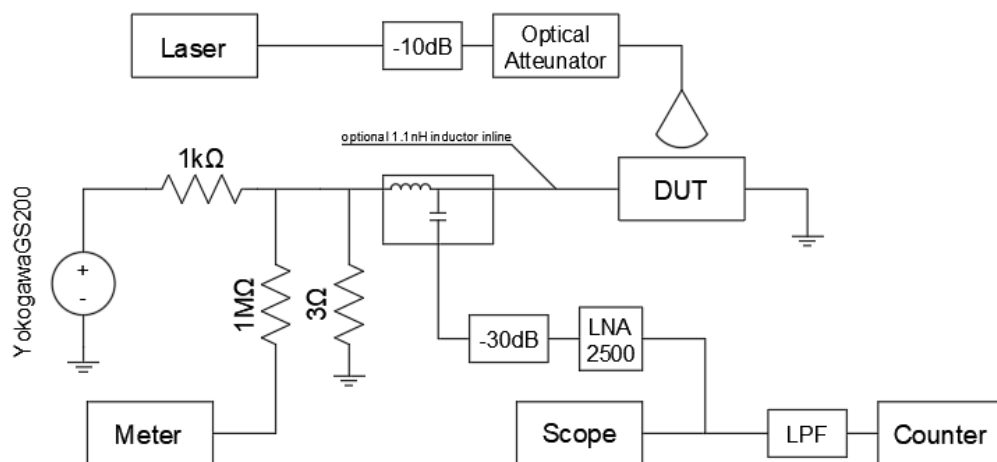
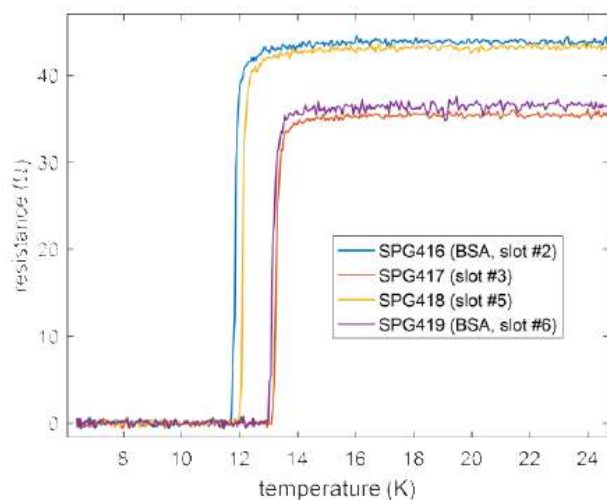
Because of the strange current density in the plot above I wanted to take a closer look at splitting the model. Below is a plot of a continuous (original and unsplit) geometry and a split (but with no SPICE elements in-between, ie just shorted) geometry. Ideally they are identical. There is a difference during the rising voltage bias but the decaying nature is the same. There is a temperature boundary condition that asserts the same electron, phonon temperature at either side of the split.

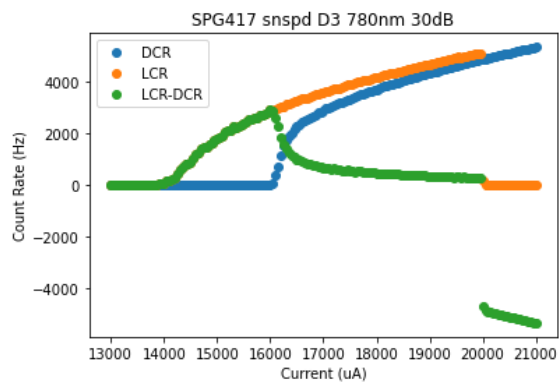
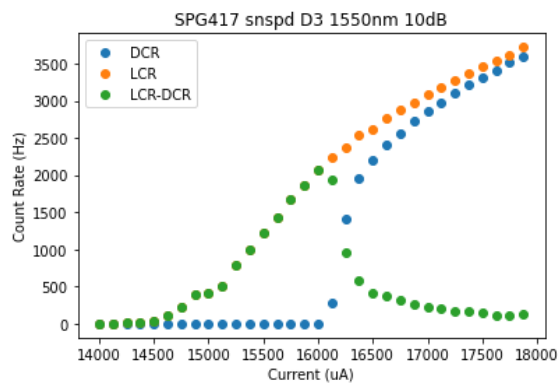


SPG417 wide wires on 30nm high Tc film (AED colab)

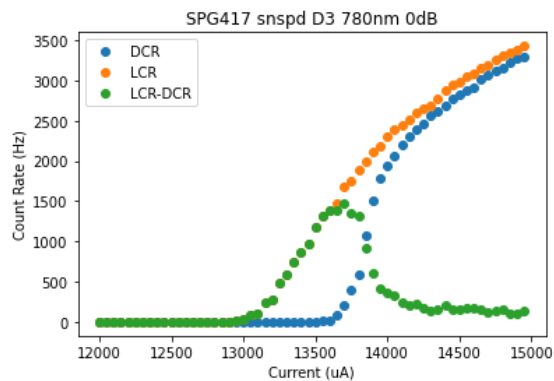
April 7, 2021

Categories: General

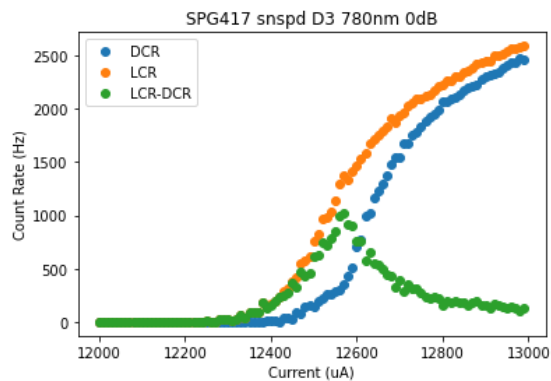




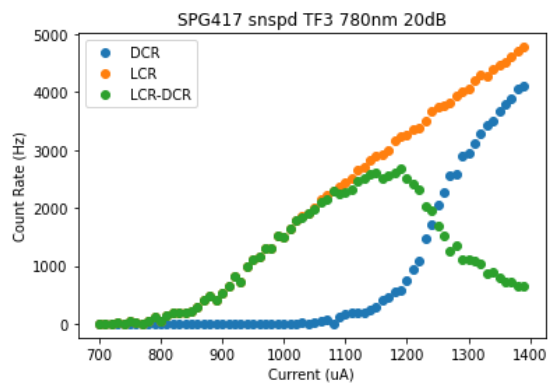
2.5 μ m wide detector Actually -40dB there is a 10dB attenuator inline. T=1.3K



T=4K



T=5K



100nm wide 10 μ mX10 μ m detector

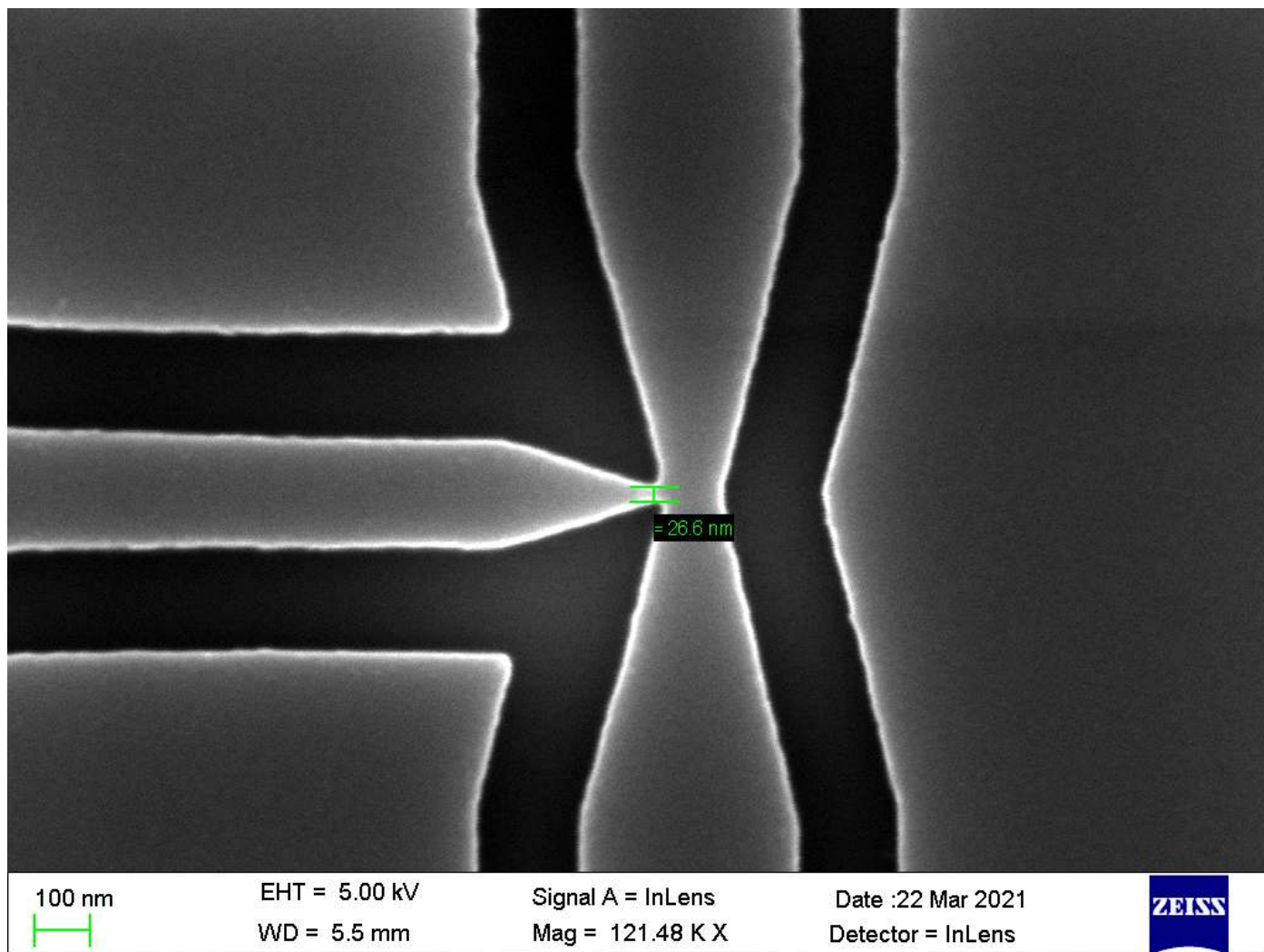
Same layout as SPG371

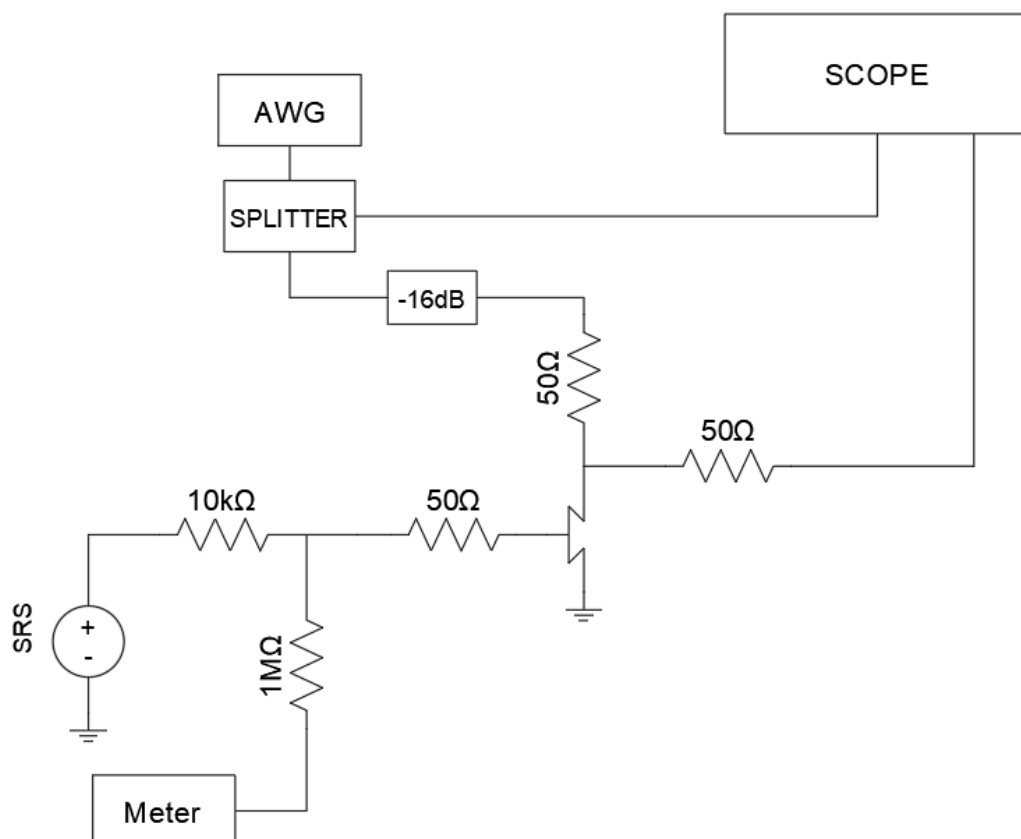
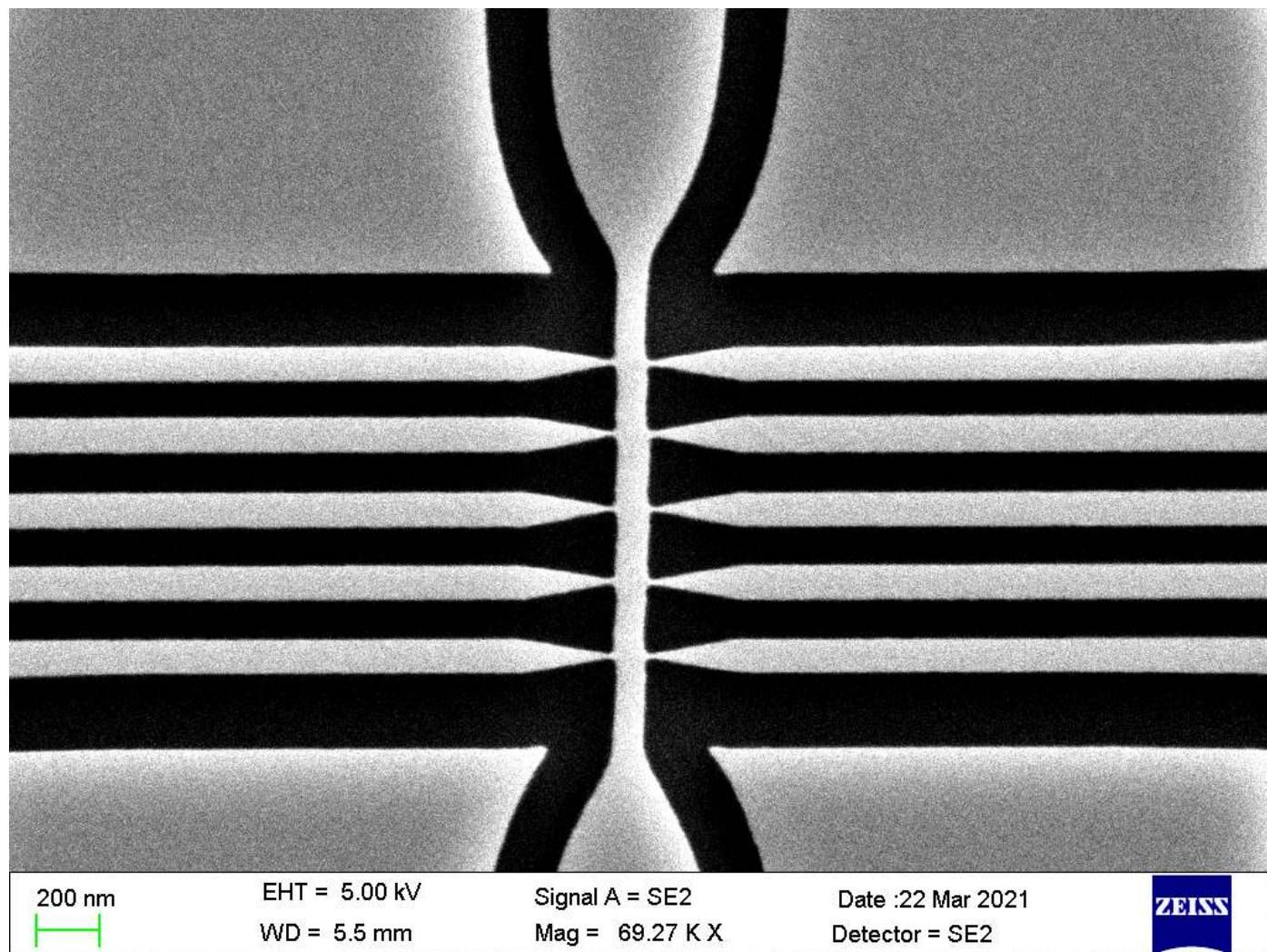
SPG371_2020-11-19 10-05-34.gds

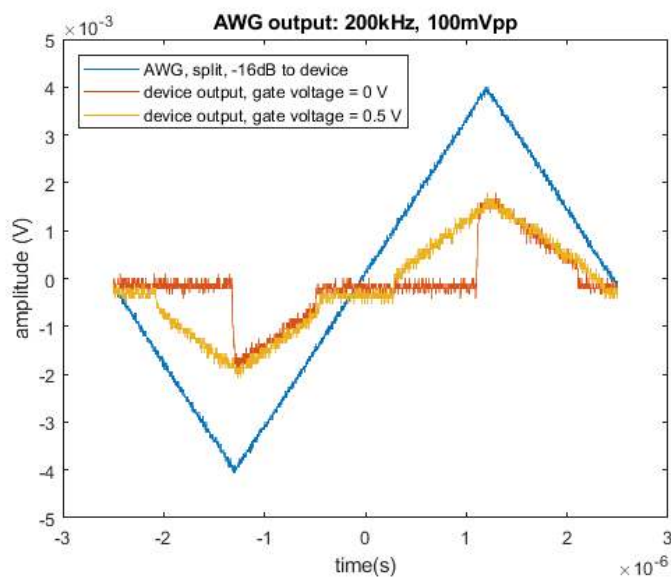
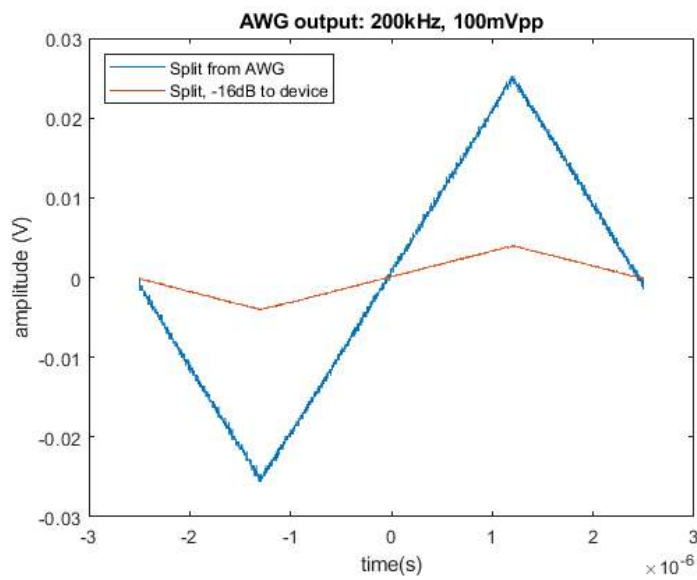
SPG432 nTron measurement

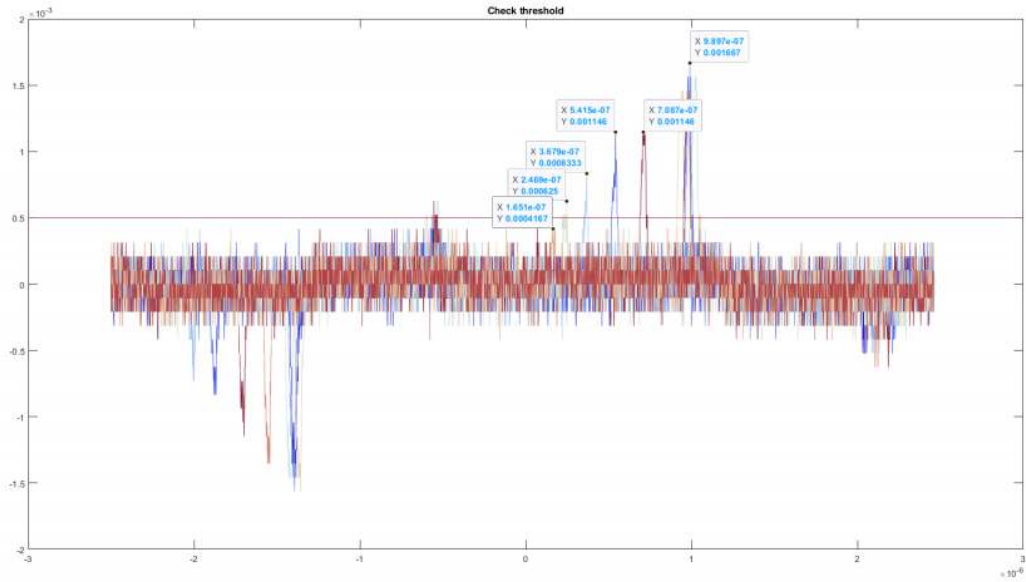
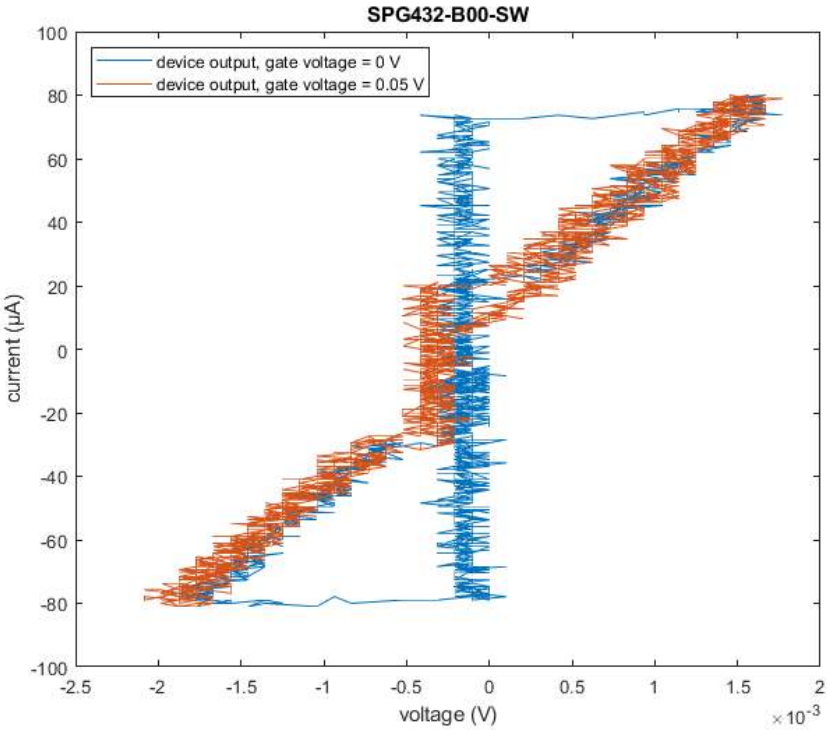
April 14, 2021

Categories: General

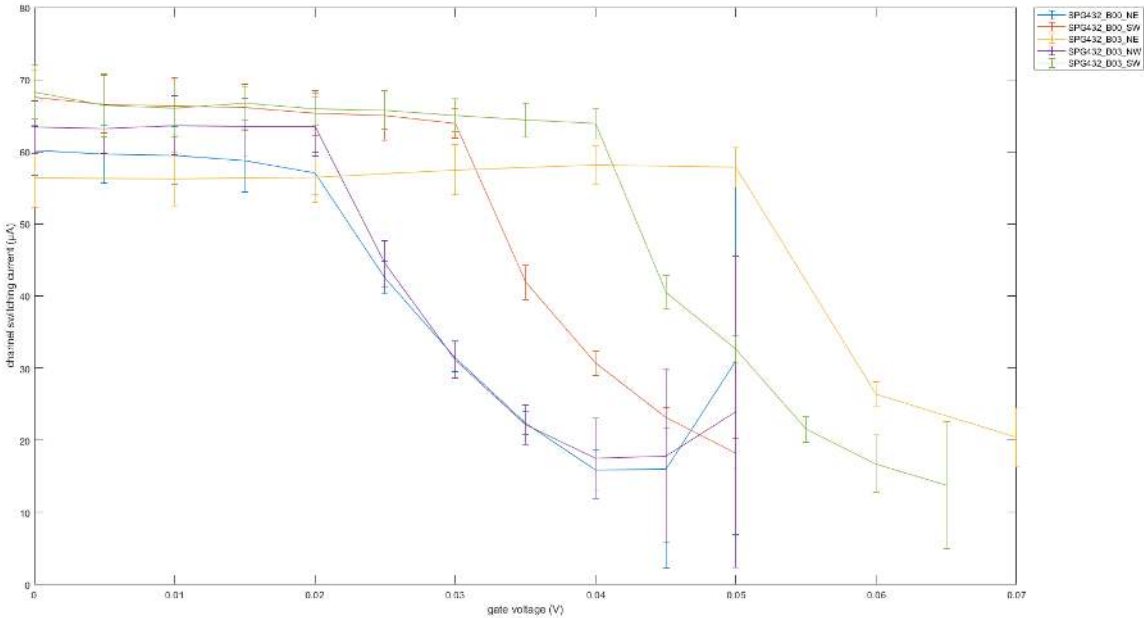
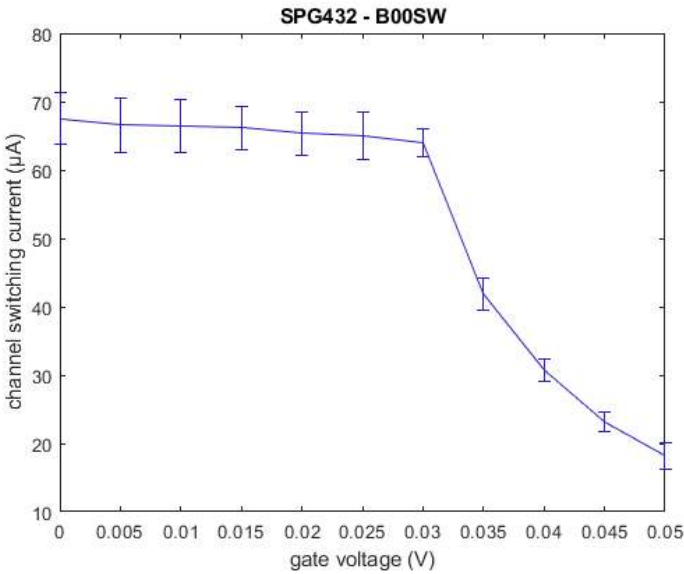
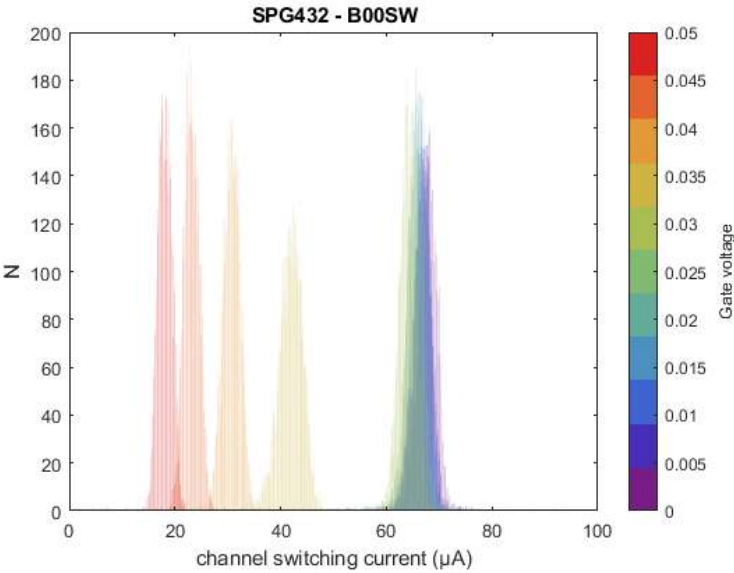


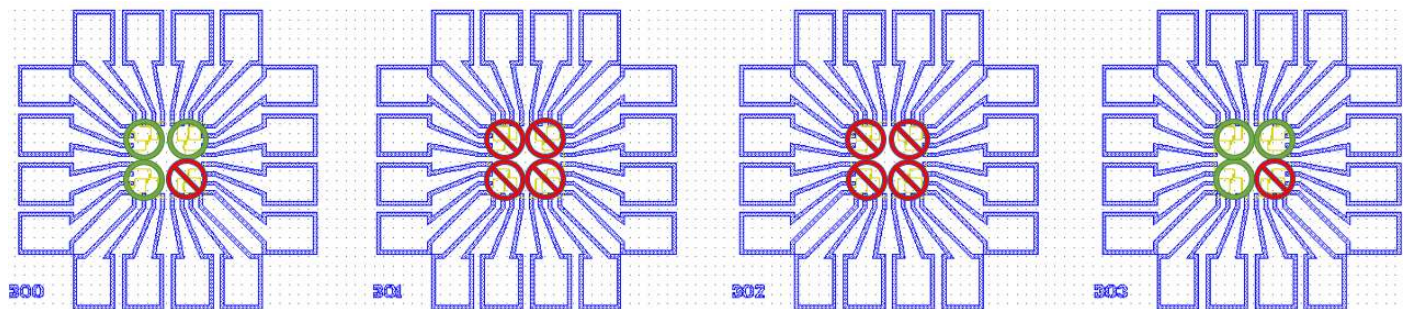
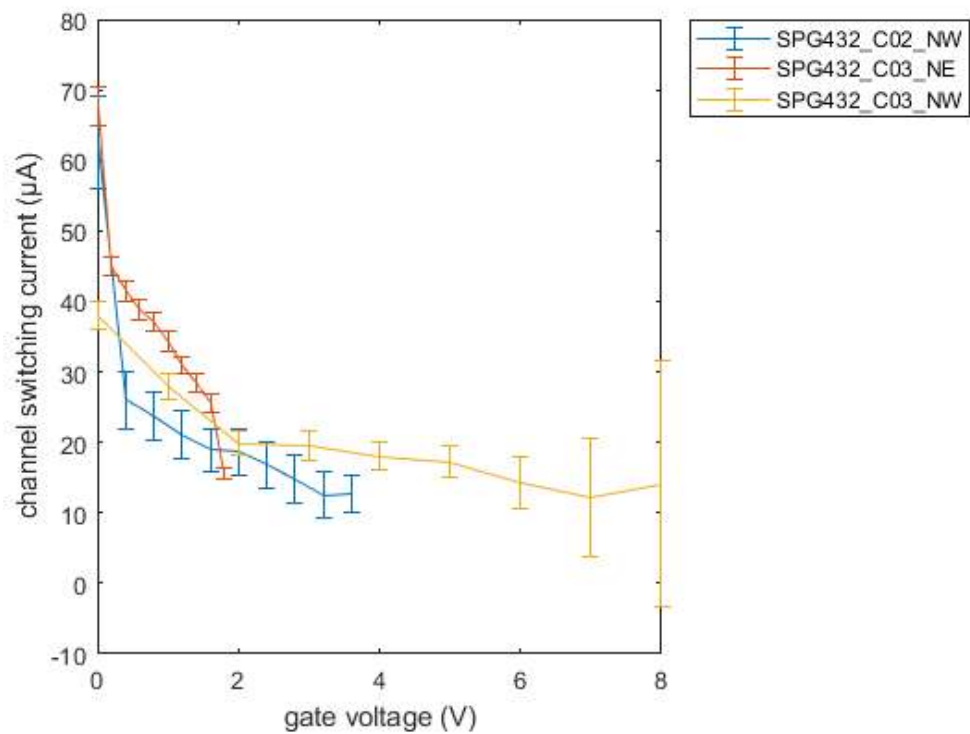






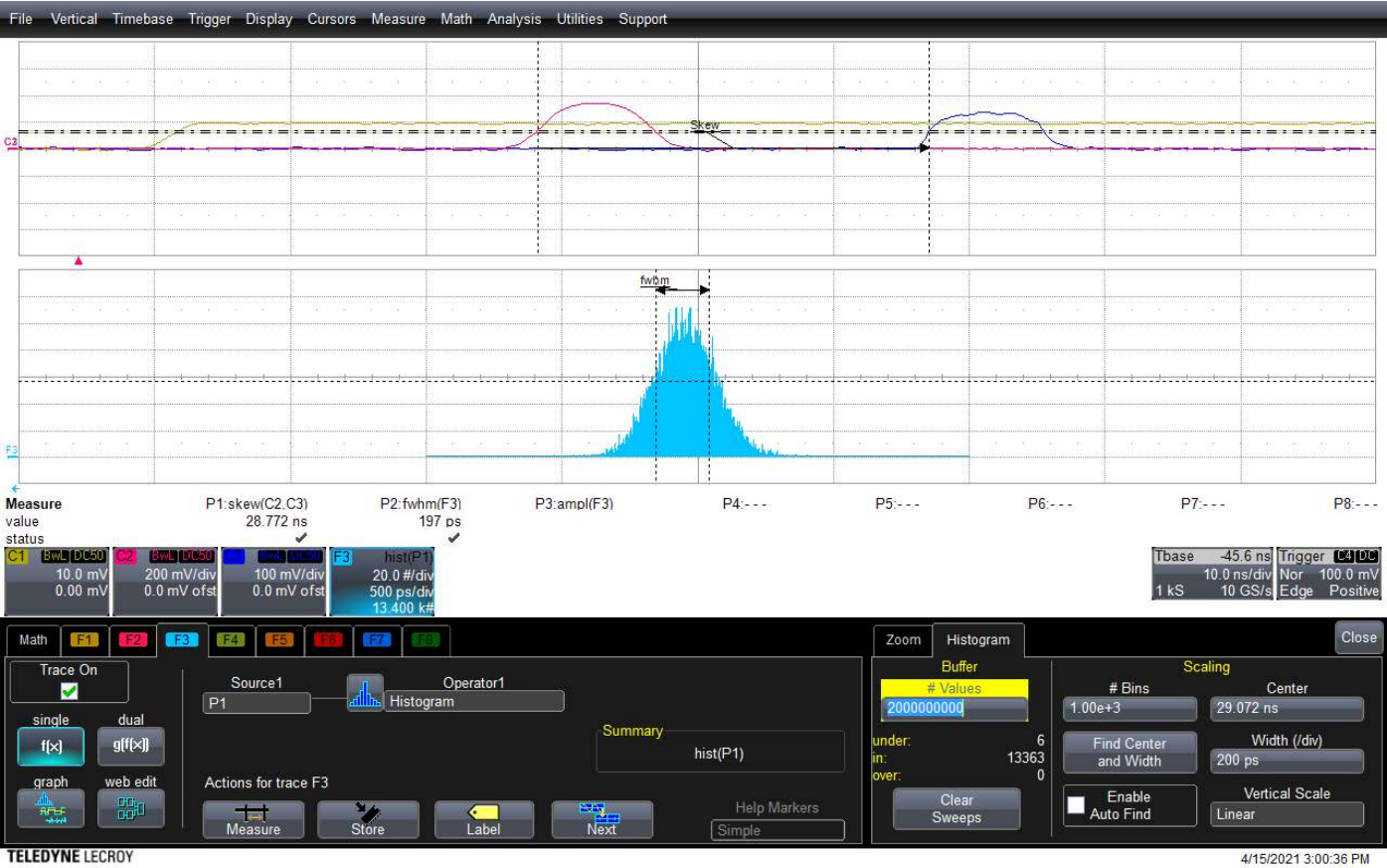
B00_NE



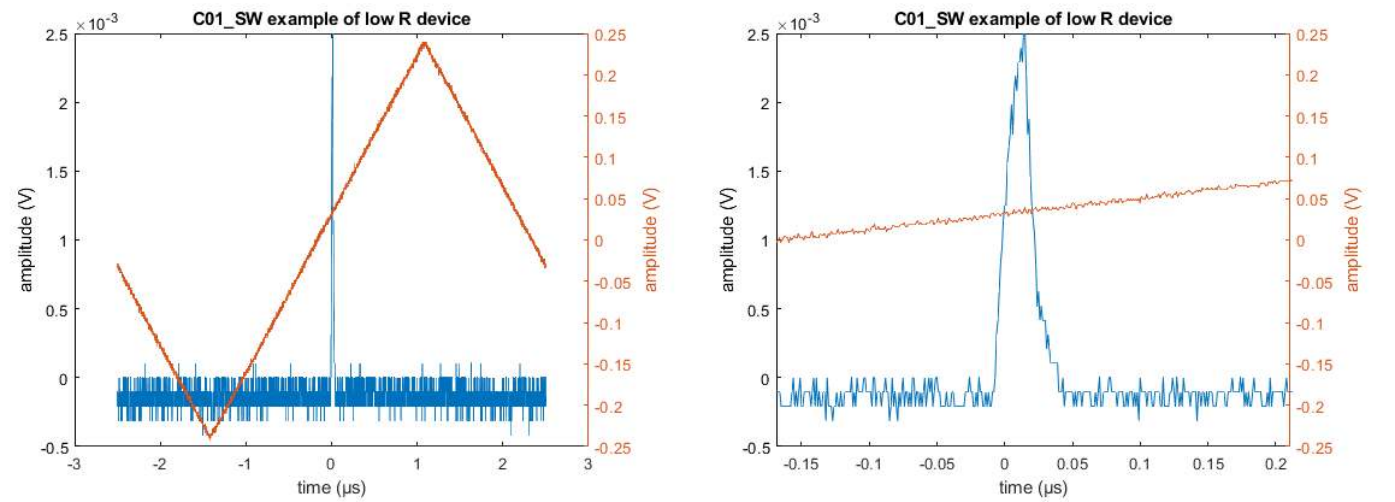


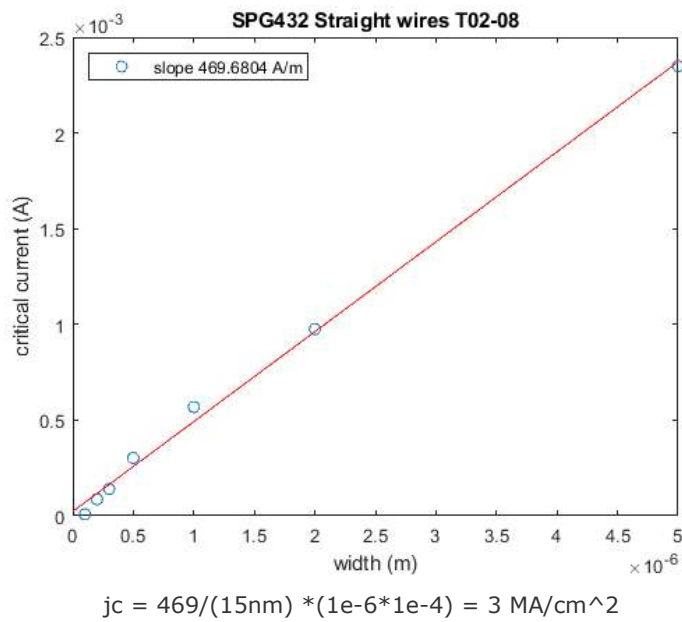
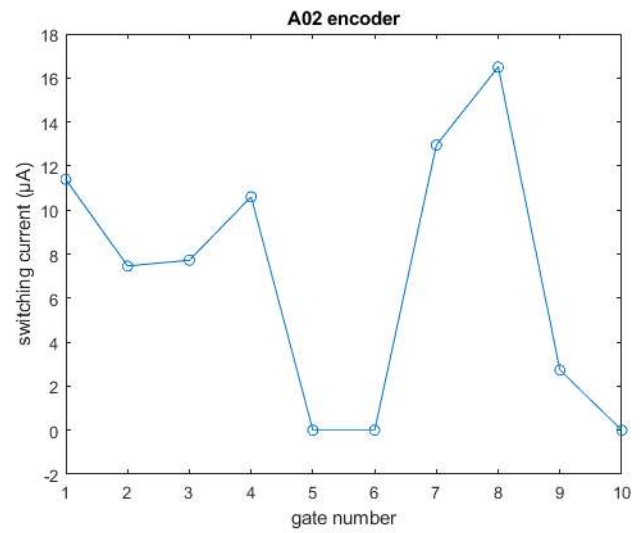
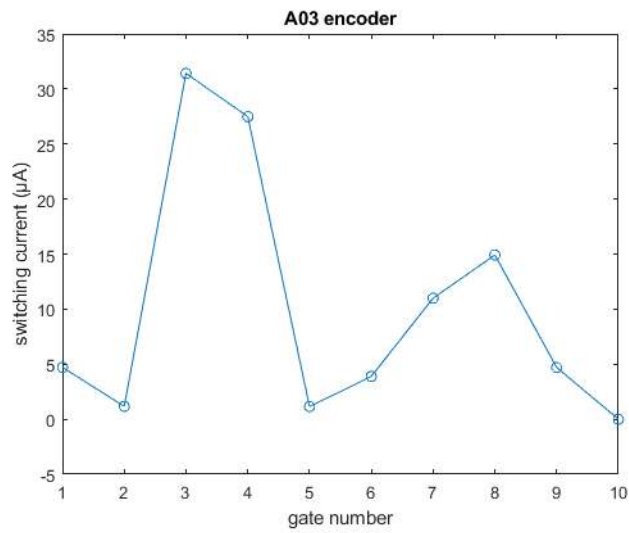
Elionix was not calibrated. Major stitching issues.

[Elionx stitching issues.pdf](#) saving here to recall date if needed.



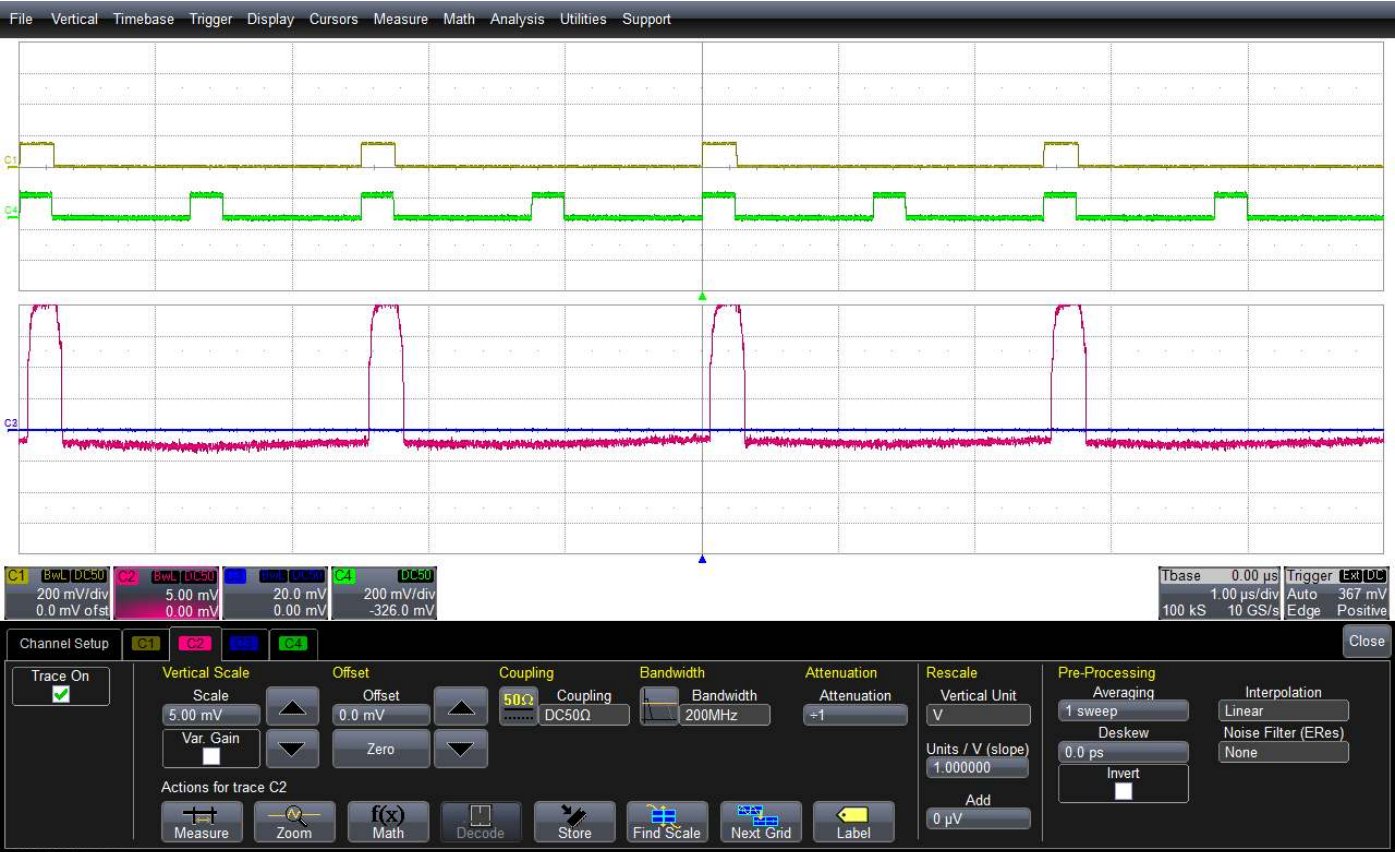
Bad devices produce the following traces:





Logic Gates

AND

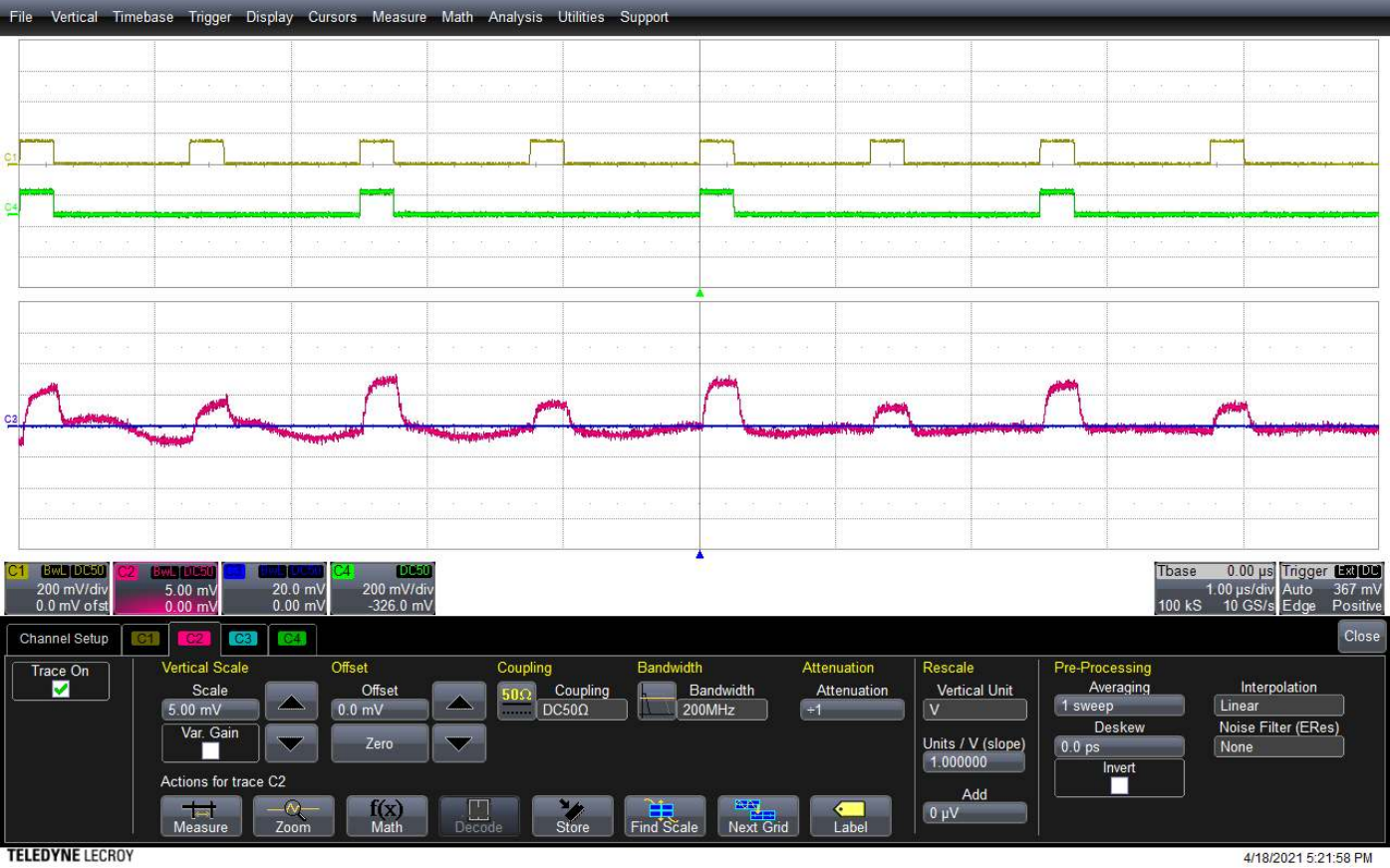


200mV(-40dB) input

OR



300mV(-40dB) input

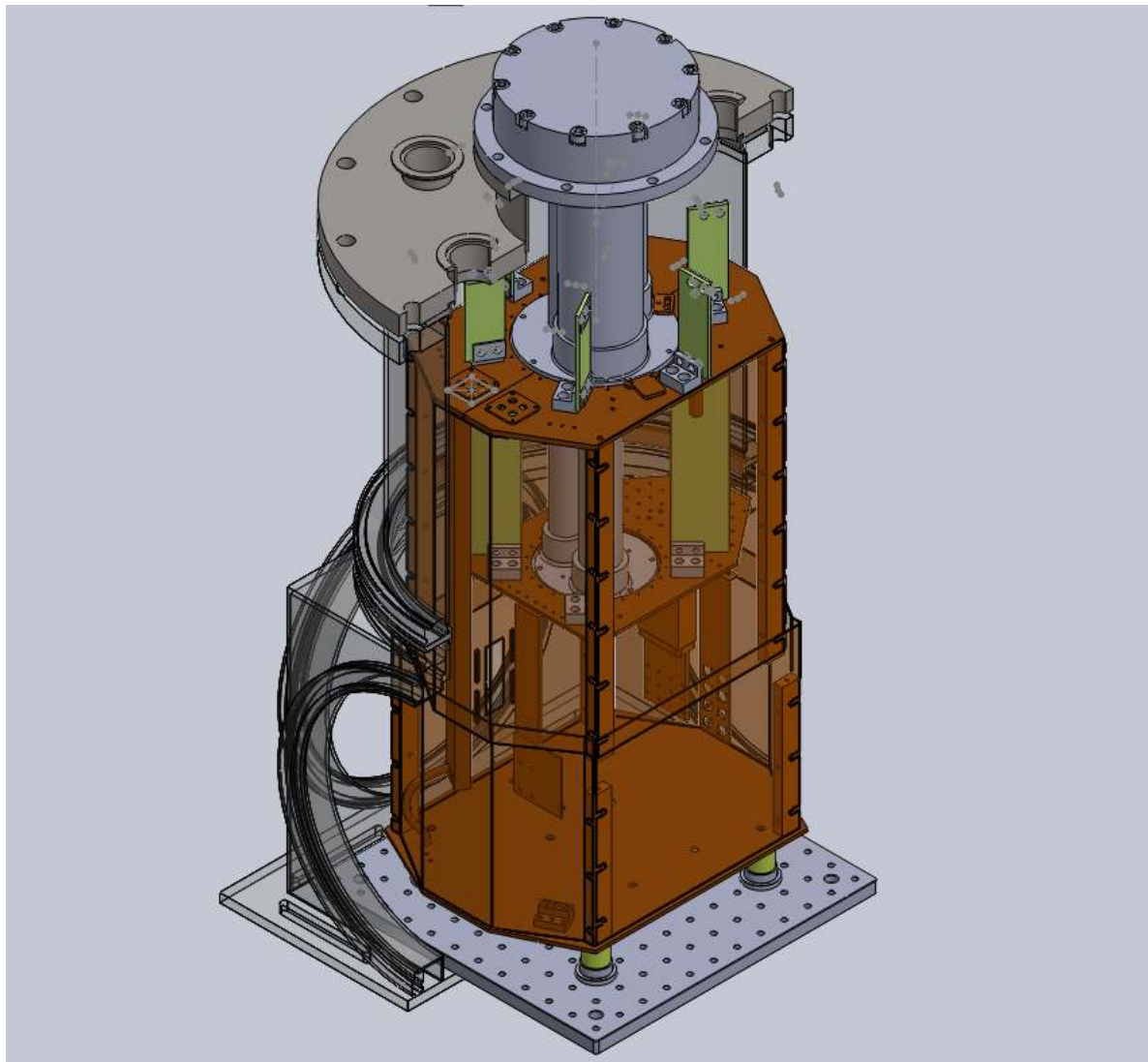


Free Space Cryostat Updated Model April 2021

April 19, 2021

Categories: Cryostat

The bottom connection to the breadboard is inaccurate. I could not find the correct model and seeing as that is what we are looking to replace I did not create new models of that area.



[Link to previous post](#)

[2021_updated.zip](#)

AJA Sample Database phpMyAdmin Guide

June 9, 2021

Categories: General

LINK: <http://qnn-nas-rle.mit.edu/phpMyAdmin/index.php>

LOGIN: lab

PASSW0RD: qn&ngpwdDB1

DATABASE NAME: qnndb

TABLE NAME: deposition

TABLE LINK : <http://qnn-nas-rle.mit.edu/phpMyAdmin/sql.php?db=qnndb&table=deposition>

the table link is bookmarked on the AJA pc.

The database looks like this. You can sort the table by clicking on the desired header.

Server: MariaDB 10 » Database: qnndb » Table: deposition

Showing rows 0 - 24 (508 total, Query took 0.0024 seconds.) [sample: [BLOB - 6 B]... - [BLOB - 6 B]...]

```
SELECT * FROM `deposition` ORDER BY `sample` DESC
```

1 > >> | Number of rows: 25 | Filter rows: Search this table | Sort by key: PRIMARY (DESC) v

	sample	date	description	process_id	user	run_id	material	substrate	capping_layer
☐	SPG518	5/16/2021	NbN xrd	OMK_noRFbias	OM	2145	NbN	SiO2	
☐	SPG517	5/16/2021	NbN xrd	AED_RT	OM	2144	NbN	SiO2	
☐	SPG516	5/14/2021	AlN 20 nm DC test	manual	IC	2143	AlN	SiO2	
☐	SPG515	5/14/2021	JPL MoSi experiement V3	YM_MoSi_Si_cap	IC	2142	MoSi	SiO2	
☐	SPG514	5/13/2021	MoSi evaluation	YM_MoSi_Si_cap	MC	2141	MoSi- Si	SiO2	
☐	SPG513	5/12/2021	NbN	OMK_noRFbias	OM	2140	NbN	SiO2	
☐	SPG512	5/12/2021	AlN target calibration: XRR	manual	IC	2139	AlN	SiO2	
☐	SPG511	5/11/2021	NbN	AED_RT	OM	2138	NbN	SiO2	
☐	SPG510	5/10/2021	NbN	AED_RT	OM	2137	NbN	SiO2	
☐	SPG509	5/10/2021	NbN	AED_RT	OM	2136	NbN	SiO2	
☐	SPG508	5/9/2021	NbN	AED_RT	OM	2135	NbN	SiO2	
☐	SPG507	5/7/2021	Glenn.Photolithography	Manual	IC	2134	NbN	SiO2	
☐	SPG506	5/7/2021	Glenn.Photolithography	Manual	IC	2134	NbN	SiO2	
☐	SPG505	5/7/2021	JPL MoSi experiement	YM_MoSi_Si_cap	IC	2133	MoSi	SiO2	
☐	SPG504	5/7/2021	TEST JPL	YM_MoSi_Si_cap	IC	2132	MoSi	SiO2	
☐	SPG503	5/6/2021	NbN via	AED_RT	OM	2131	NbN	SiO2	
☐	SPG502	5/5/2021	NbN RT	AED_RT	MC	2130	NbN	SiO2	
☐	SPG501	5/5/2021	NbN RT calibration - reproducibility	AED_RT	MC	2129	NbN	SiO2	
☐	SPG500	5/5/2021	NbN RT calibration	AED_RT	MC	2128	NbN	SiO2	
☐	SPG499	5/5/2021	MoSi_comp_test 20 nm "D"	YM_MoSi	IC	2127	MoSi	SiO2	
☐	SPG498	5/5/2021	MoSi_comp_test 20 nm "C"	YM_MoSi	IC	2126	MoSi	SiO2	
☐	SPG497	5/5/2021	Si capping XRR	YM_Si_only	IC	2125	Si	SiO2	

Insert a new row or search for past depositions using these tabs. Copying a past entry might be a fast method.

Server: MariaDB 10 » Database: qnndb » Table: deposition

Browse Structure SQL **Search** **Insert** Export Import Privileges Operations Triggers

All of the columns are listed. There is an "Ignore" section halfway down the page. This

Browse

Structure

SQL

Search

Insert

Export

Import

Privileges

Operations

Triggers

Column	Type	Function	Null	Value
sample	text			
date	text			
description	text			

<https://qnn.mit.edu/wordpress/?format=pdf&post-type=post&order-date=asc&order-menu=asc&statuses%5B%5D=publish&pmb-author=165&dates%5Bafter%5D=>

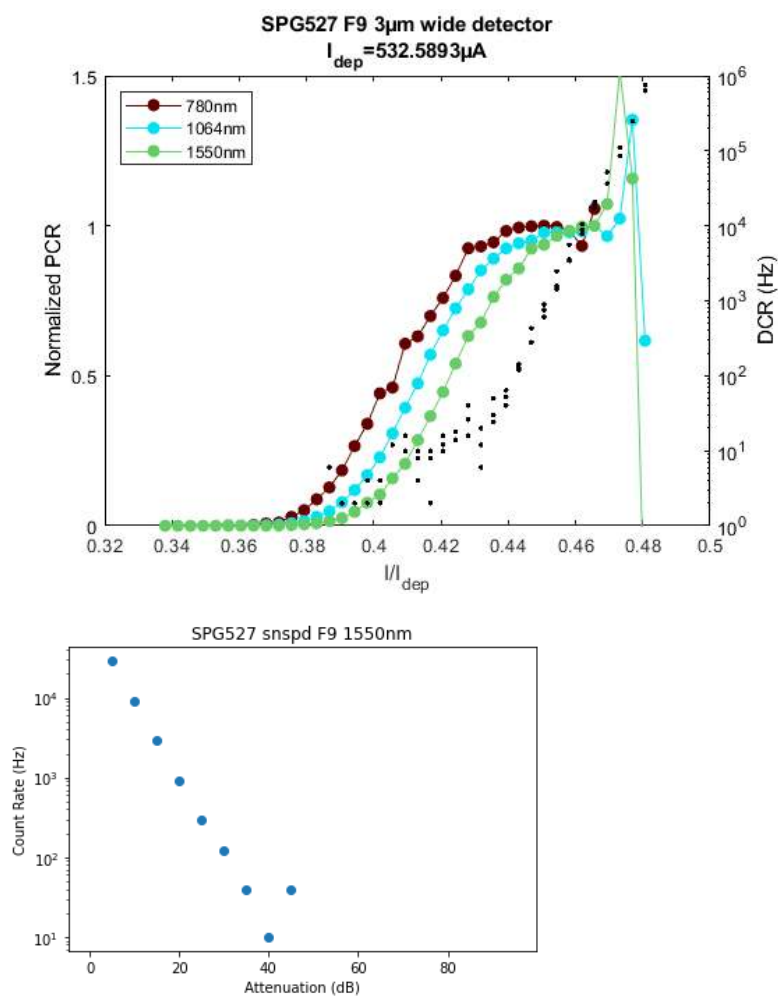
194/642

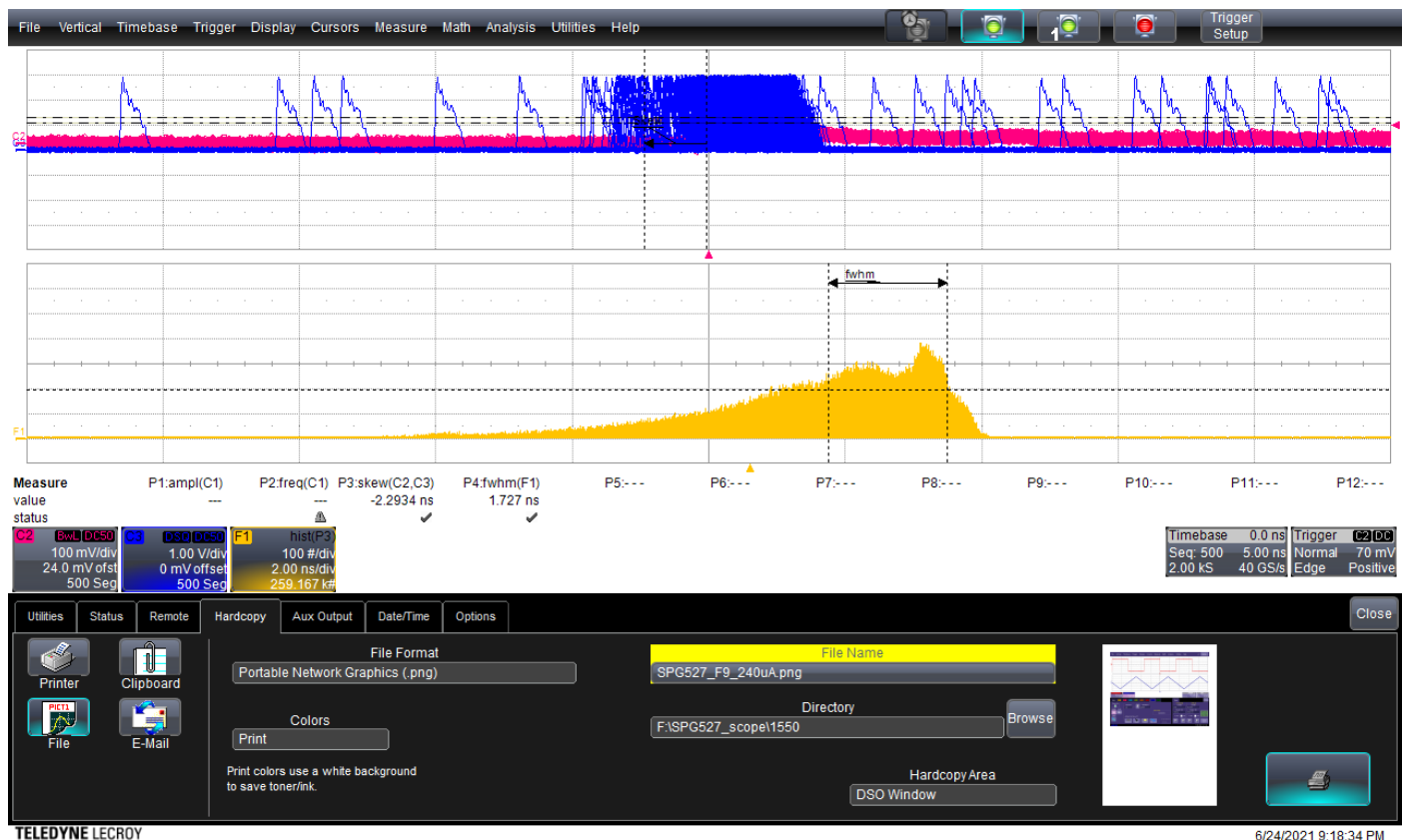
SPG527 wide wire nbn

June 30, 2021

Categories: General, SNSPD

N2 = 14, Ar = 40





INDUCTOR 7 μ m wide and 0.5 μ m wide gap. CPW effective dielectric constant.

load constants

ee = 363;

vp = c.c/sqrt(ee);

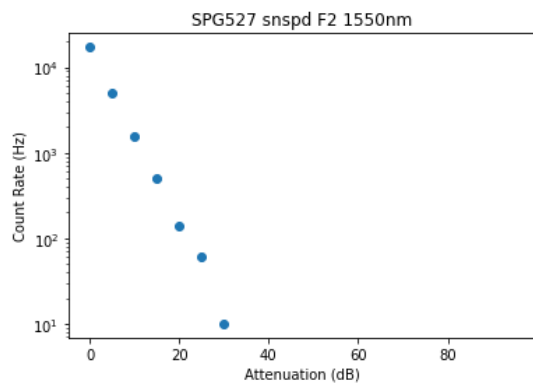
l = 10.85e-3;

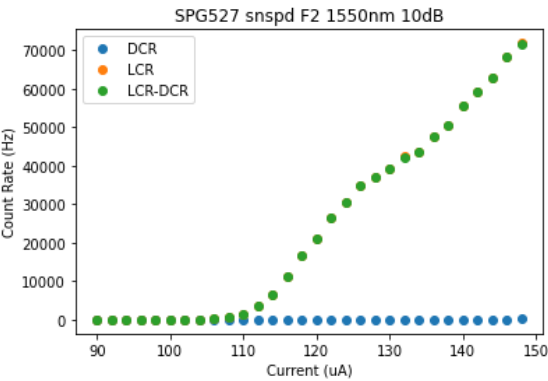
f=1e9;

lg = c.c/(f*sqrt(ee));

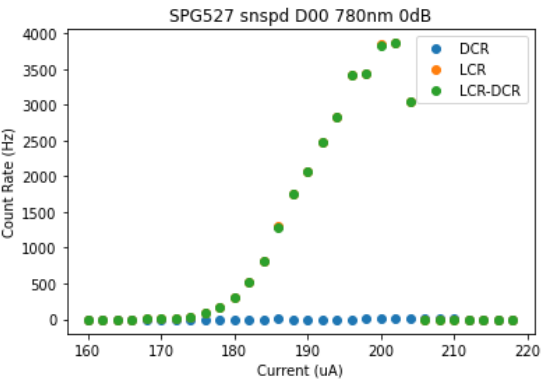
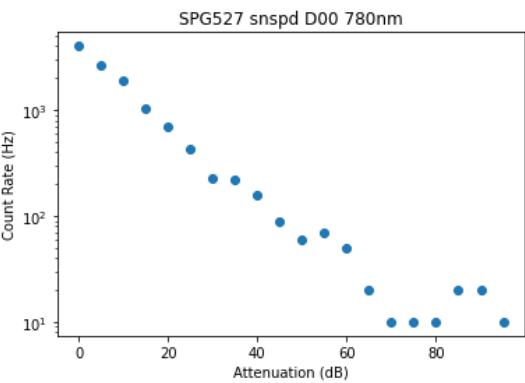
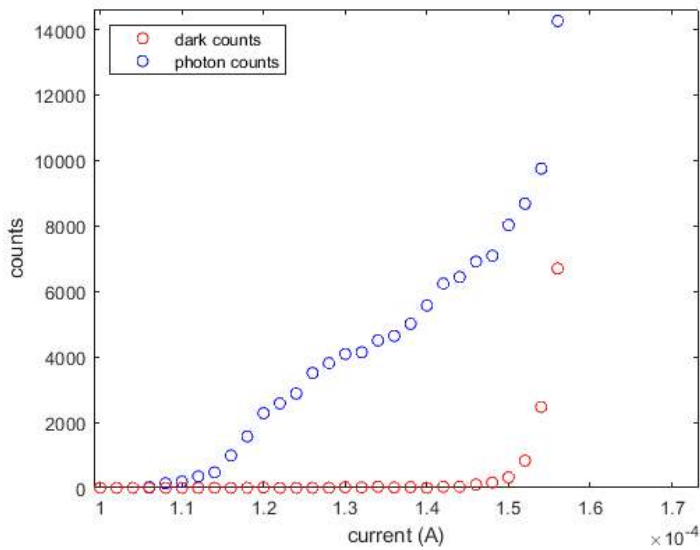
dt = l/vp*1e9

dt = delay_time_in_inductor = 689ps

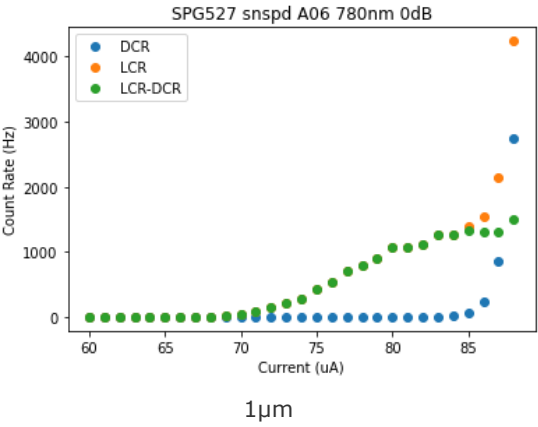
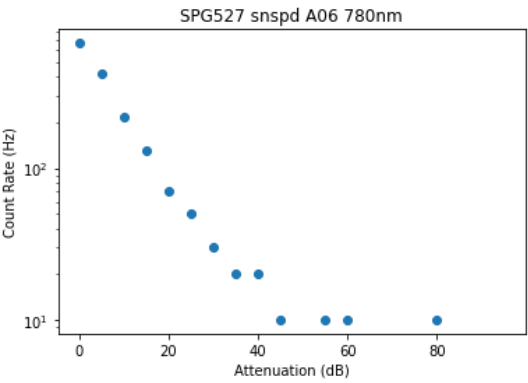




1.5μm



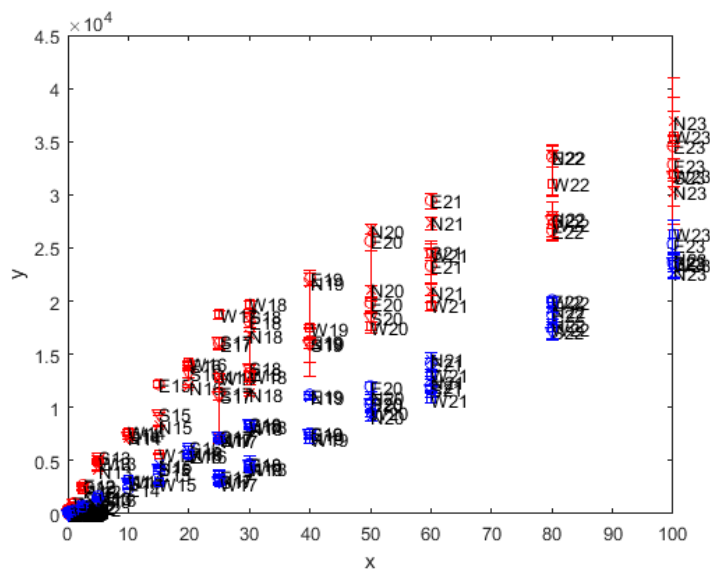
2.5μm



More pearl length...

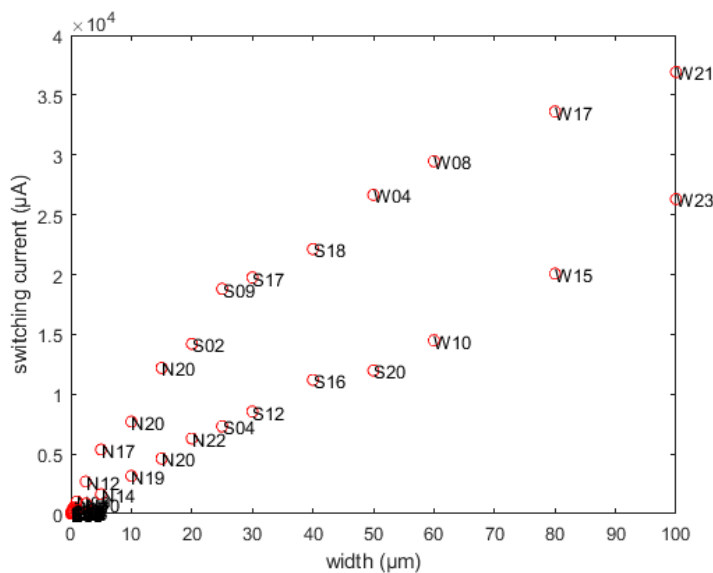
July 13, 2021

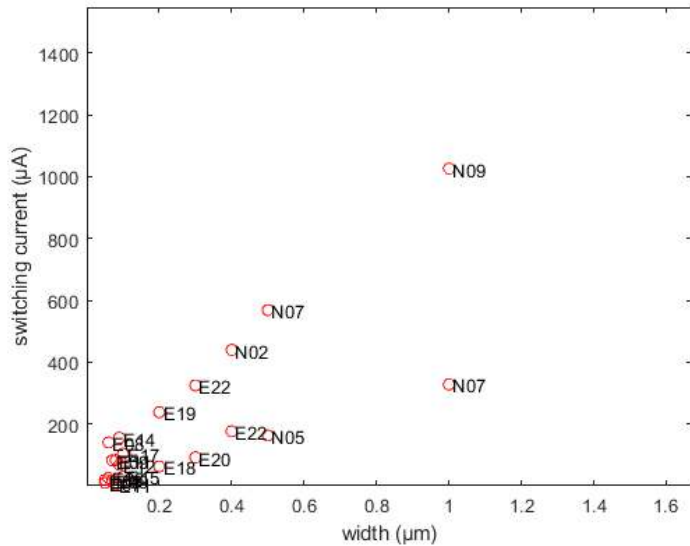
Categories: Superconductivity



Heat problems as well as $t=0$ problems

[switching_currents.zip](#)





```
j42 = Table[a /. FindFit[data42[[1 ;; i]], a x, a, x], {i, 3, 12}];
j75 = Table[a /. FindFit[data75[[1 ;; i]], a x, a, x], {i, 3, 13}];
```

```
Tc = 9.5
```

```
9.5
```

```
j75 / kl[7.5 / Tc]
```

```
j42 / kl[4.2 / Tc]
```

```
{1090.37, 767.012, 1430.88, 1341.74, 1260.94, 1208.33, 1435.19, 1347.41, 1279.92, 1284.85, 1249.85}
```

```
{1584.91, 1444.37, 1619.24, 1501.08, 1434.73, 1335.12, 1303.51, 1307.71, 1230.49, 1242.56}
```

```
Λ75 = Table[Ap /. FindFit[data75,  $\frac{w j75[[i]]}{\left(1 + \left(c[7.5 / Tc] + \frac{4 k (7.5/Tc) - c[7.5/Tc]}{1 + 3 k (7.5/Tc) \frac{w}{2 \pi \Delta p}}\right) \left(\frac{w}{2 \pi \Delta p}\right)^2}\right)^{1/4}}, Ap, w], \{i, 1, \text{Length}[j75]\}]$ 
```

```
{14.1341, 6.52752 × 10-8, 4.32754, 5.39917, 6.83108, 8.17225, 4.28485, 5.31816, 6.43976, 6.34431, 7.07973}
```

```
Λ42 = Table[Ap /. FindFit[data42,  $\frac{w j42[[i]]}{\left(1 + \left(c[4.2 / Tc] + \frac{4 k (4.2/Tc) - c[4.2/Tc]}{1 + 3 k (4.2/Tc) \frac{w}{2 \pi \Delta p}}\right) \left(\frac{w}{2 \pi \Delta p}\right)^2}\right)^{1/4}}, Ap, w], \{i, 1, \text{Length}[j42]\}]$ 
```

```
{0.73452, 0.905512, 0.700233, 0.829859, 0.919413, 1.08443, 1.14639, 1.13786, 1.31201, 1.28221}
```

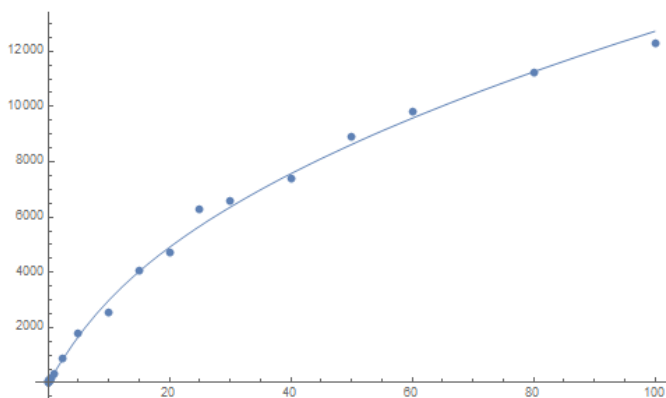
```
Λ75 l[7.5 / Tc]
```

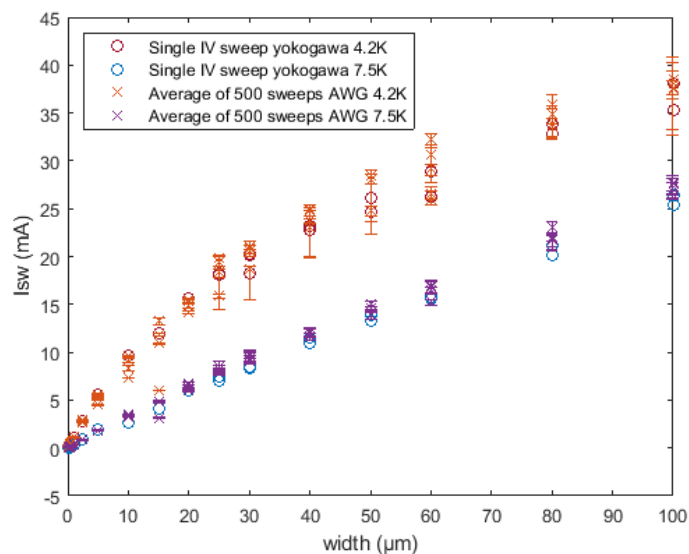
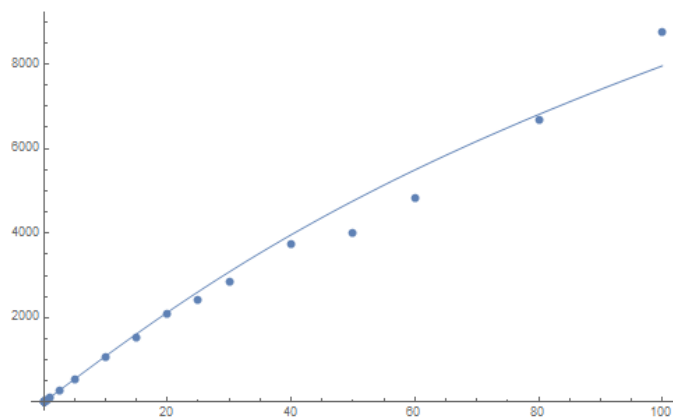
```
Λ42 l[4.2 / Tc]
```

```
{7.03201, 3.24757 × 10-8, 2.15304, 2.68619, 3.3986, 4.06586, 2.1318, 2.64589, 3.20391, 3.15642, 3.52231}
```

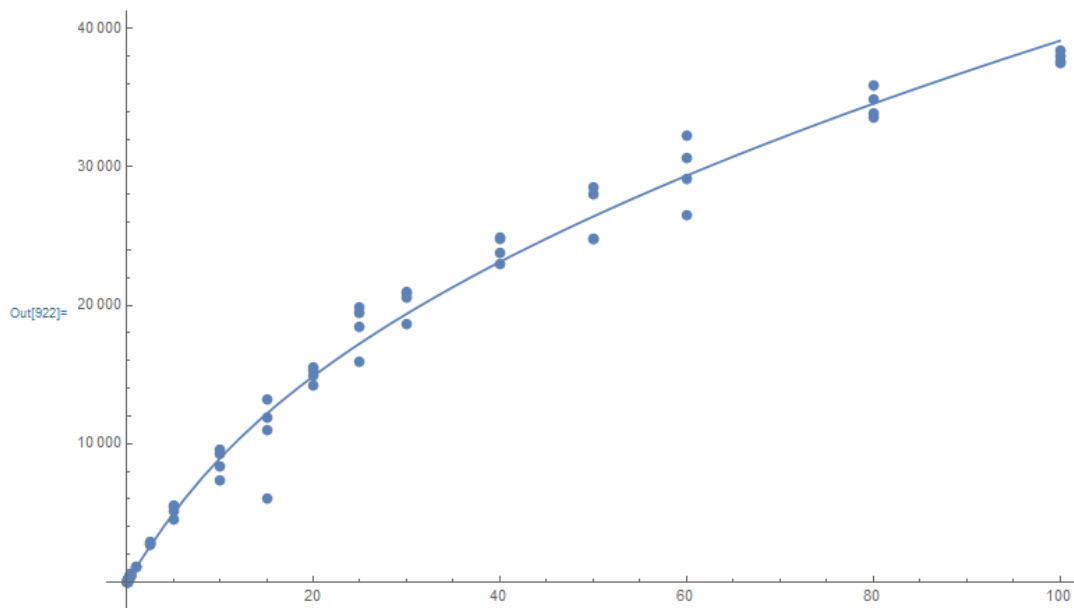
```
{0.6797, 0.837931, 0.647972, 0.767924, 0.850794, 1.0035, 1.06083, 1.05293, 1.21409, 1.18651}
```

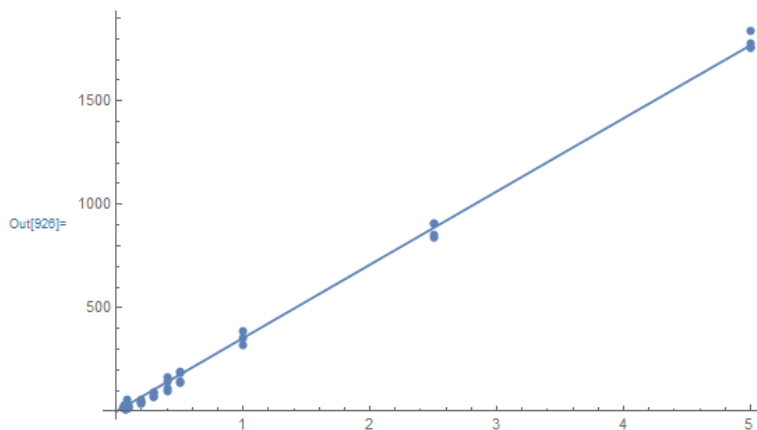
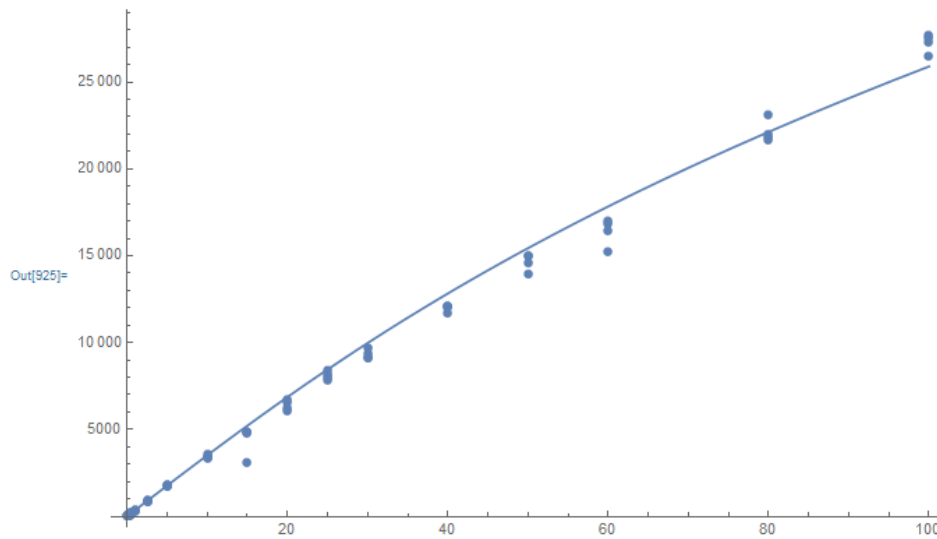
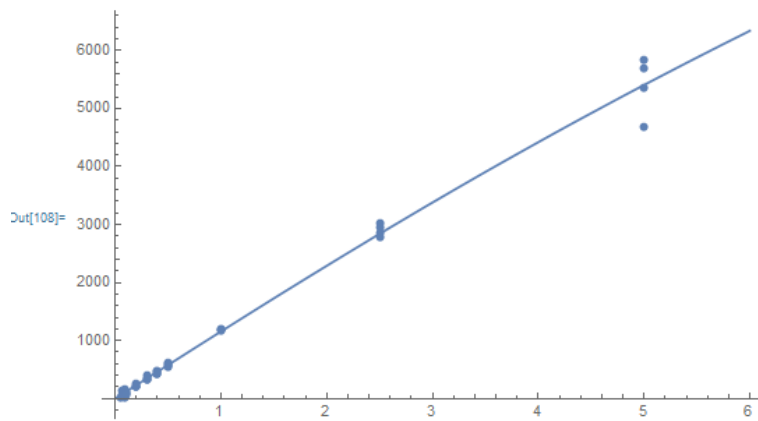
```
Show[Plot[ $\frac{w j42[[-1]]}{\left(1 + \left(c[4.2 / Tc] + \frac{4 k (4.2/Tc) - c[4.2/Tc]}{1 + 3 k (4.2/Tc) \frac{w}{2 \pi \Delta p}}\right) \left(\frac{w}{2 \pi \Delta p}\right)^2}\right)^{1/4}}, \{w, 0, 100\}], \text{ListPlot}[data42]]$ 
```





Ic from AWG had to be scaled by ~ 1.8 for appropriate voltage splitting. Scaling came from yokogawa ic at 100 μ m and 7.5K. A better method would be to use the same device but with 50ohm and without 50ohm





mathematica.zip

Hi Owen,

Thank you for the data.

The maximum w/λ_p value should be less than ~ 3 to determine the critical current density. If we choose this range for both temperatures, the temperature dependence of the critical current

density satisfies the Kupriyanov-Luckichevs results.

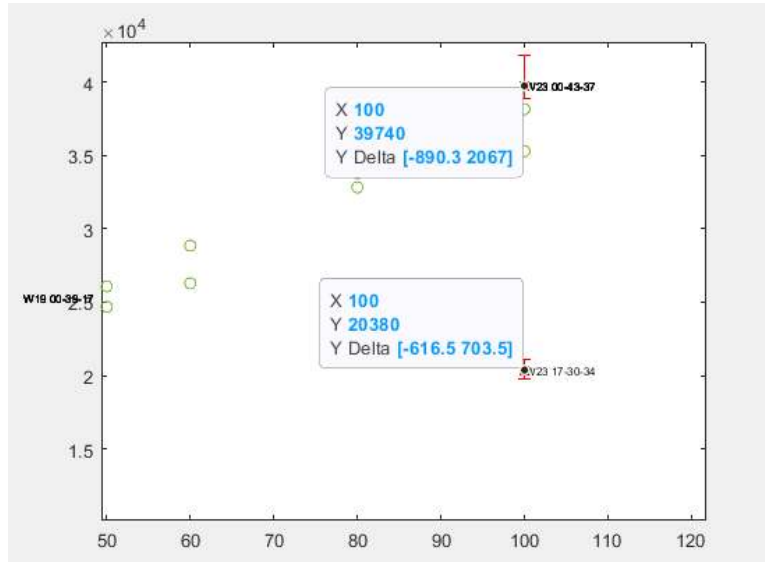
But the temperature dependence of Pearl penetration depth is still non-BCS though the fit is better (I wonder why the best one was at the beginning 😊). I guess Karl and Mikhail should decide about the quality of the fit, but I think for non-BCS behavior, we need to obtain the Pearl penetration depth of more than two points to find the temperature dependence.

There is a strange point at both temperatures at $w=15\mu\text{m}$. I suppose we can drop it.

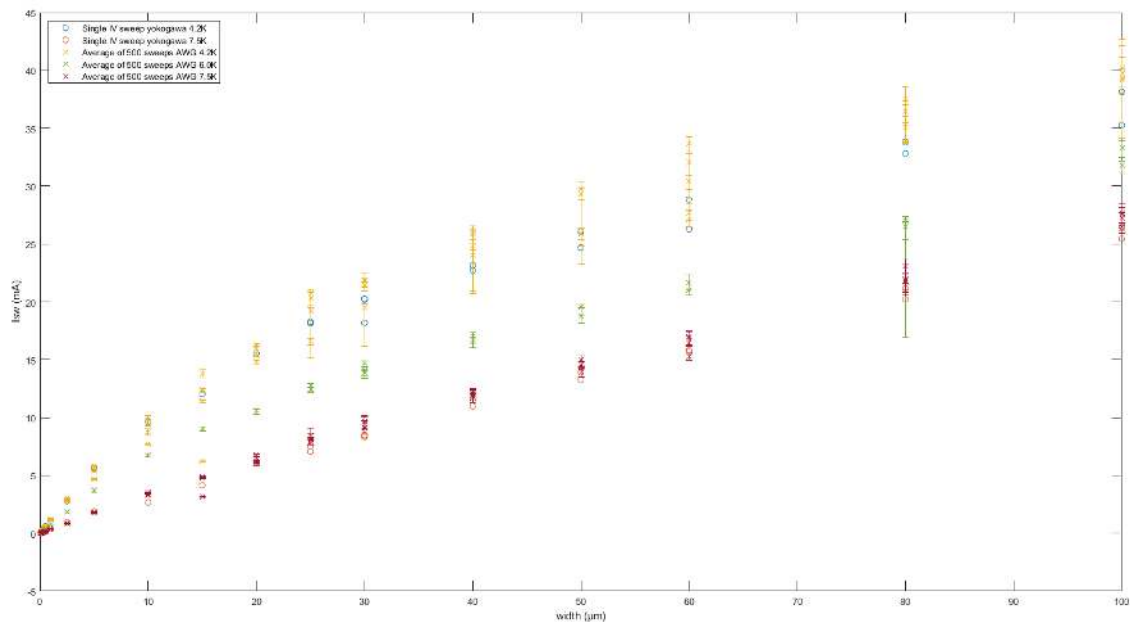
Let me know what Karl thinks.

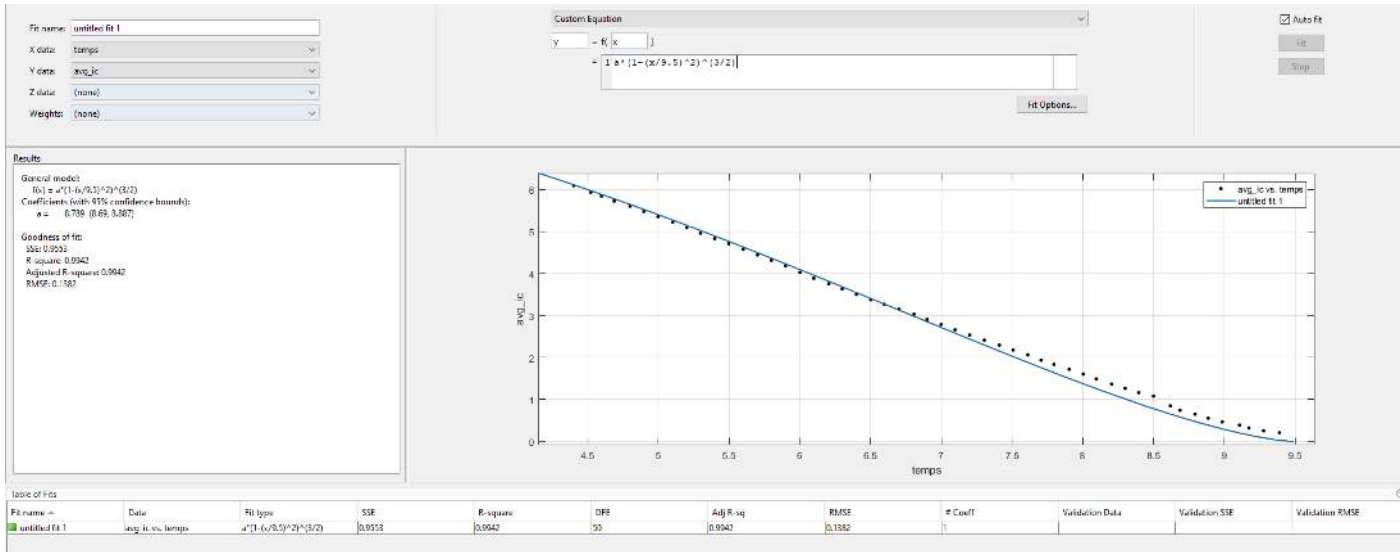
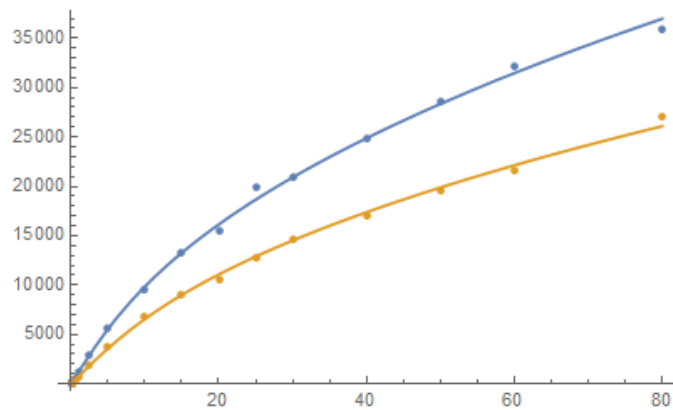
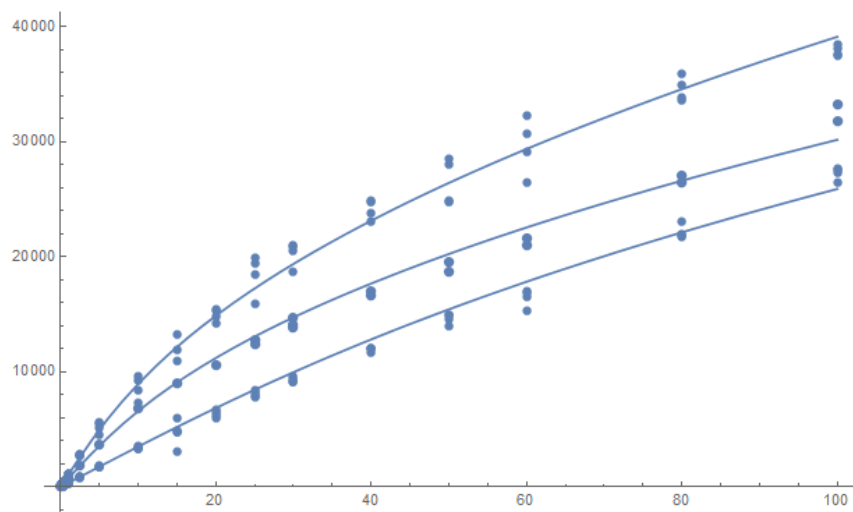
Dina

Ratio of 50ohm measurement and without 50ohm



$39740/20380 = 1.95$. Previously I was using 1.8672 which is the ratio of the yokogawa measured result of $100\mu\text{m}$ wide at 7.5K compared to the same device with AWG



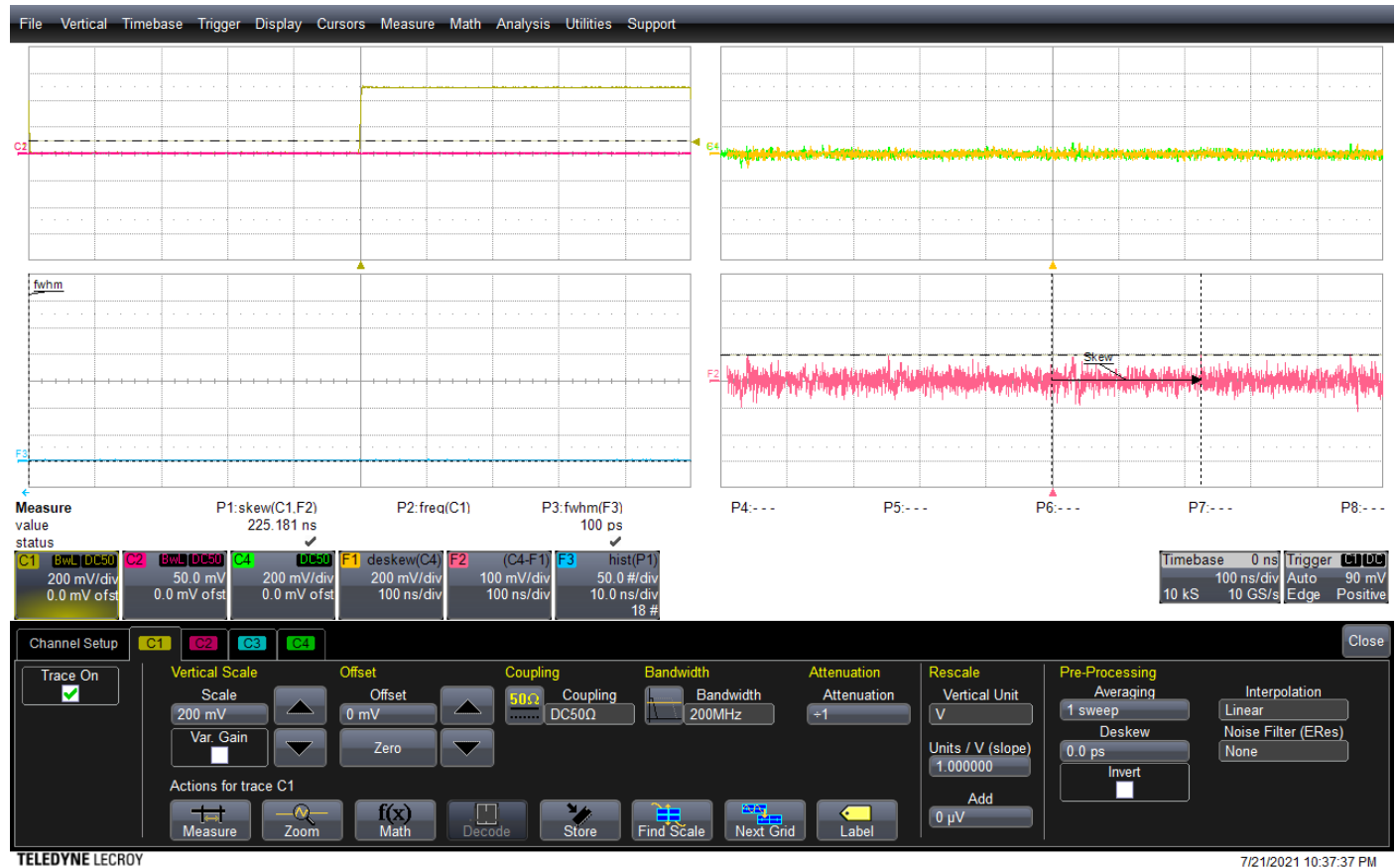


W11

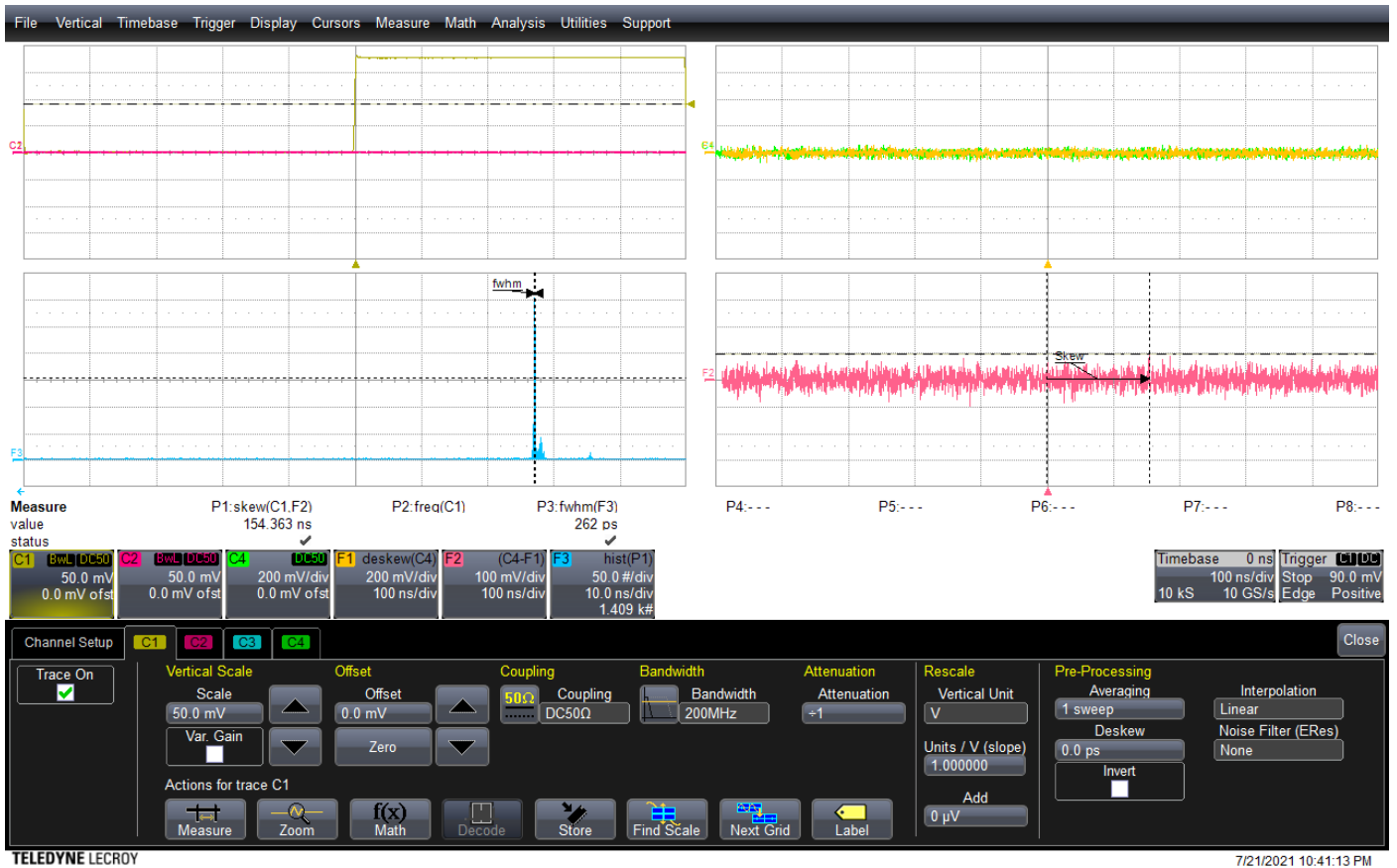
SPG573 nTron grey zone

July 28, 2021

Categories: General



1.13 volts from AWG. Split, -37dB, 50Ohm = 159uA. Biasing slightly lower you can see that there is some small pulse on the output. I believe it is the gate switching.



Lowering the bias to 360mV (50uA) the spikes less visible, but still sorta there. (not clear in this image)



140μA to channel. a 21μA input to the gate latches the device.

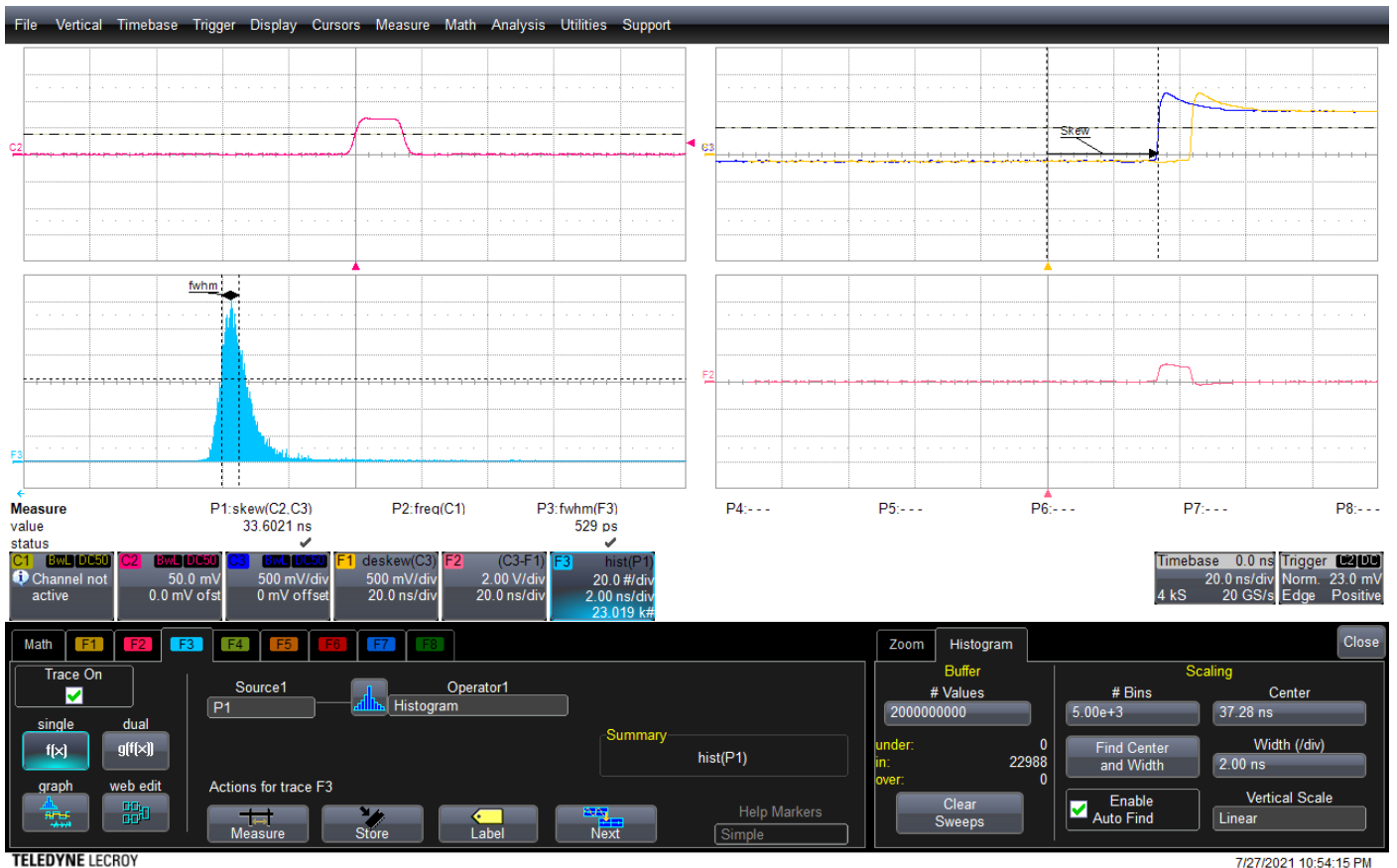
Sweeping pulse width and height. `np.linspace(5e-9, 150e-9, 11), np.linspace(0.07, 0.09, 9)`

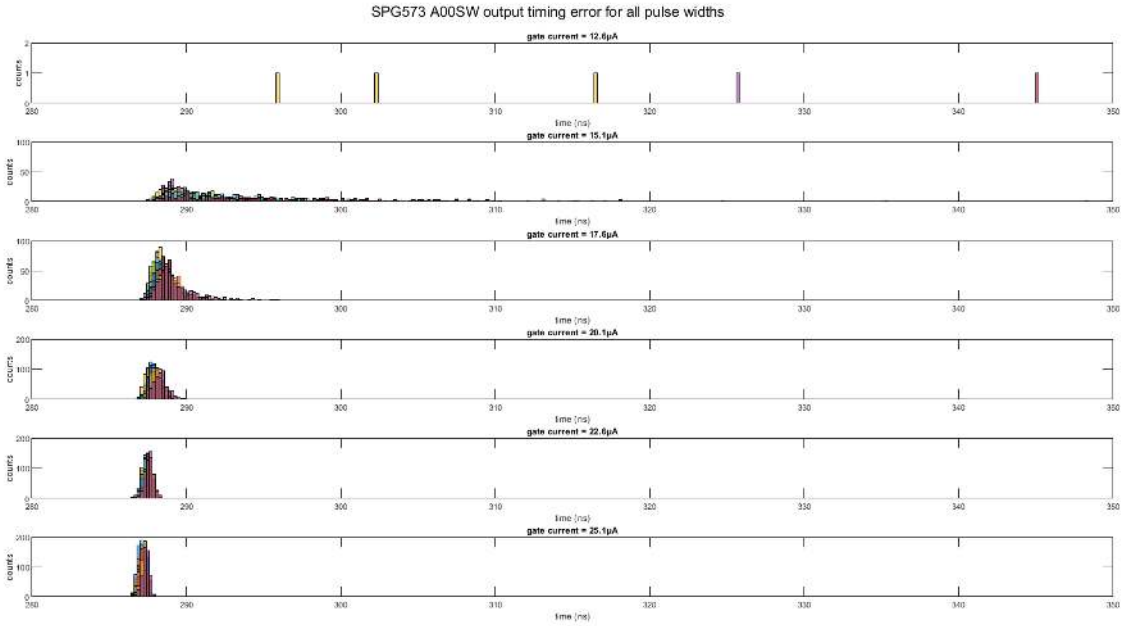
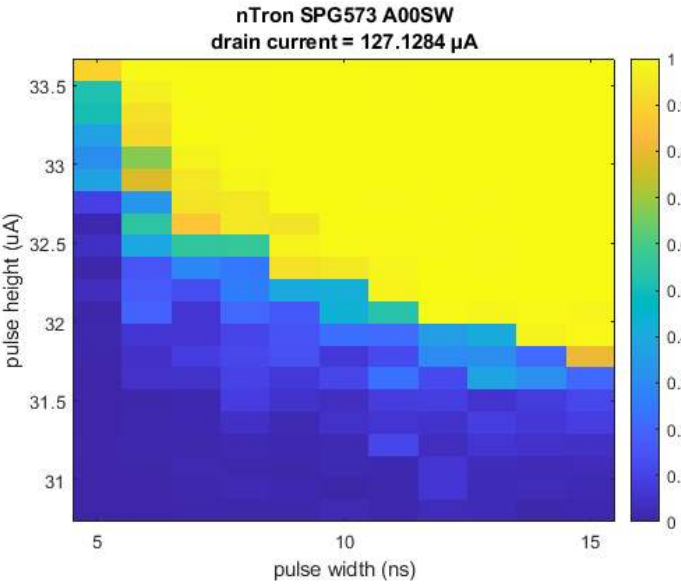


I had to retake the data because the scrip saved the wrong traces :(. Here there was some error where the channel would switch early. This is likely because the bias was too close to I_c . I_c was slightly lower than normal as the temp was slightly higher 4.8K (empty dewar)

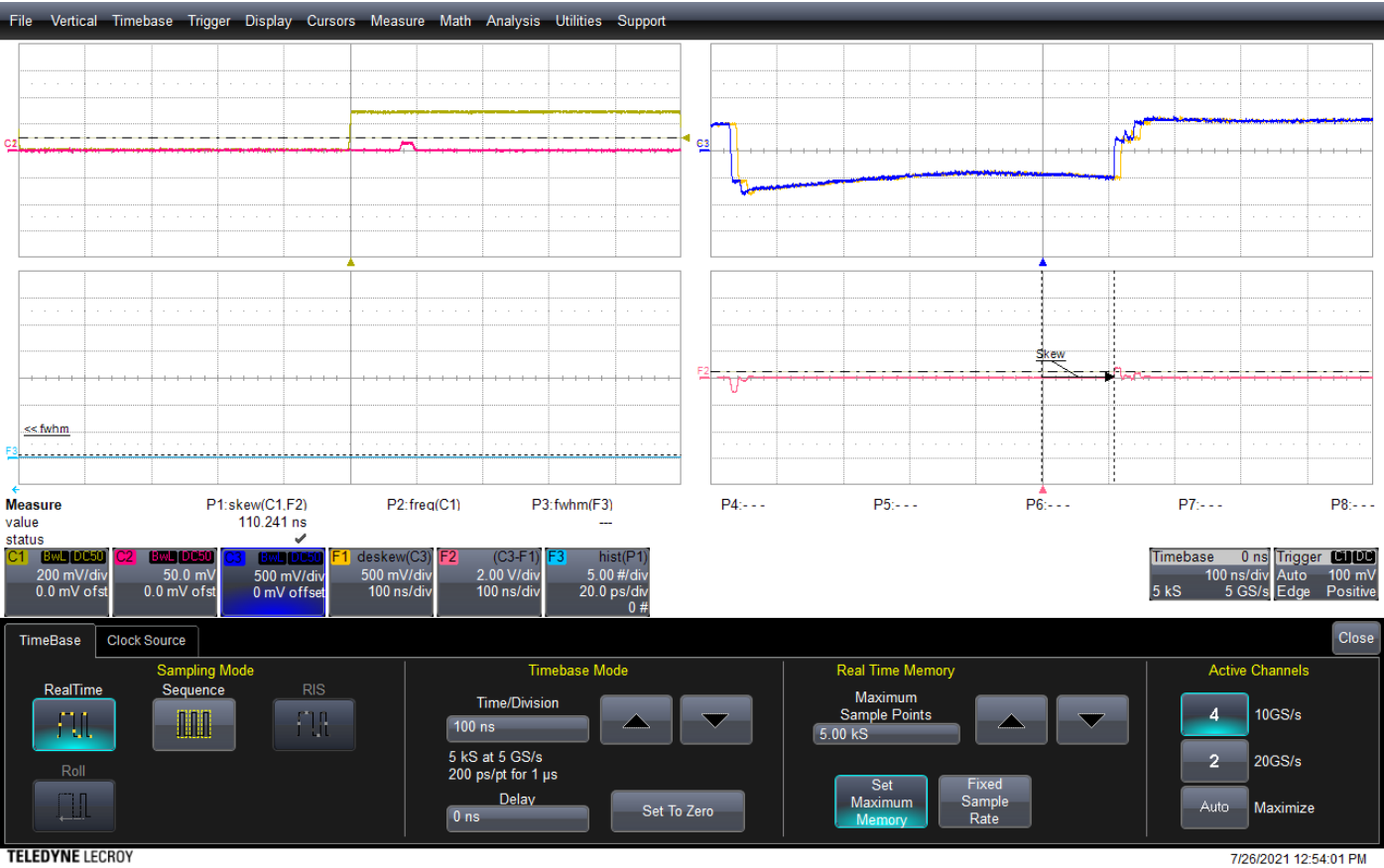


At low gate currents and long gate pulses there is some error in when the device switches. This error goes away as the gate current is increased.

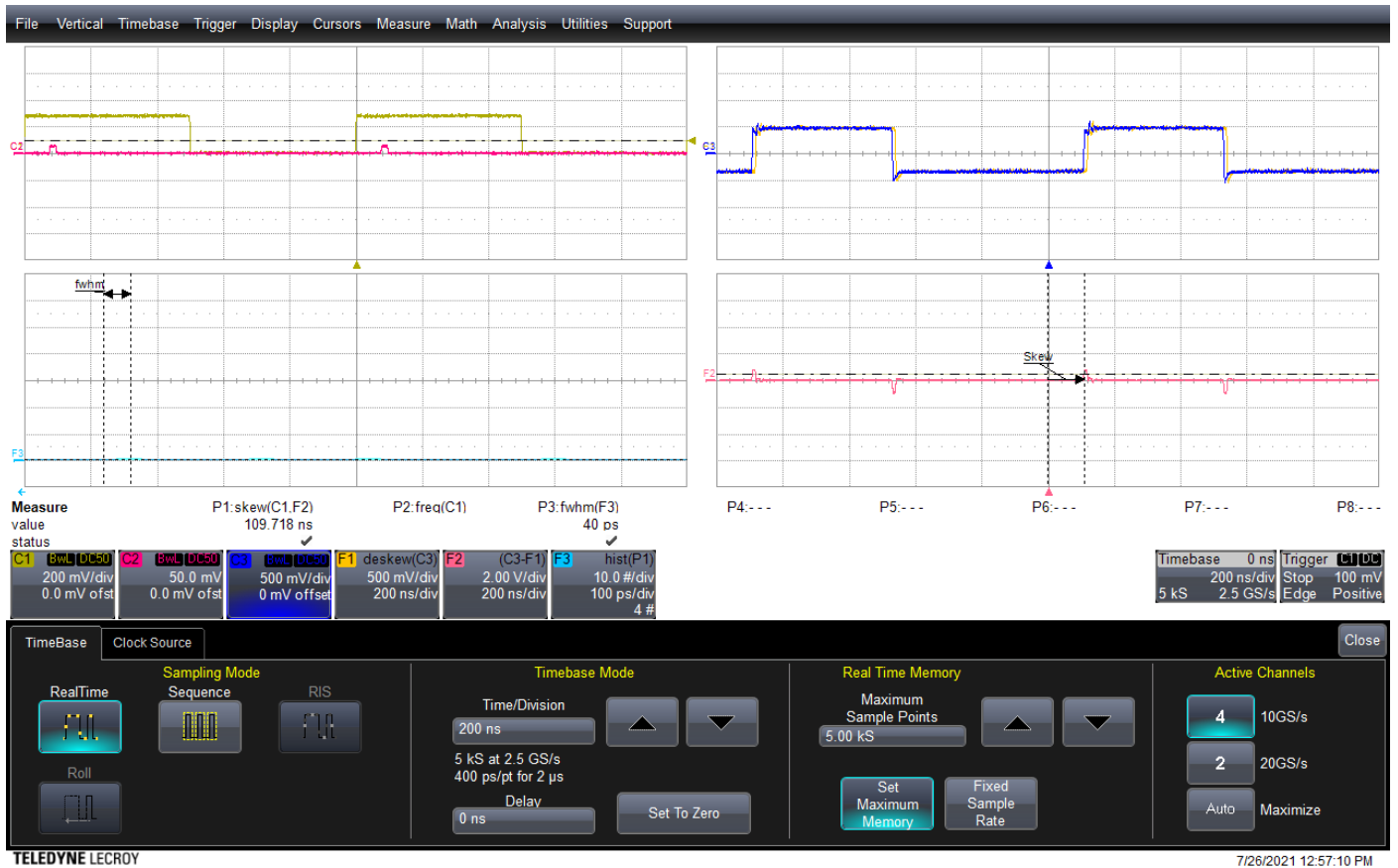




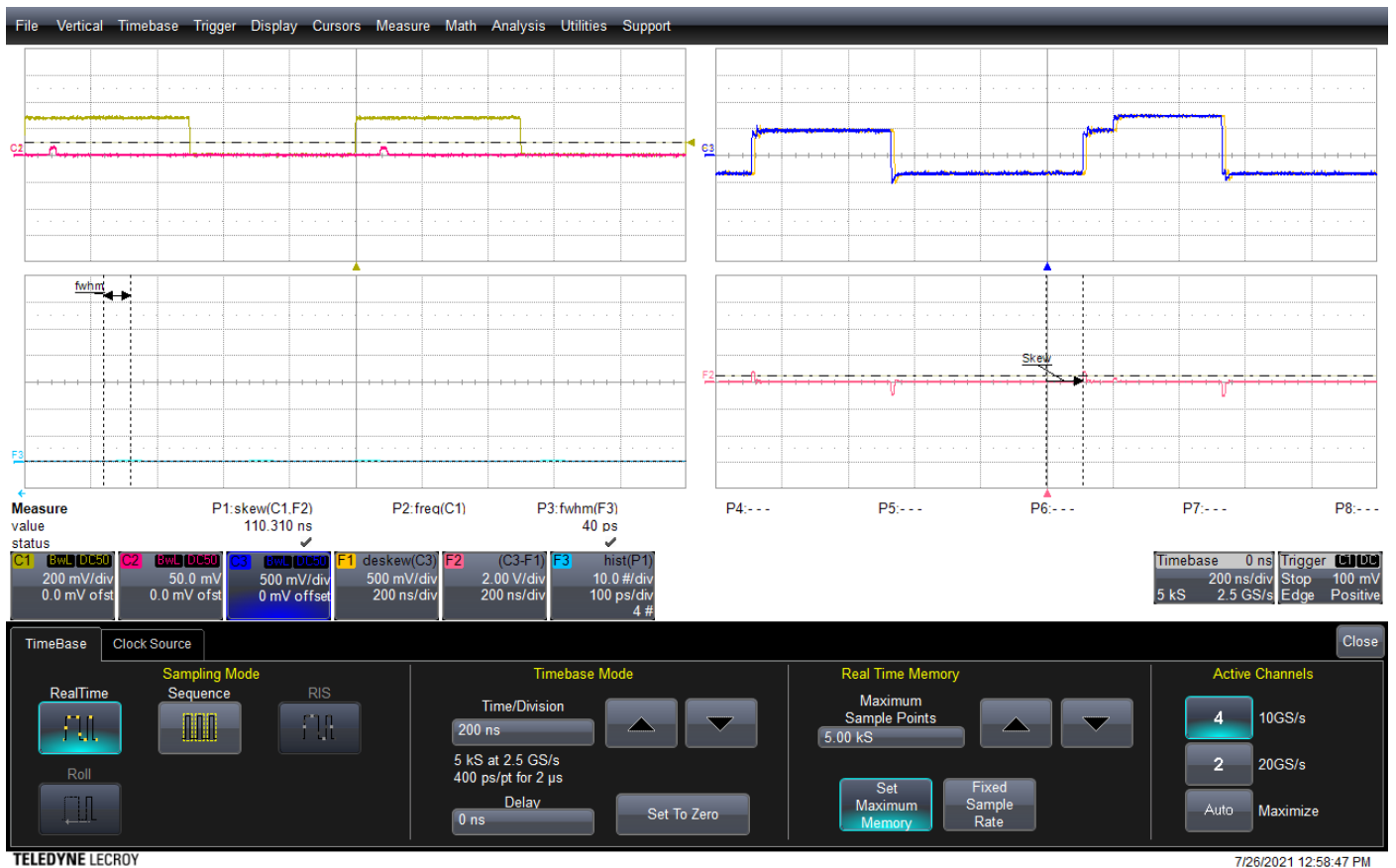
NOT GATE



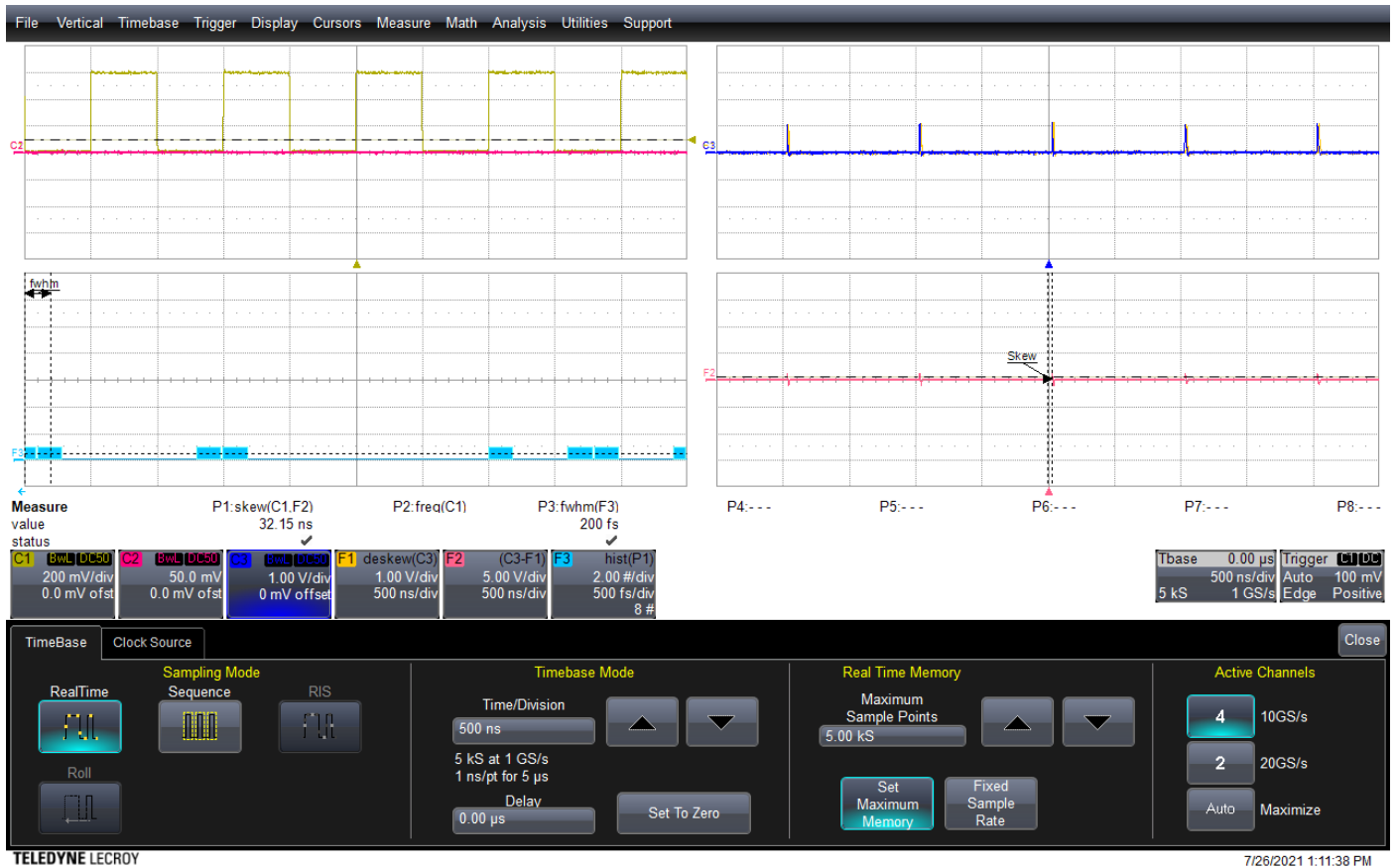
not gate. nanowire output (shown) looks the same as the ntron output. has a double bump



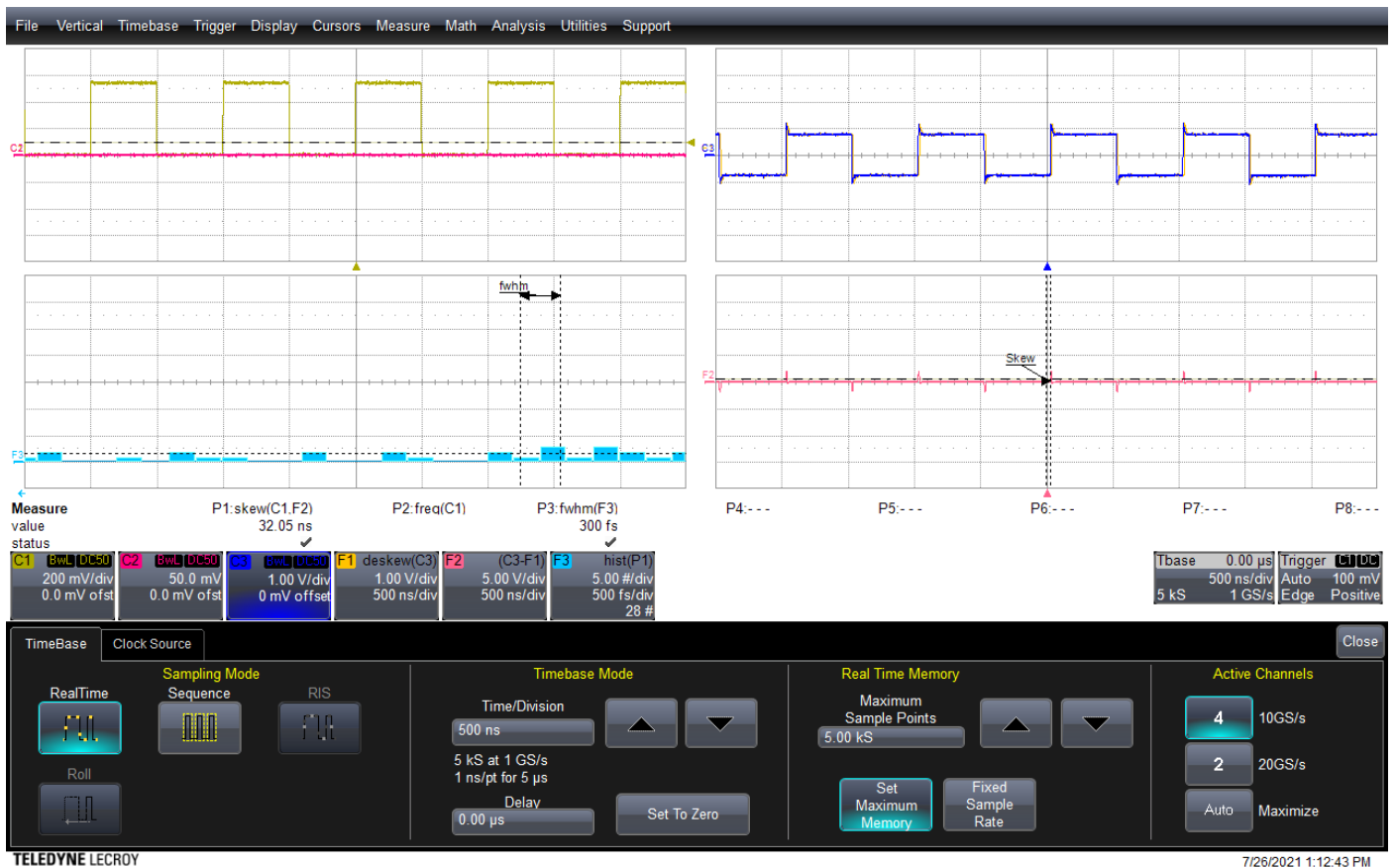
just the nanowire (80uA bias)



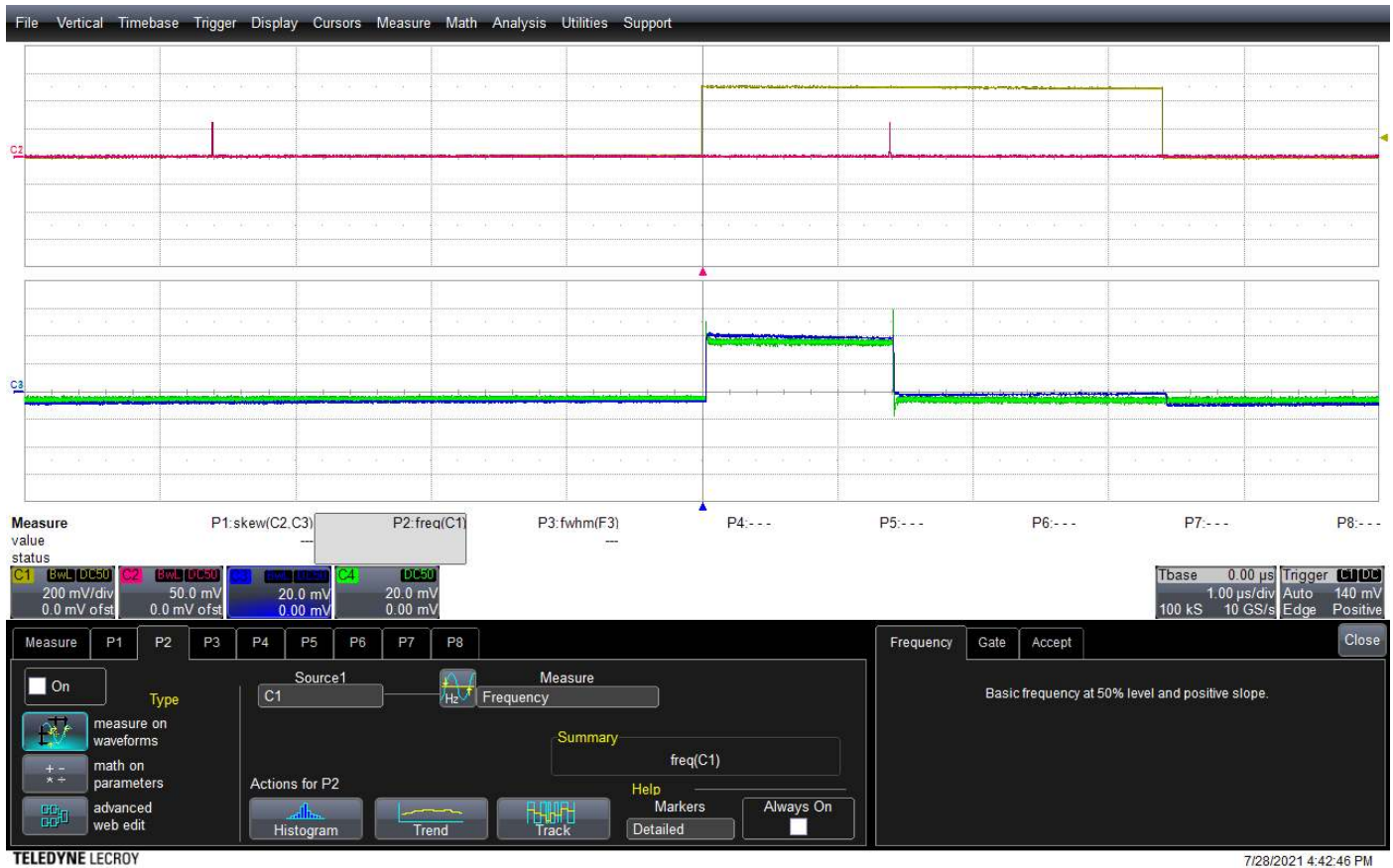
nanowire and ntron switching (80uA bias) Half microamp increase always switches the nanowire and ntron. Too close



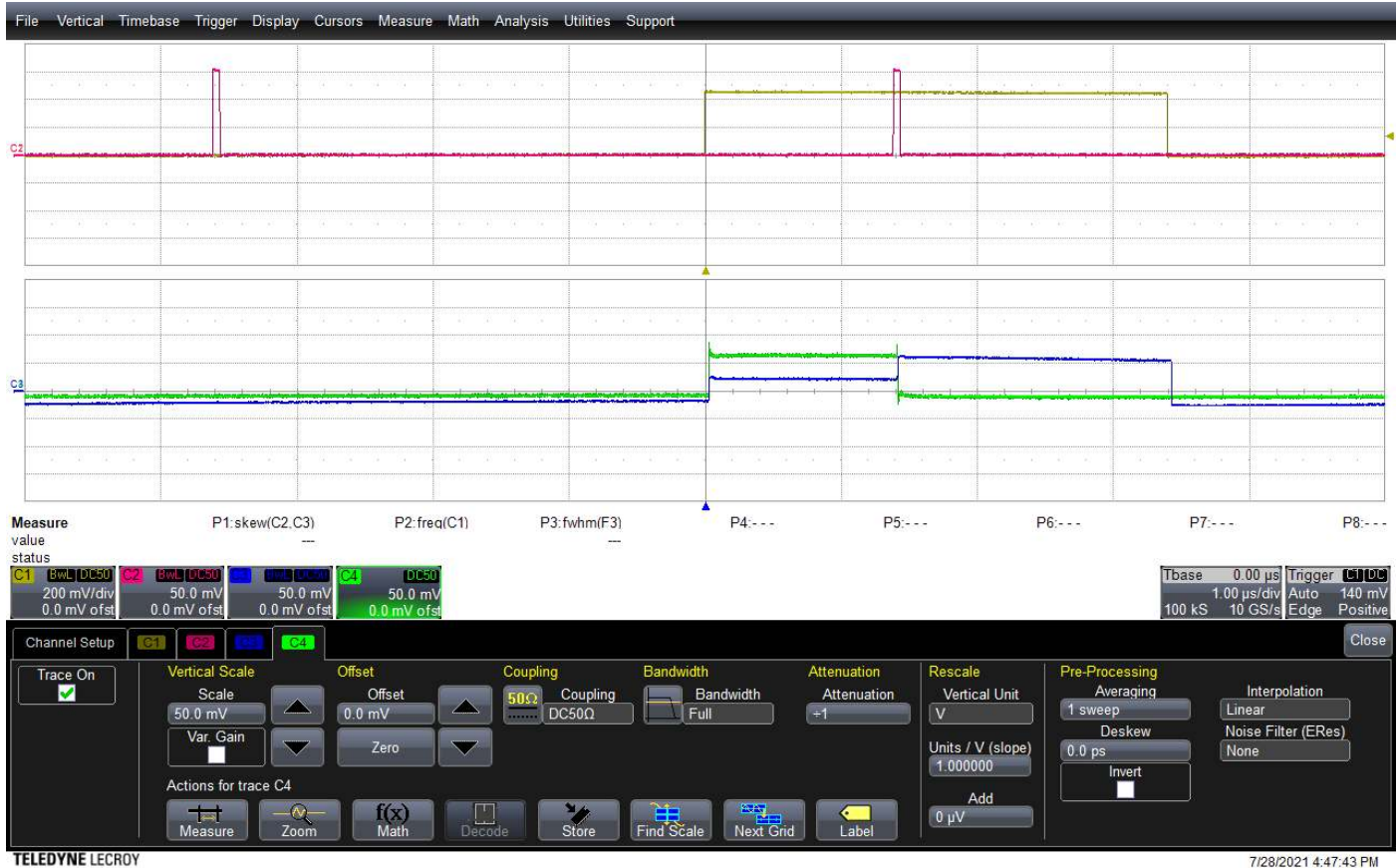
L1-500ohms at SMA. L2-500ohms at scope. 1.2V bias (169.5uA)



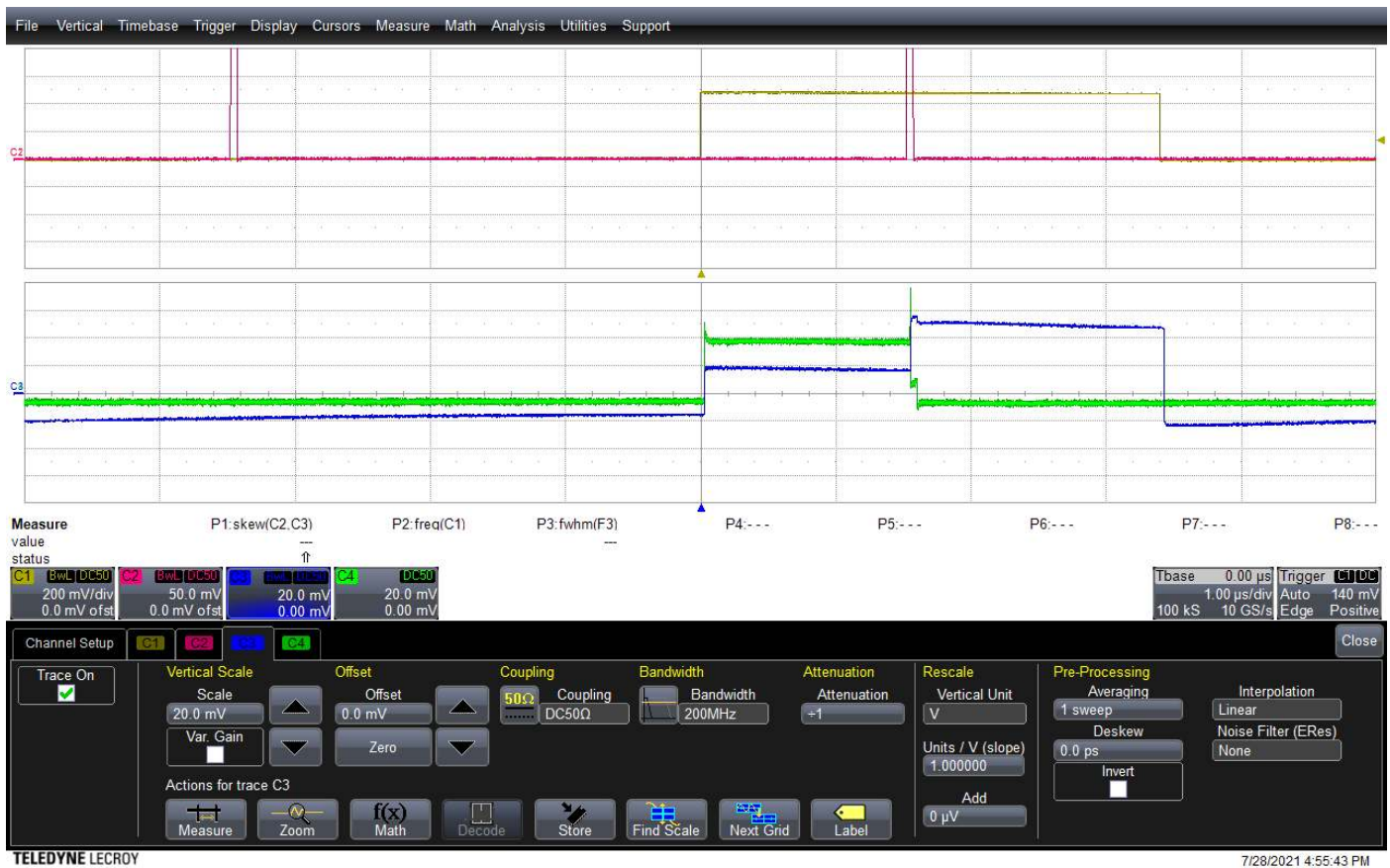
L1-500ohms at SMA. L2-500ohms at scope. 1.1V bias (155.4uA)



B00 not gate. both load outputs have the same 500hm resistance in series (blue, green)

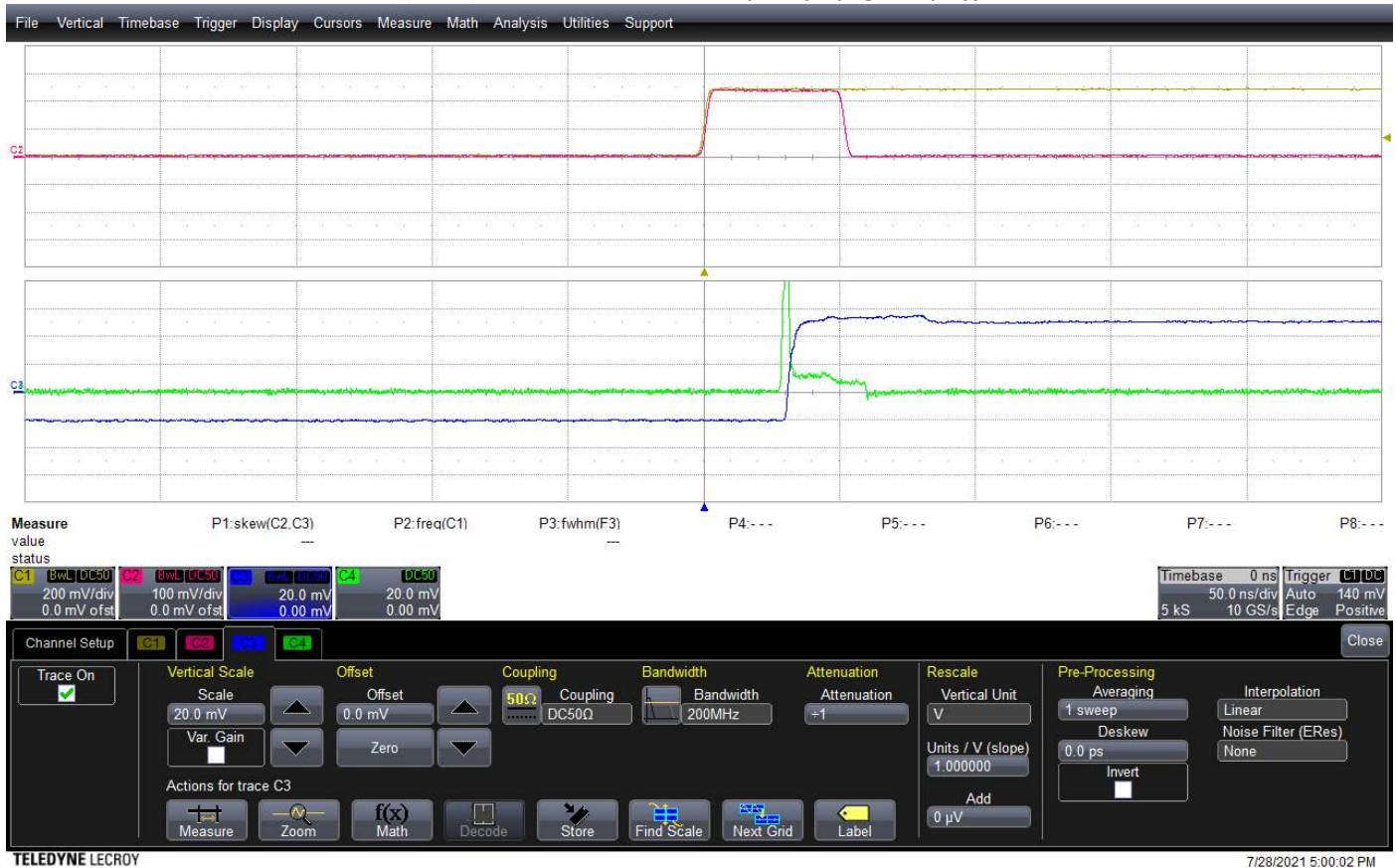


B02. L1-500hm, L2-30hm. (blue(L1), green(L2))



7/28/2021 4:55:43 PM

B11. L1-100Ohm, L2-30hm. (blue(L1), green(L2))



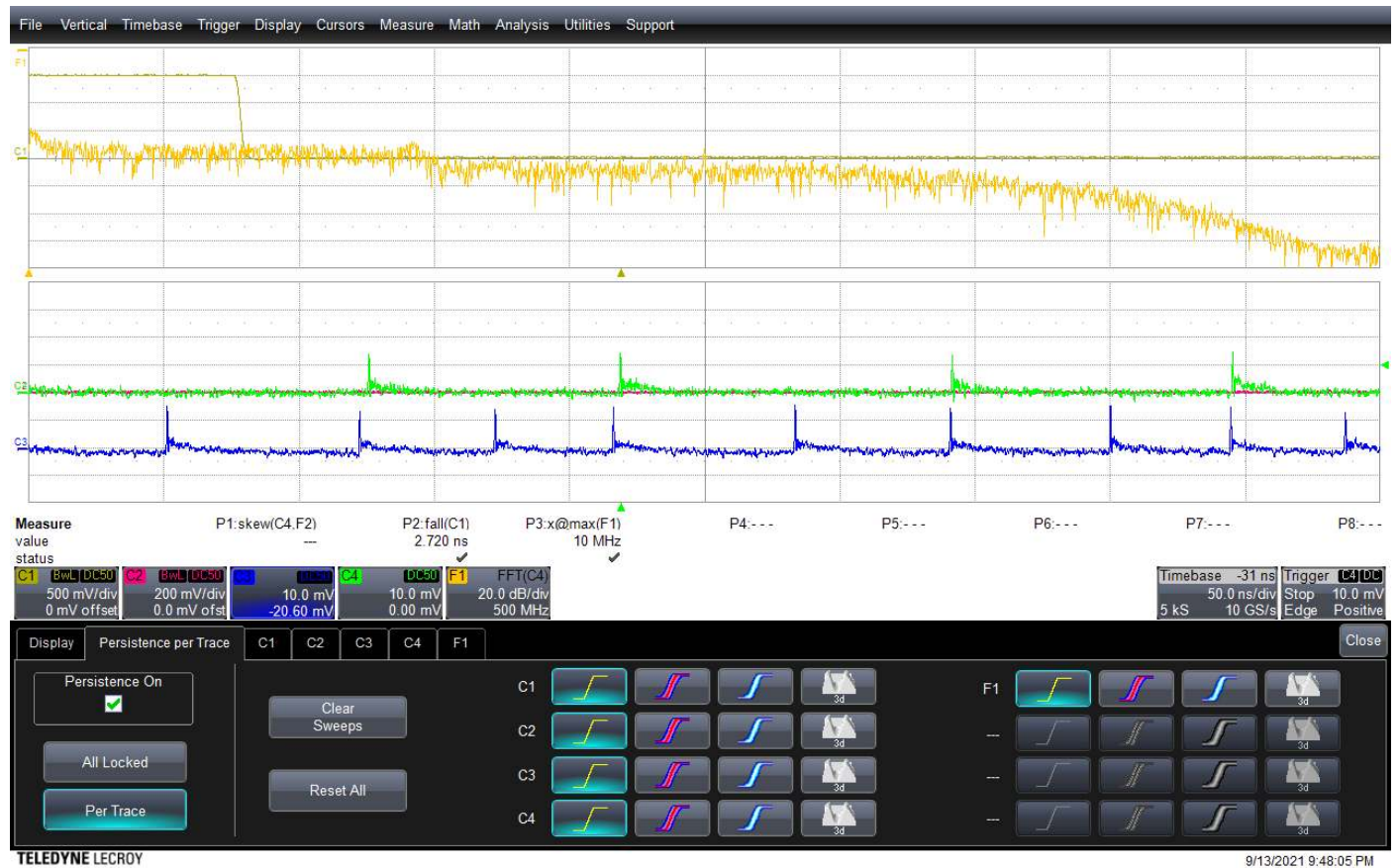
7/28/2021 5:00:02 PM

Trying to see shortest timing between ON and Not operation. Looks to be sub-ns

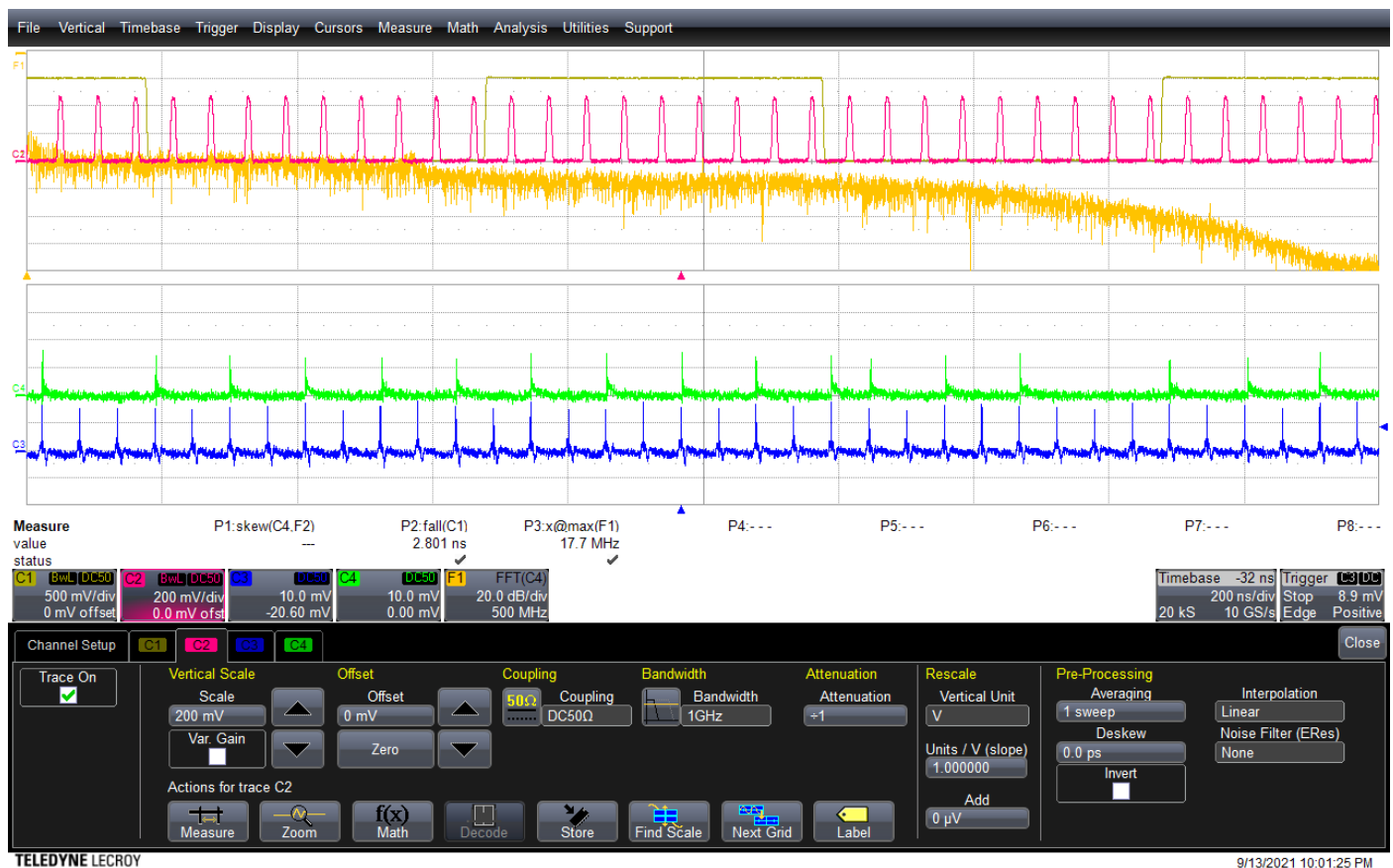
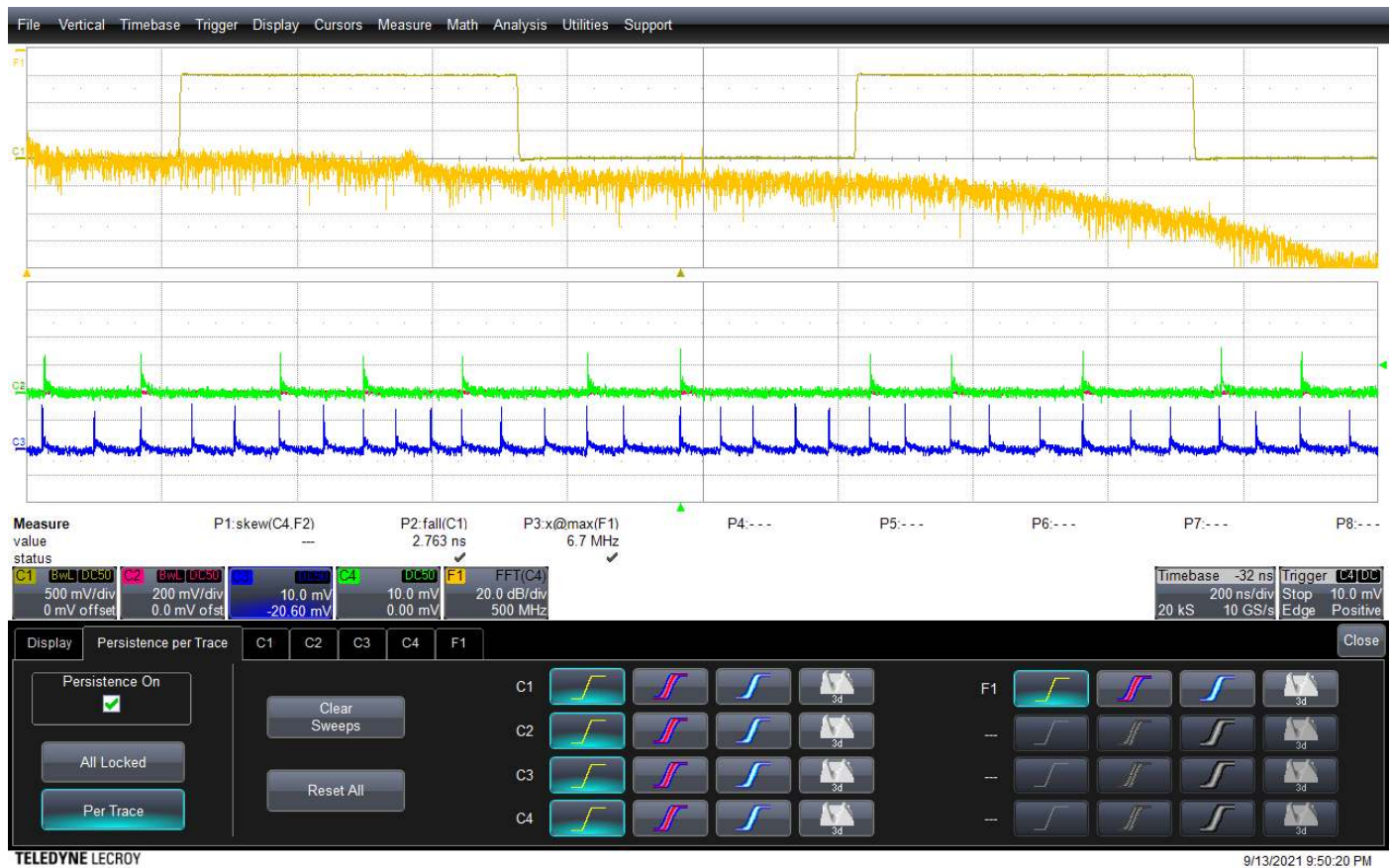
SPG613 nTron Counter

September 14, 2021

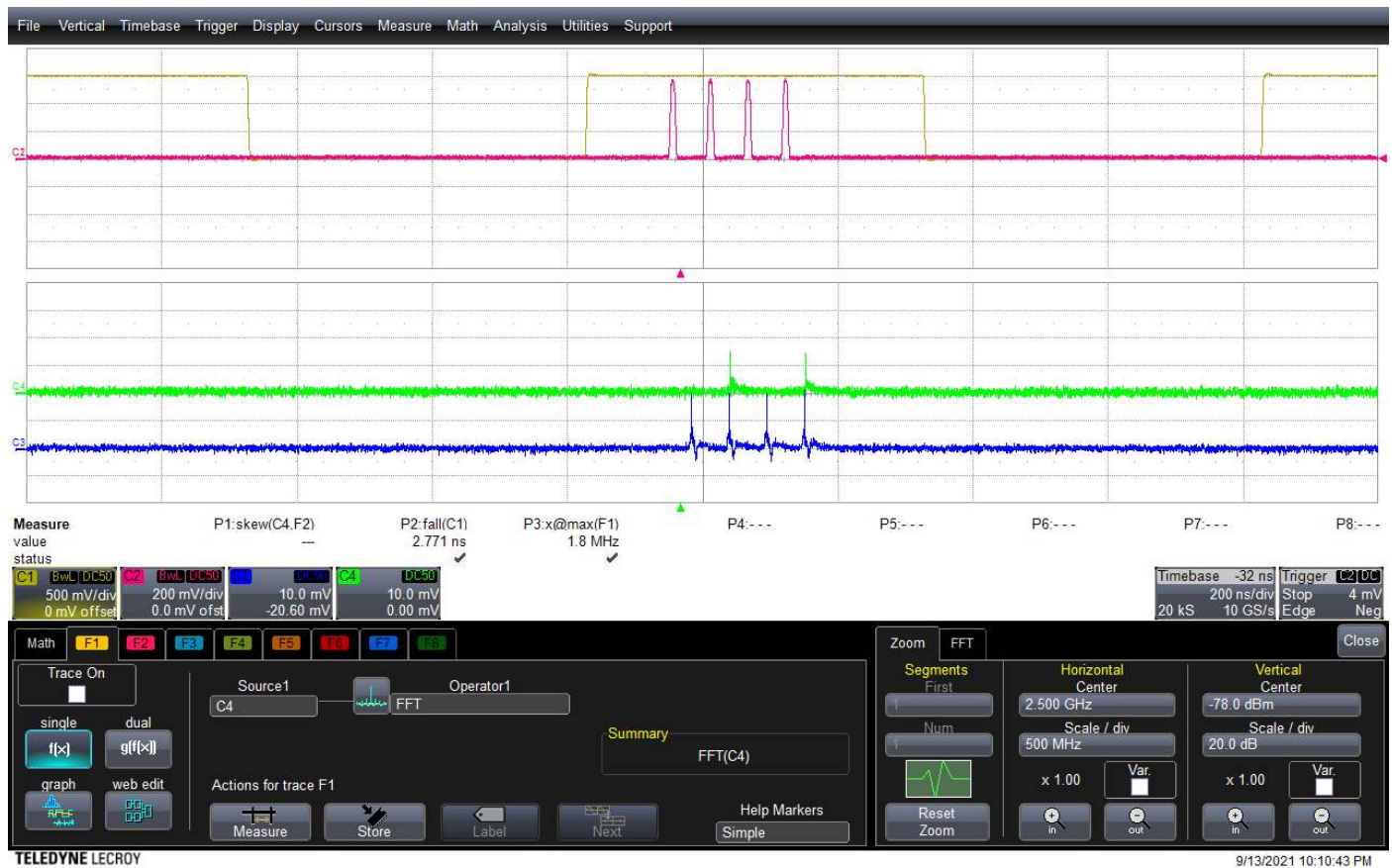
Categories: Electronics



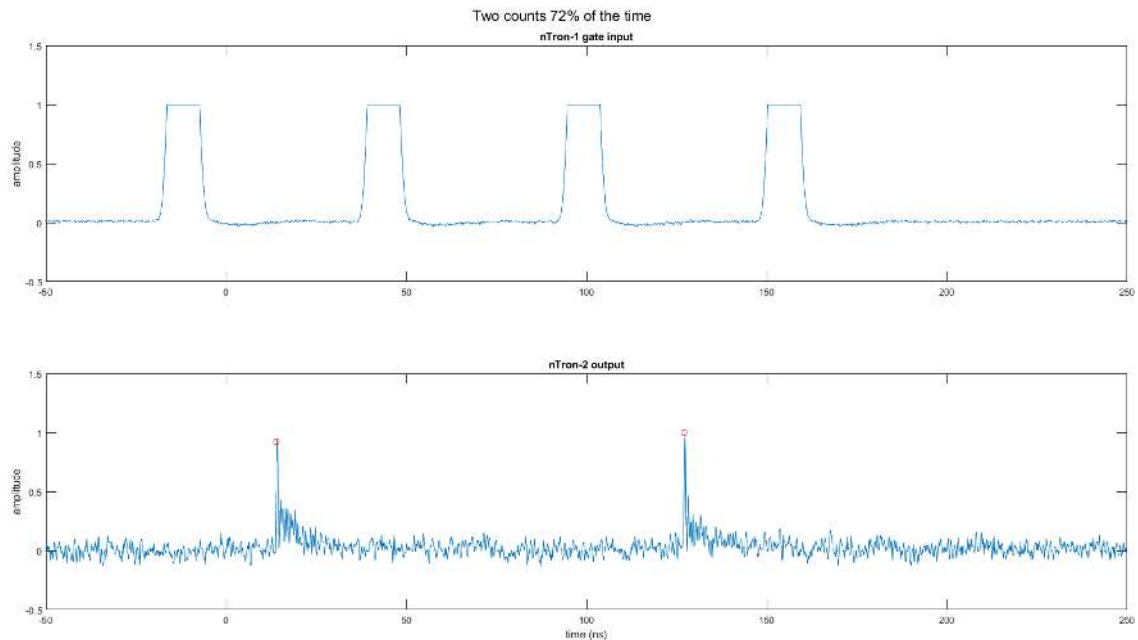
V1=12.4V V2=12.0V



$$V1=9.7V, V2=11.95, Vg=900mV$$



"working"



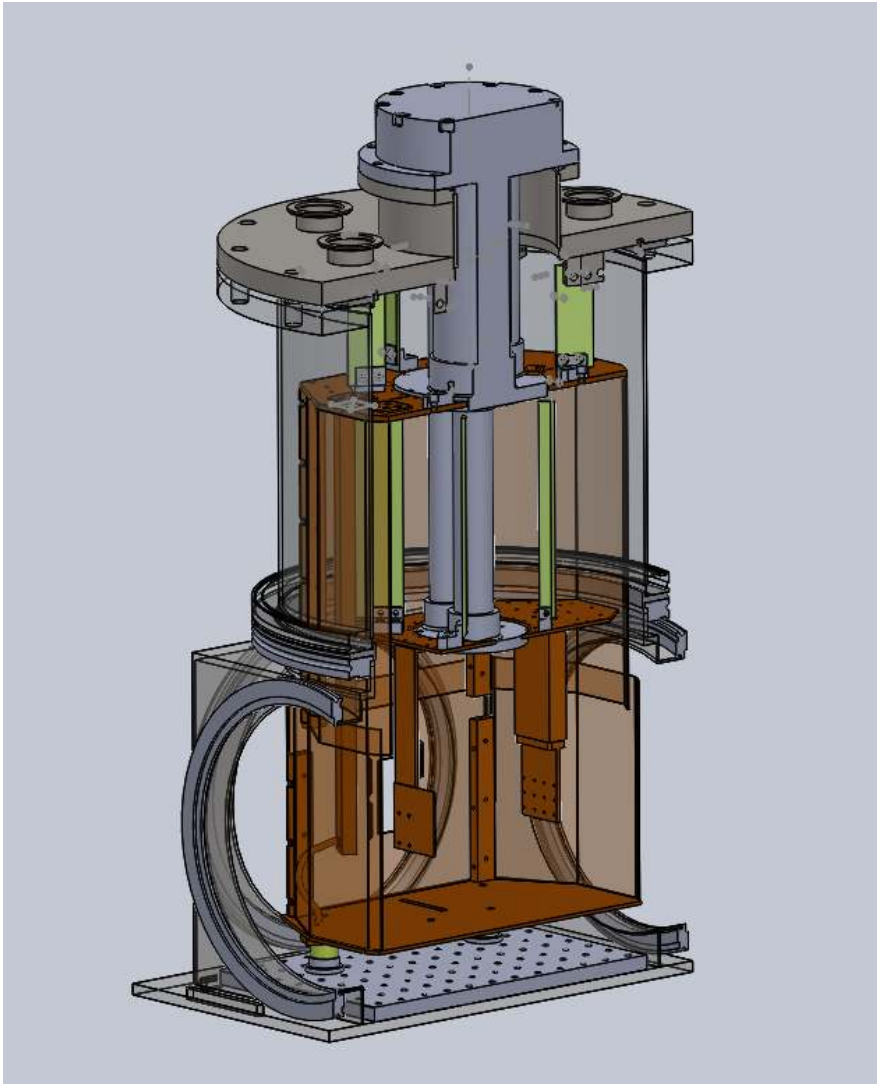
3 counts: 26%, 1 count 2%

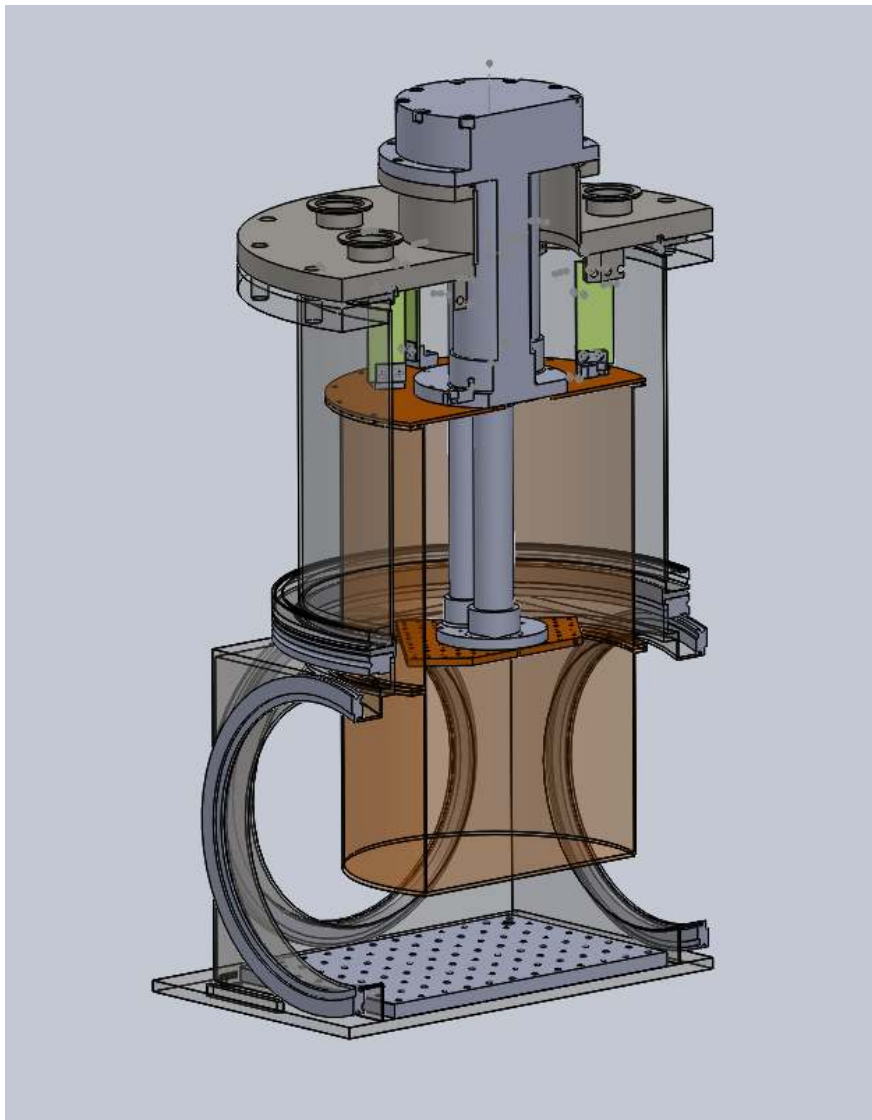
Future: Test storage time, seems like 10s+ will work

Free Space design review Oct-2021

October 4, 2021

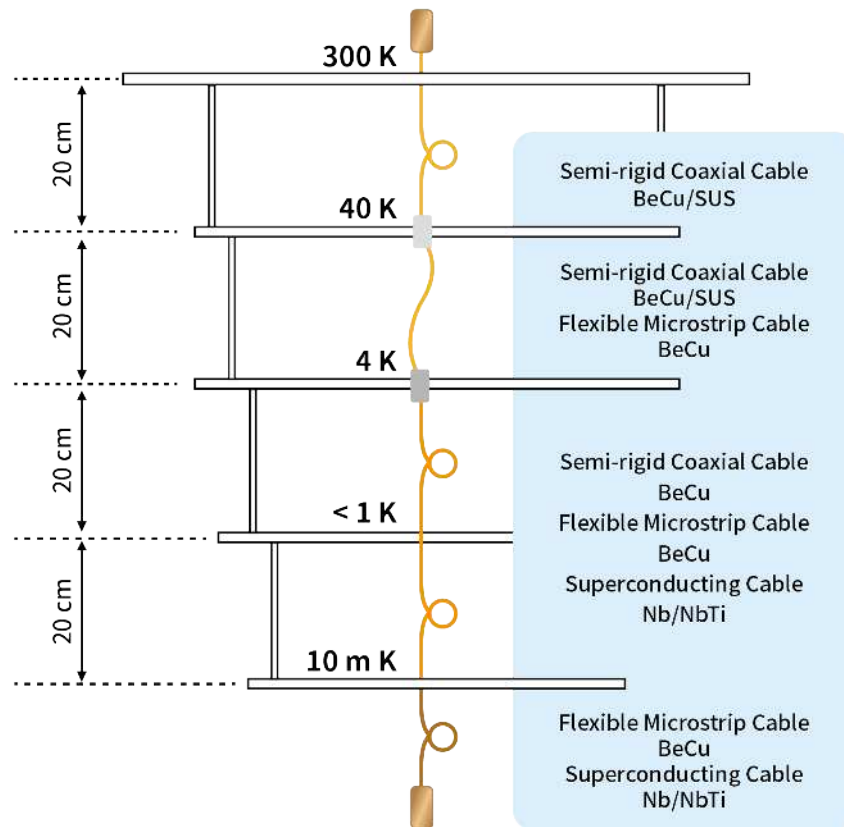
Categories: General





2021_Oct.zip

https://docs.google.com/presentation/d/1_s3IXlebmFAt-6DGOFB9JbNiNmnMgqy3w39FtH5Kp0/edit?usp=sharing

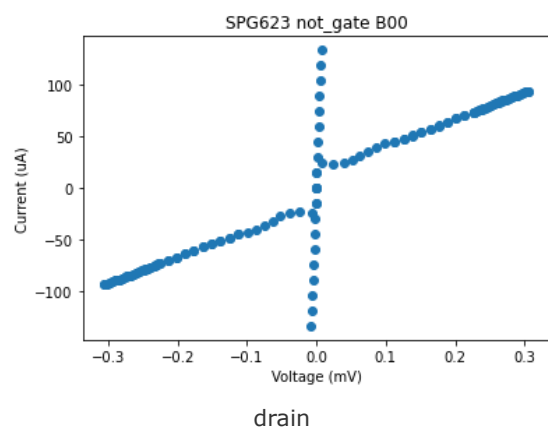
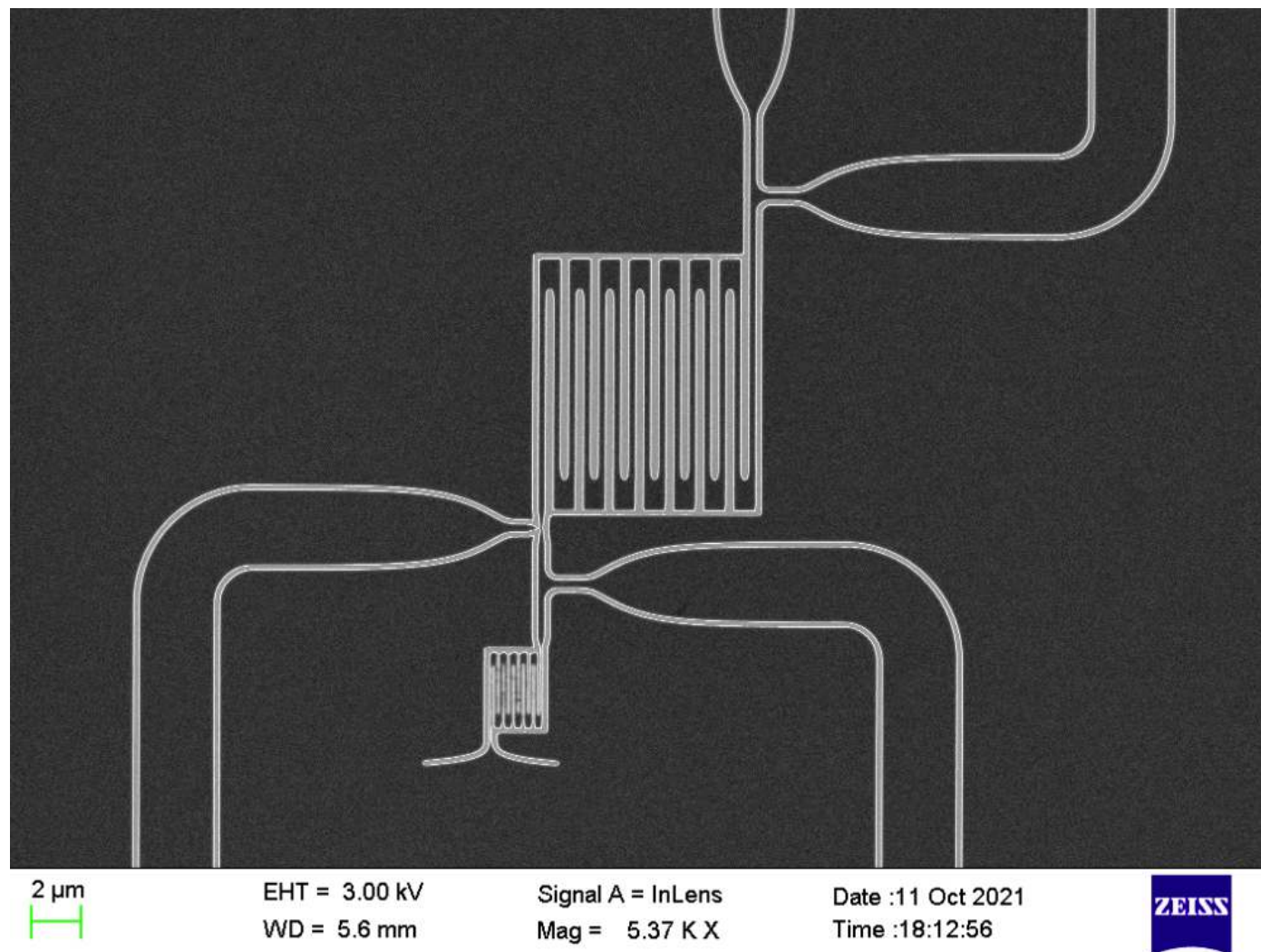


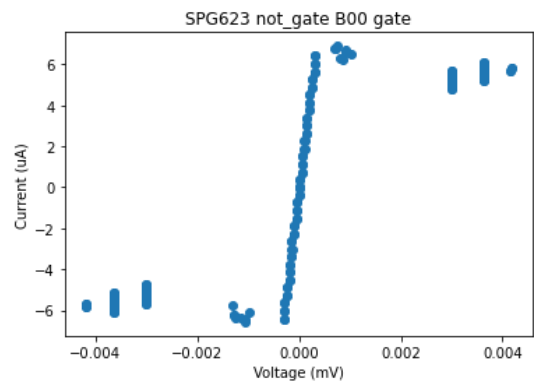
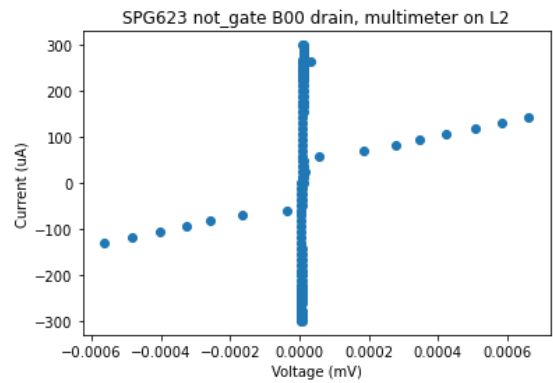
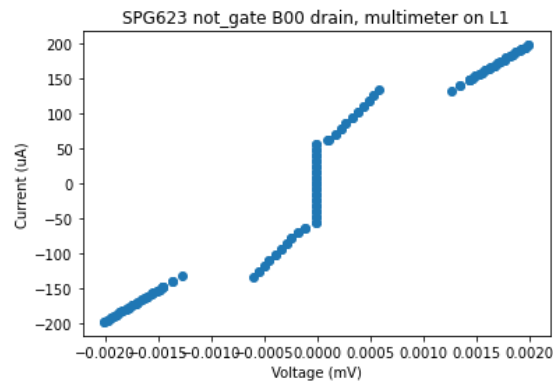
Precision Cryo can build parts. or MIT central.

SPG623 ntron not gate

October 23, 2021

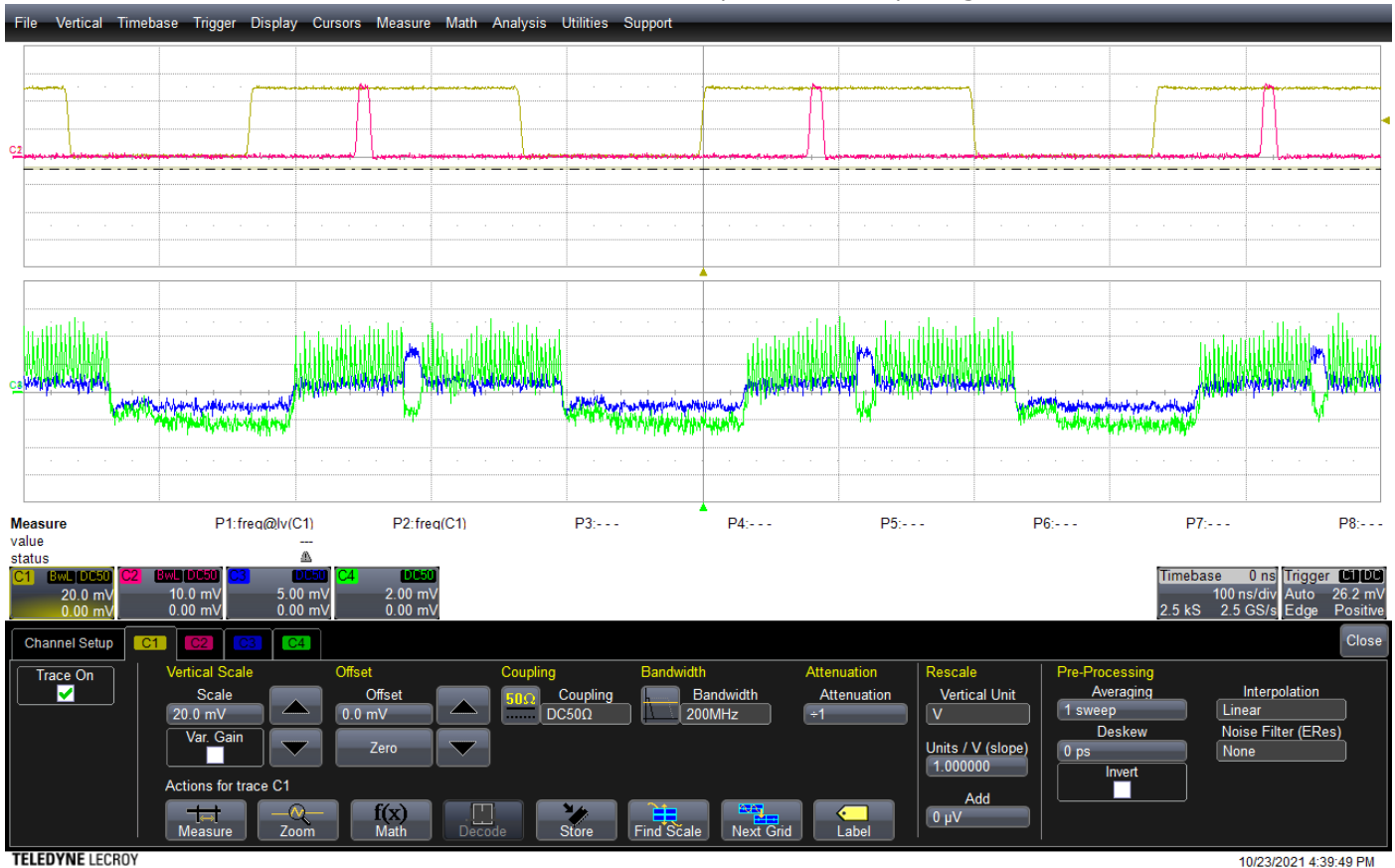
Categories: Electronics







L1:L2 = 100hm:100hm. 100μA to drain. 30μA to gate.



L1:L2 = 100hm:100hm. 100μA to drain. 50μA to gate.



L1:L2 = 100Ω:100Ω. 135μA to drain (max). 23μA to gate.



L1:L2 = 100Ω:100Ω. 150μA to drain (latching). 0μA to gate.



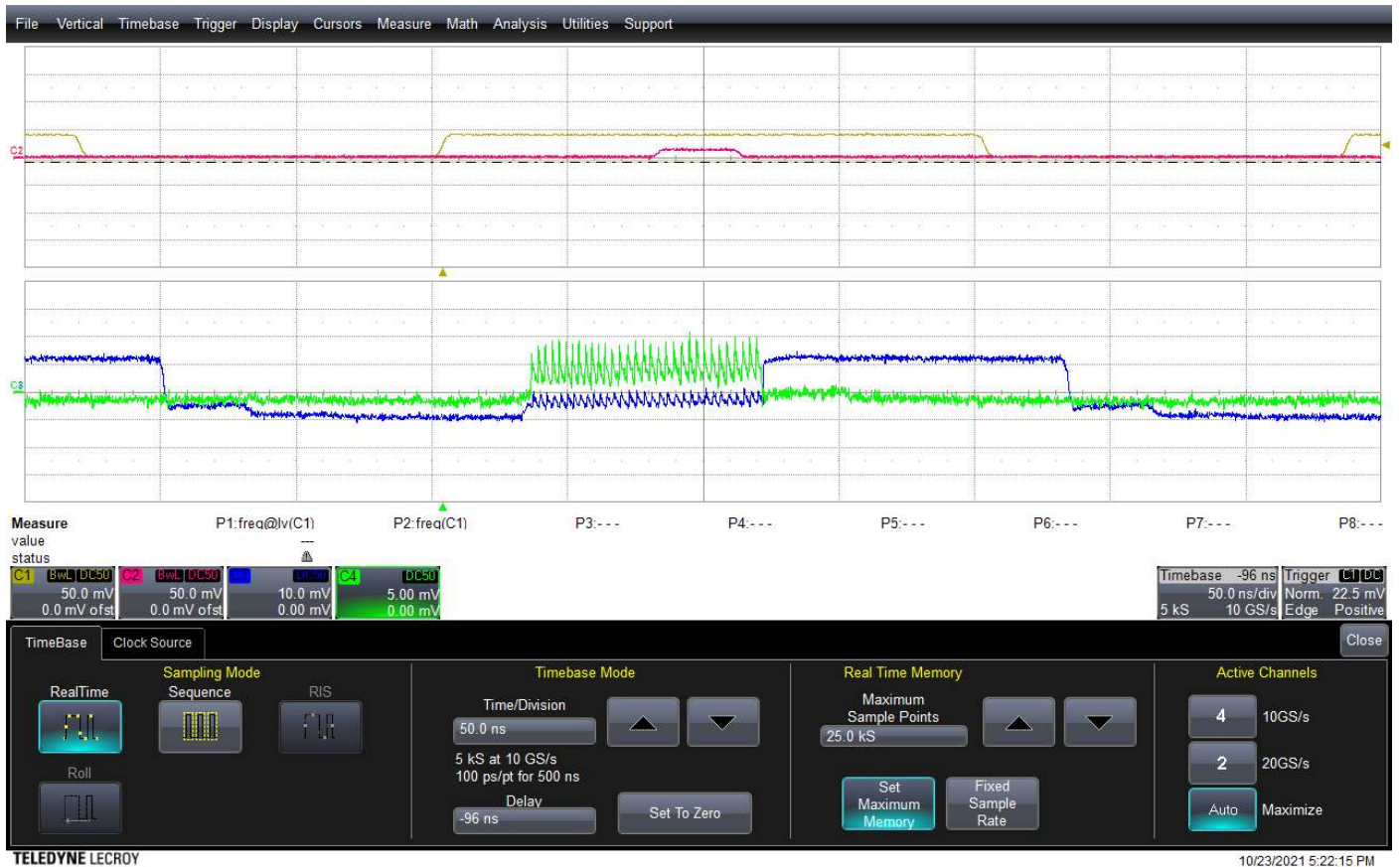
L1:L2 = 100hm:100hm. 110μA to drain (latching). 24μA to gate.

B04 showed similar operation but the choke/channel did not have any gain.

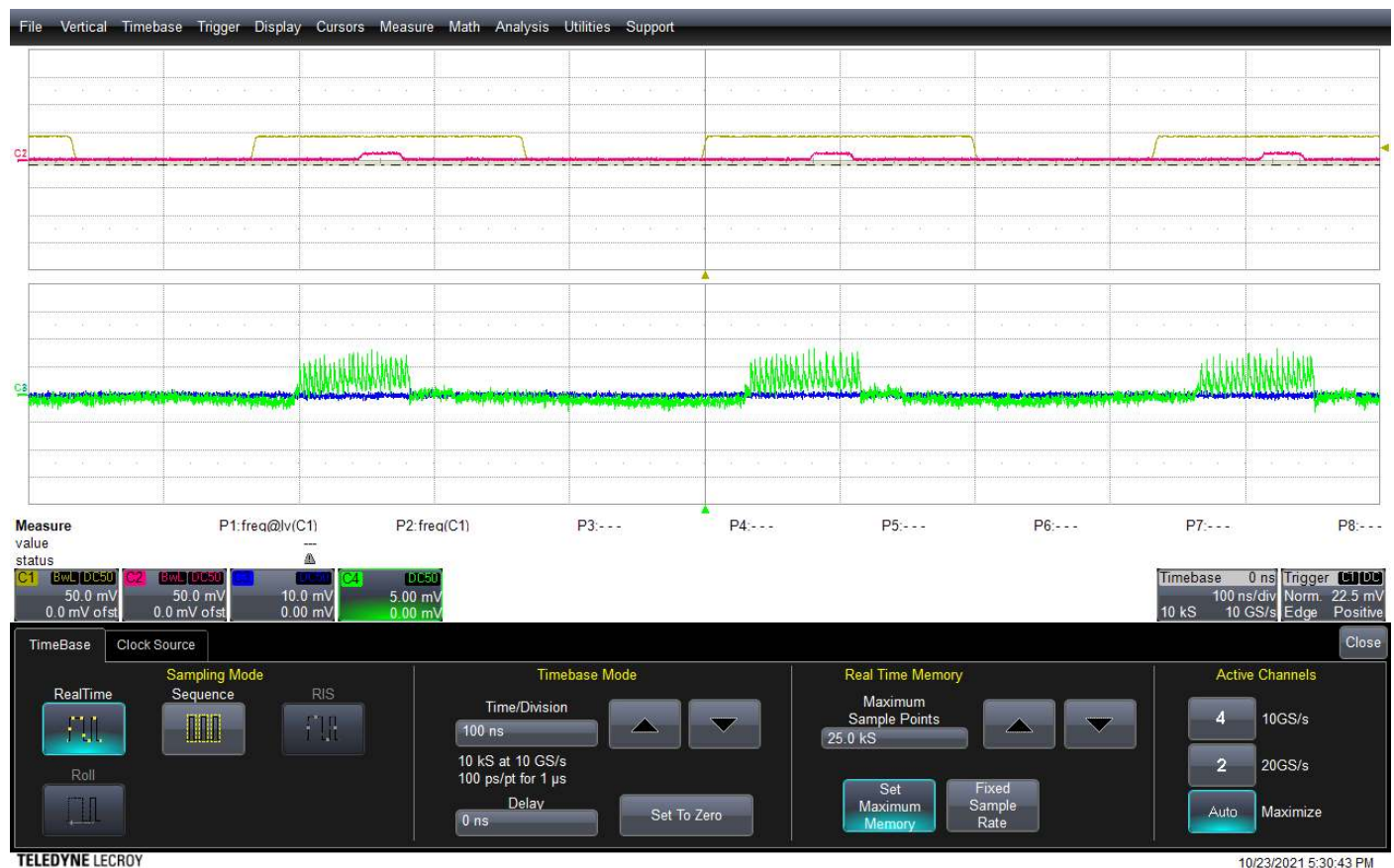
B03



L1:L2 = 500hm:200hm. 82 μ A to drain (latching). 28 μ A to gate.



L1:L2 = 500hm:200hm. 82 μ A to drain (latching). 28 μ A to gate.

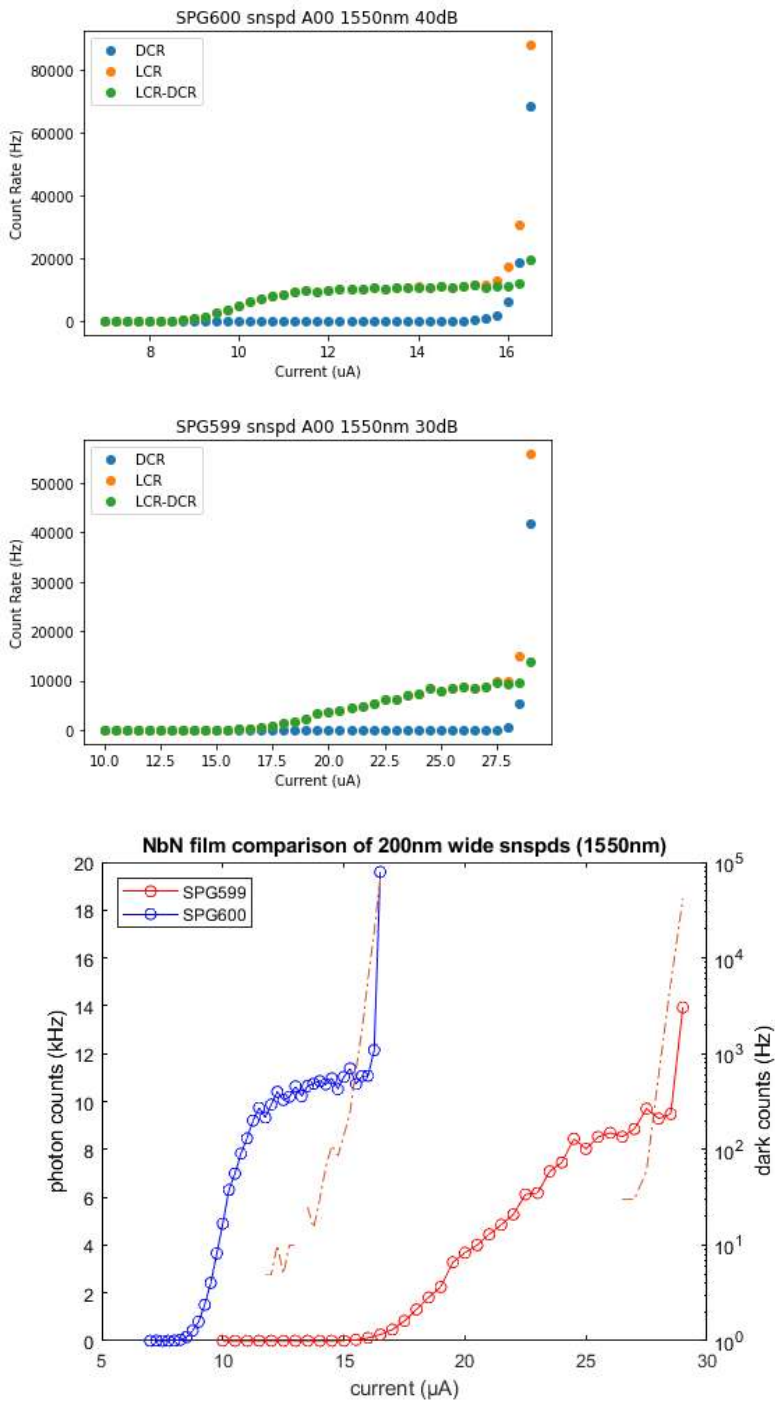


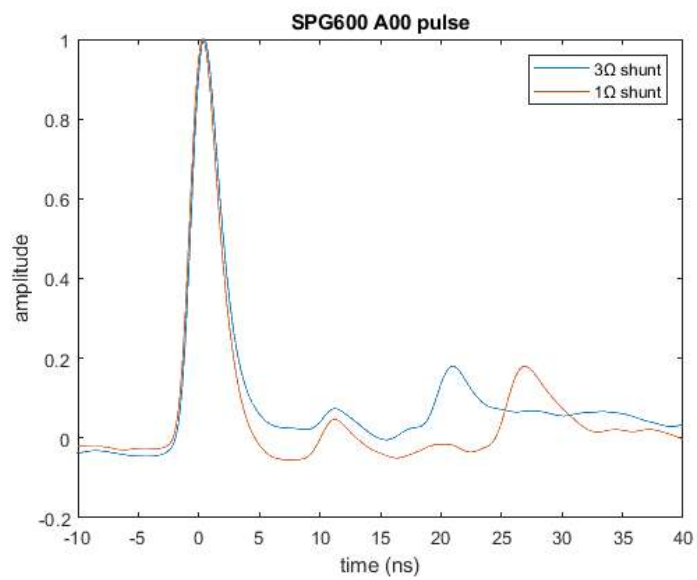
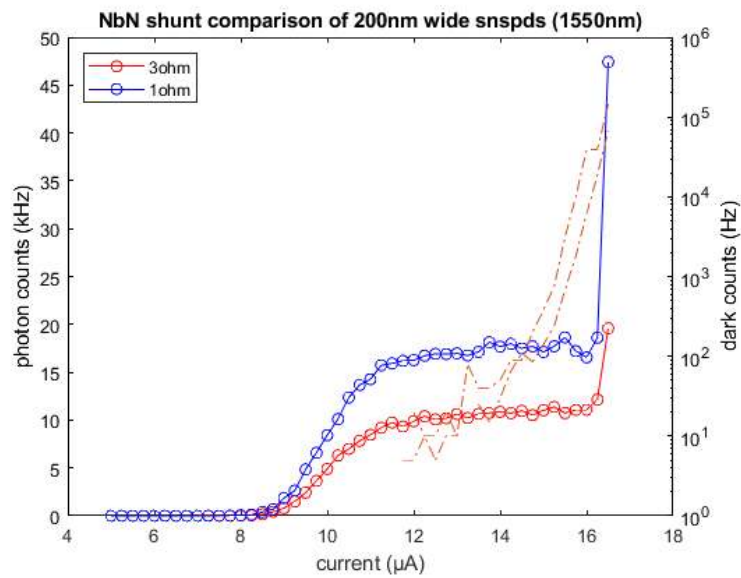
L1:L2 = 100Ohm:100Ohm. 86 μ A to drain (latching). 23 μ A to gate. Notice no voltage on L1.

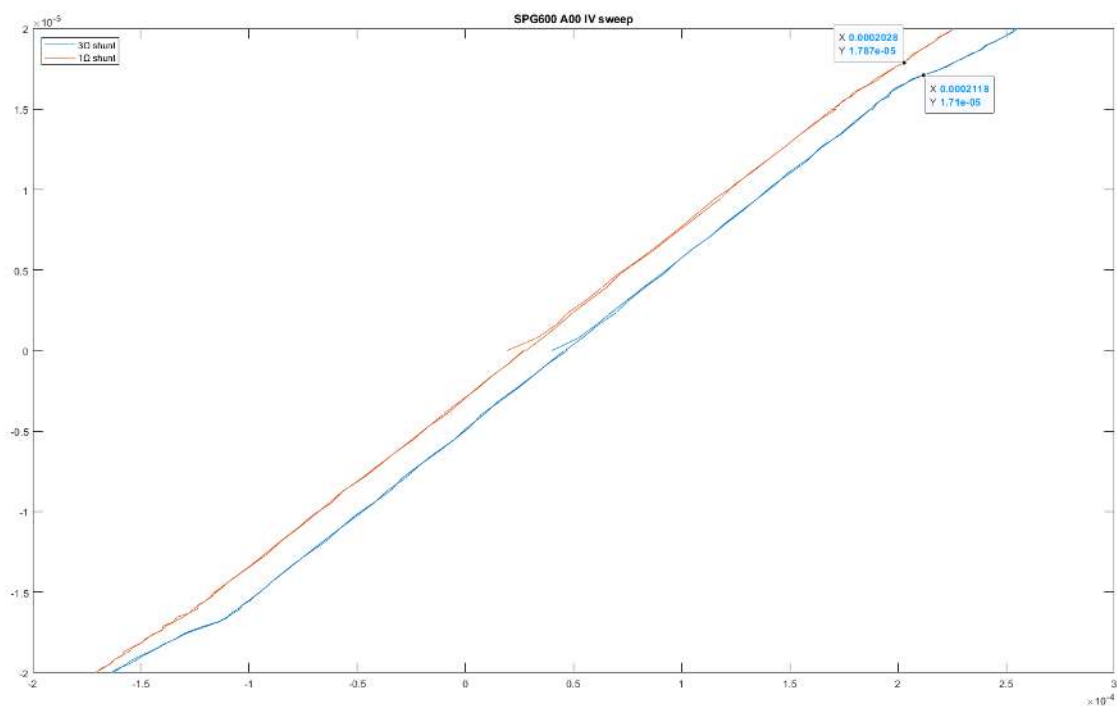
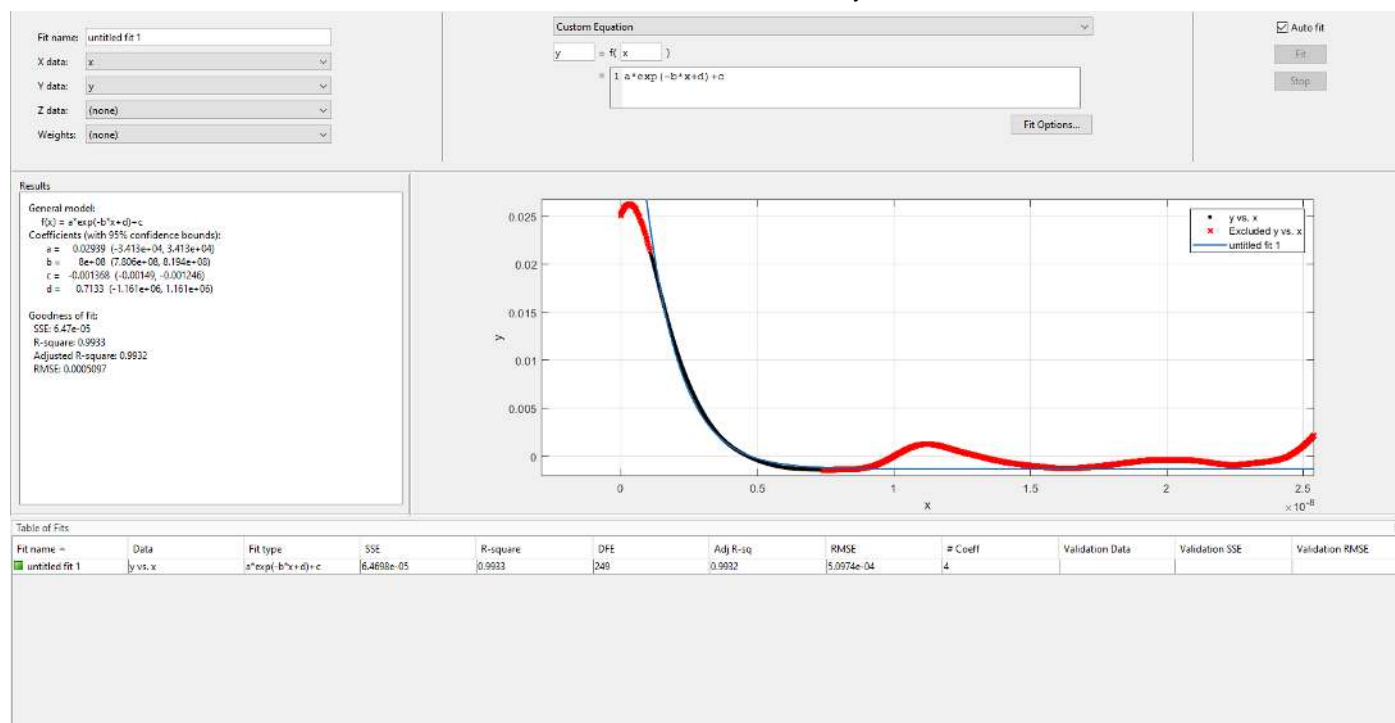
Wide wire material comparison SPG599, SPG600

October 26, 2021

Categories: SNSPD







$$L_{k,s} = 1.378 \left[\frac{\text{pH K}}{\Omega} \right] \frac{R_s}{T_c}$$

```
>> qf.kinetic_inductance_rs(521, 6)
```

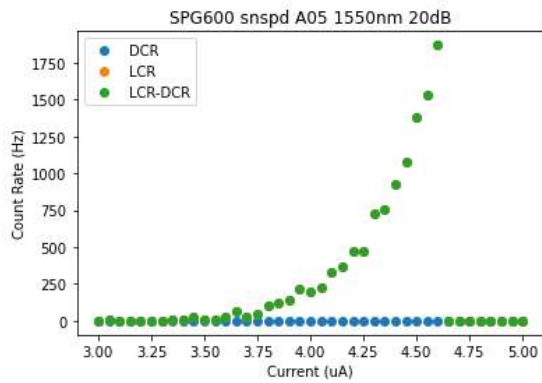
SPG599 ans =

119.6563 pH/sq

```
>> qf.kinetic_inductance_rs(700, 4.7)
```

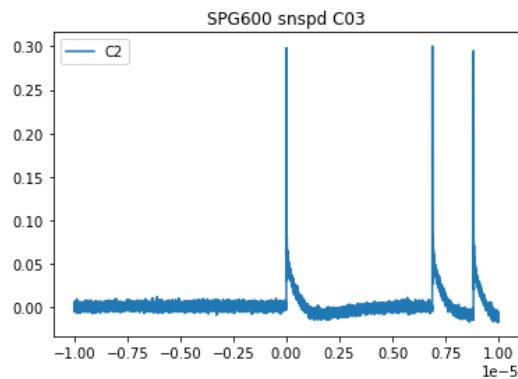
SPG600 ans =

205.2340 pH/sq

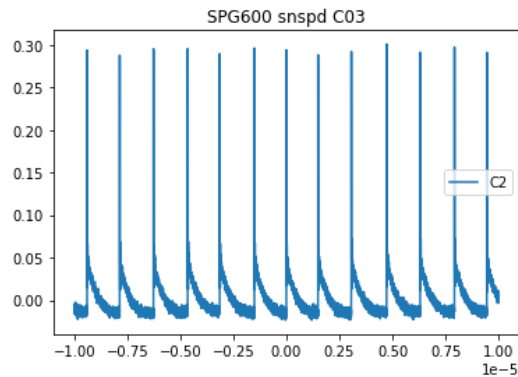


device without shunt. SPG599 A05 did not have any pulse. just latched

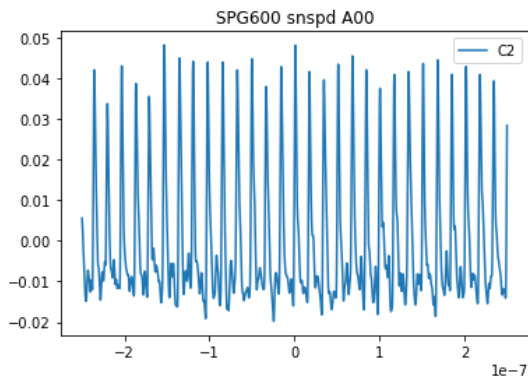
Larger devices are operating in a way I do not understand.



Light on 0db (1550nm) seems like there are regular counts, either light or dark. By regular I mean not relaxation oscillations



Light off 100db, blanked. Device has relaxation oscillations. Frequency is a max of 1.2MHz. It is possible that having the laser on (50Mhz repetitions) quenches/destroys the relaxation oscillations. I need to push the oscillations back by reducing the shunt resistance $3\Omega \rightarrow \sim 1\Omega$



For the smaller wire that has saturated detection efficiency, the max repetition rate is
~60MHz

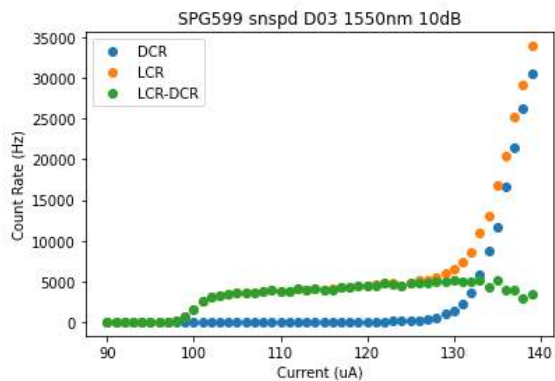
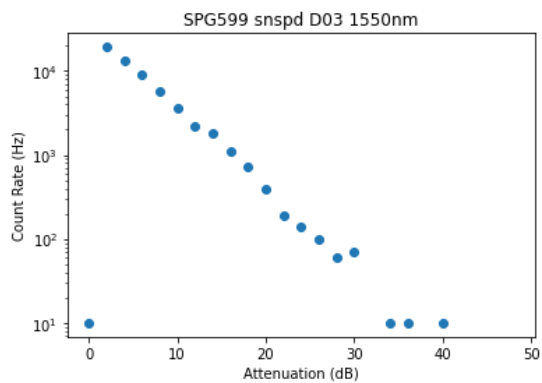
I need to find the Lk to Rshunt ratio that worked for the narrow wires and replicate that for the larger wires.

A00: $\text{Squares/Rshunt} = 850/(10\text{ohm}, 30\text{ohm}) = 850, 283$

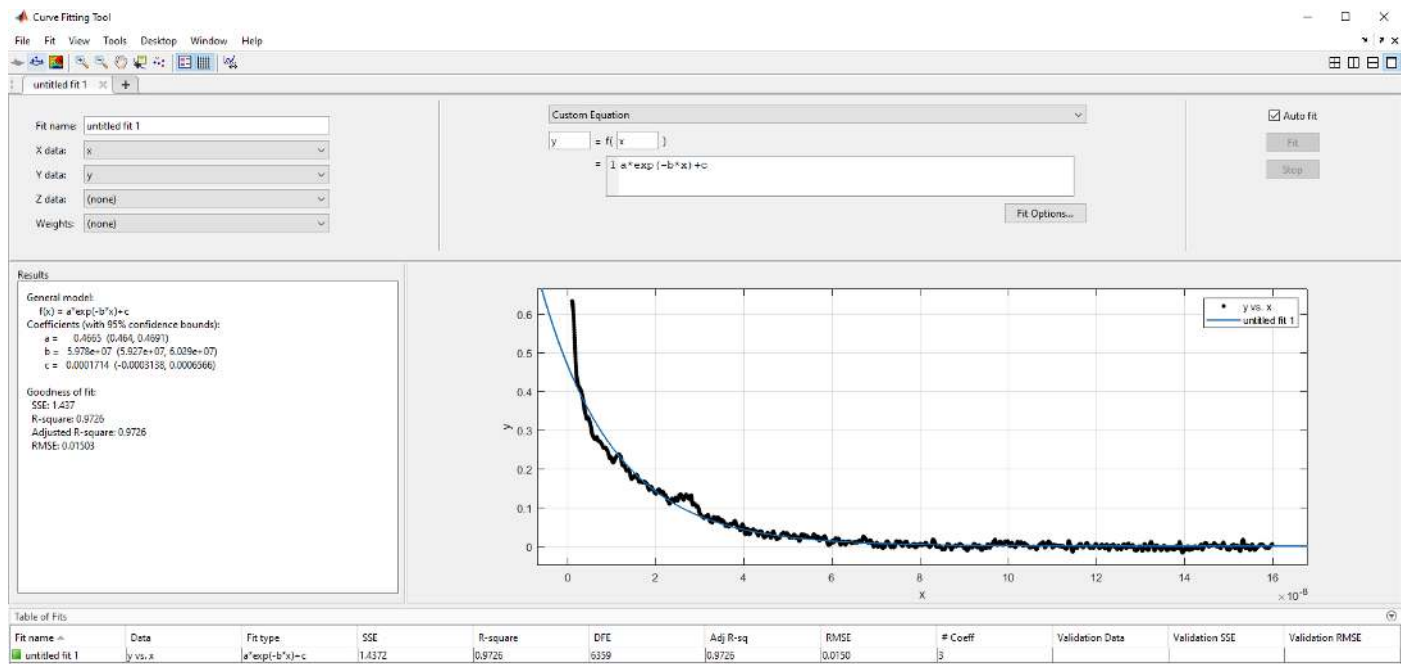
D00: $9100/(850, 283) = 10\text{ohms}, 32\text{ohms}$

D03: $31633/(850, 283) = 37\text{ohms}, 111\text{ohms}$

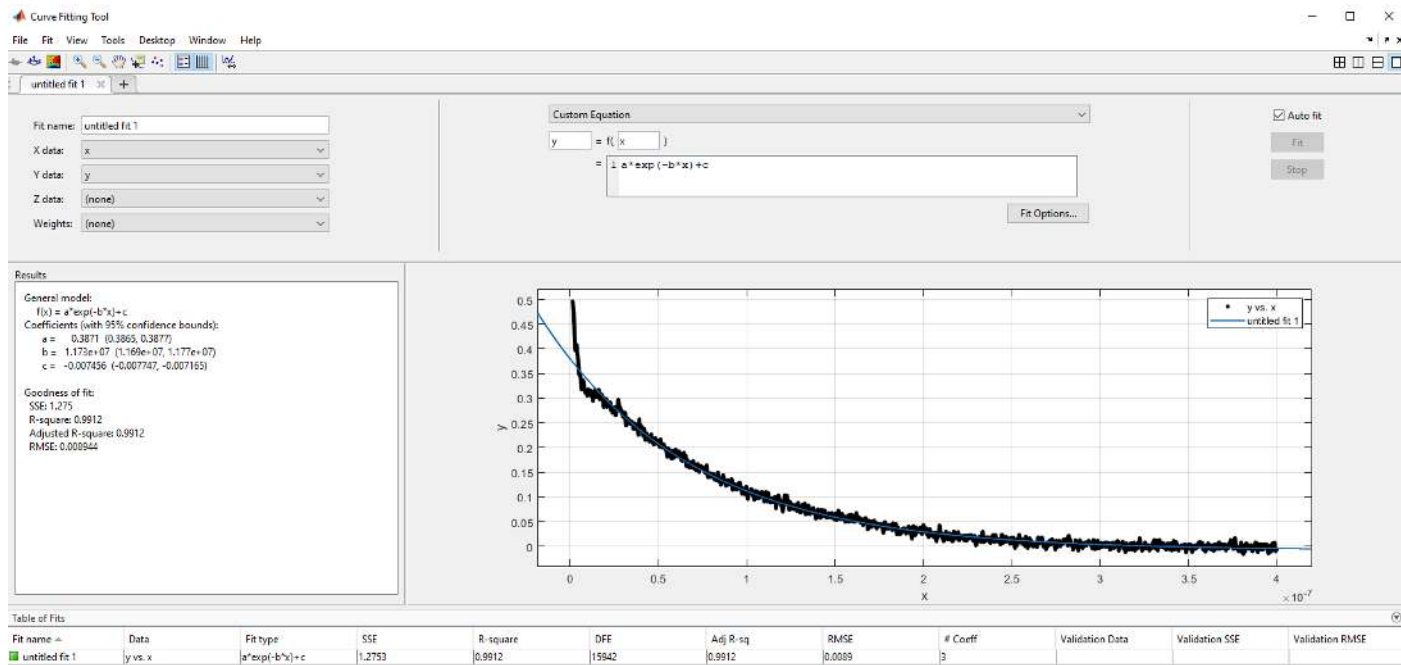
D04: $42500/(850, 283) = 50, 150$



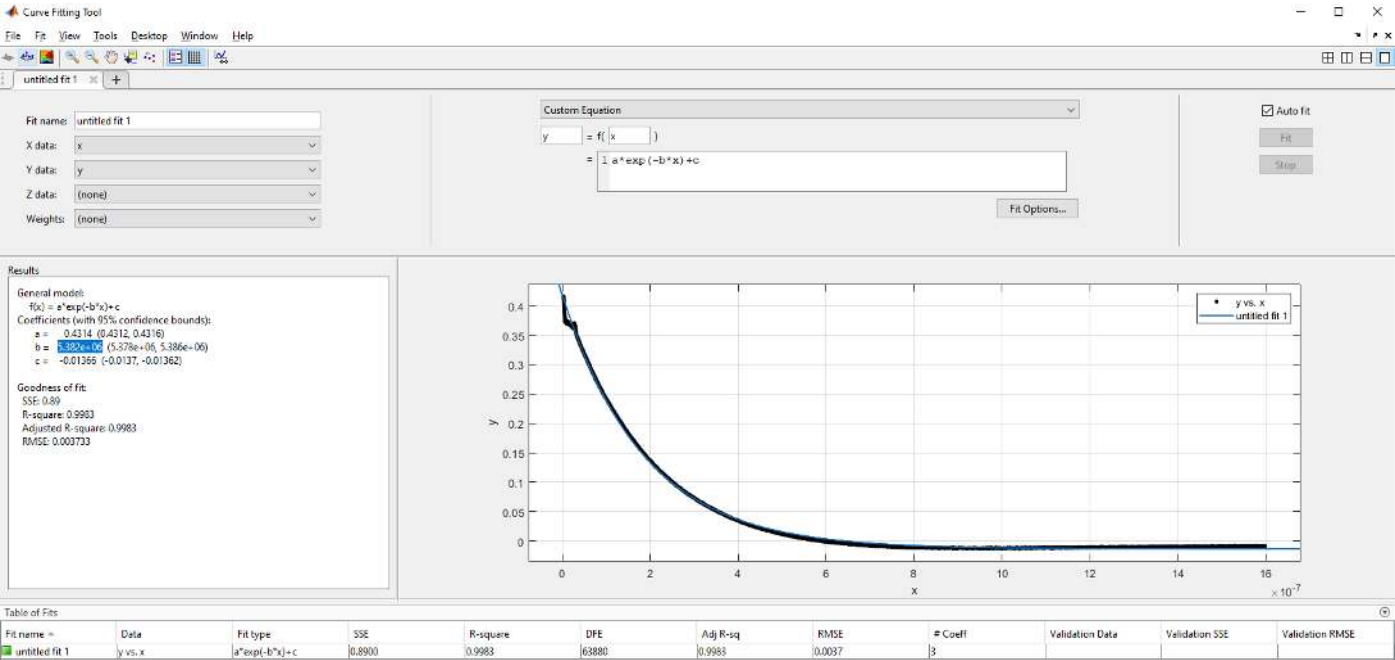
Pulse Trace fitting for inductance 100ohm shunt. SPG600.



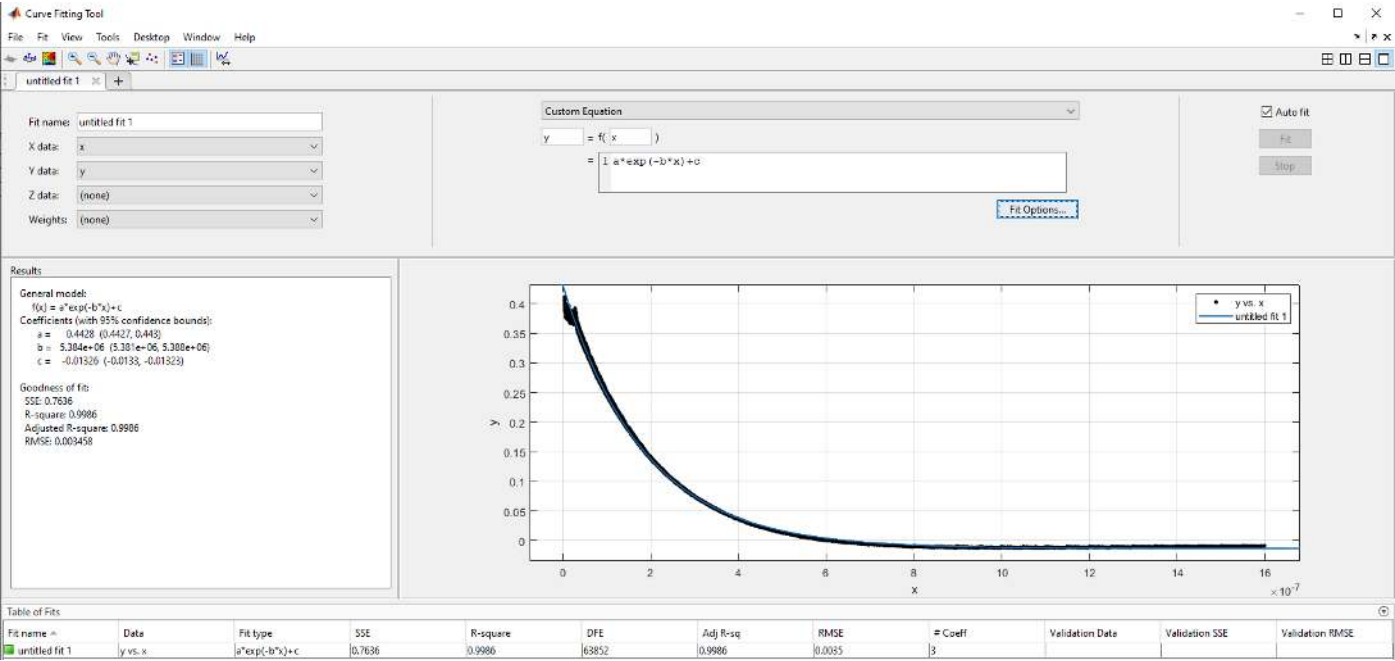
C00



C02



C04



D00

SPG599 D03 wide wire nbn

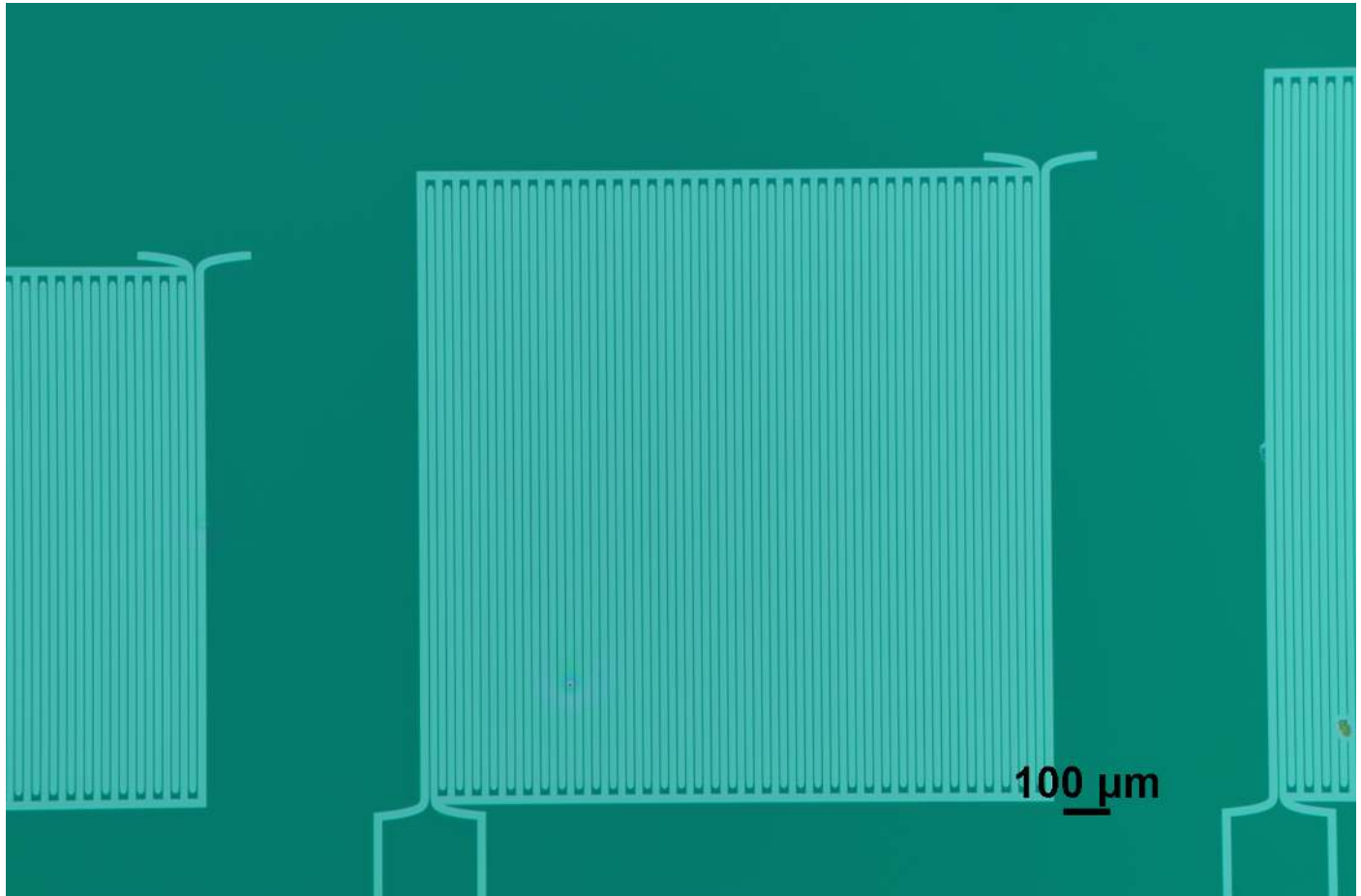
October 26, 2021

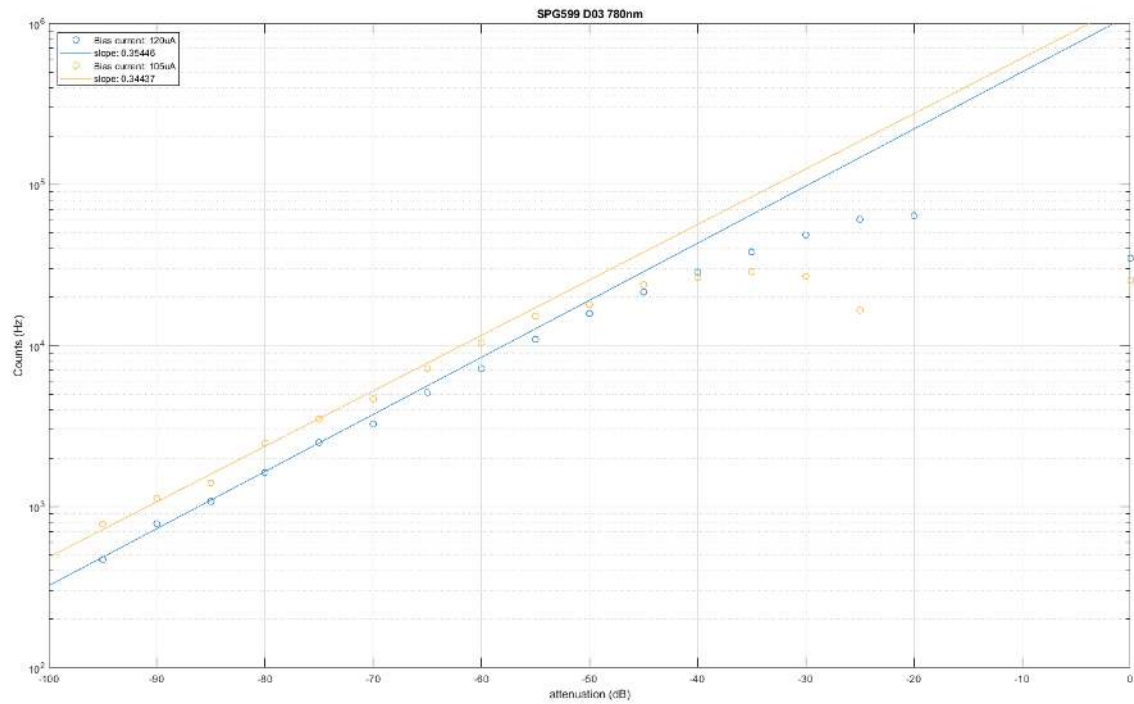
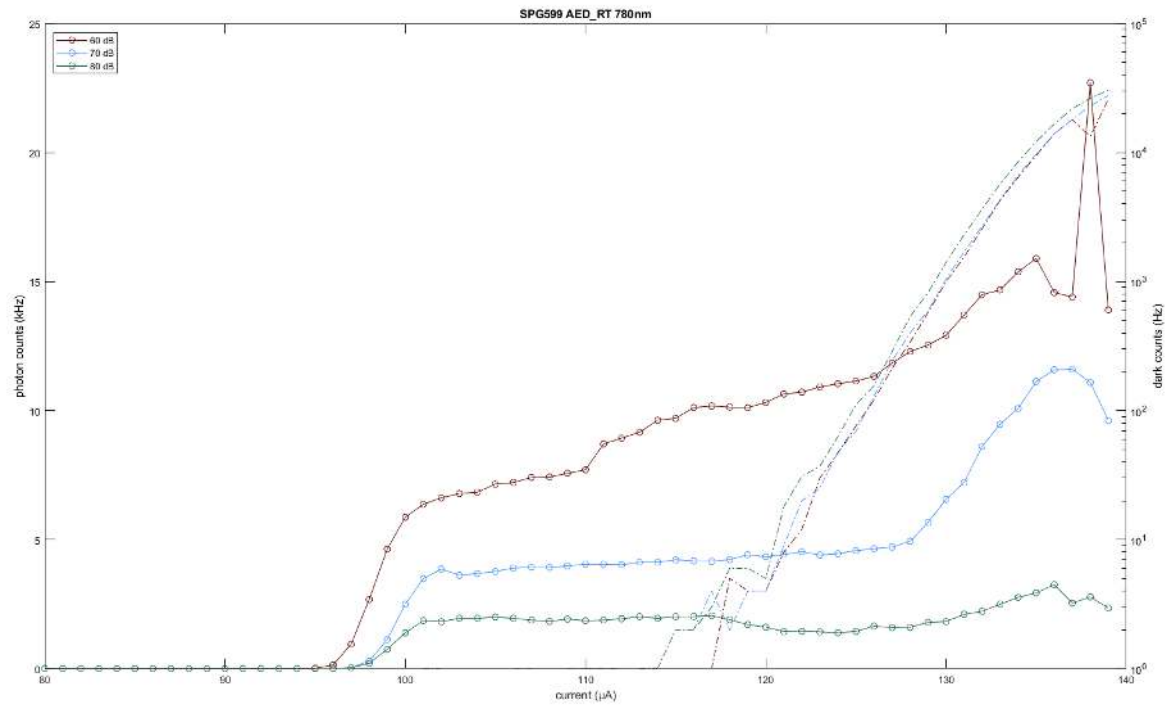
Categories: General

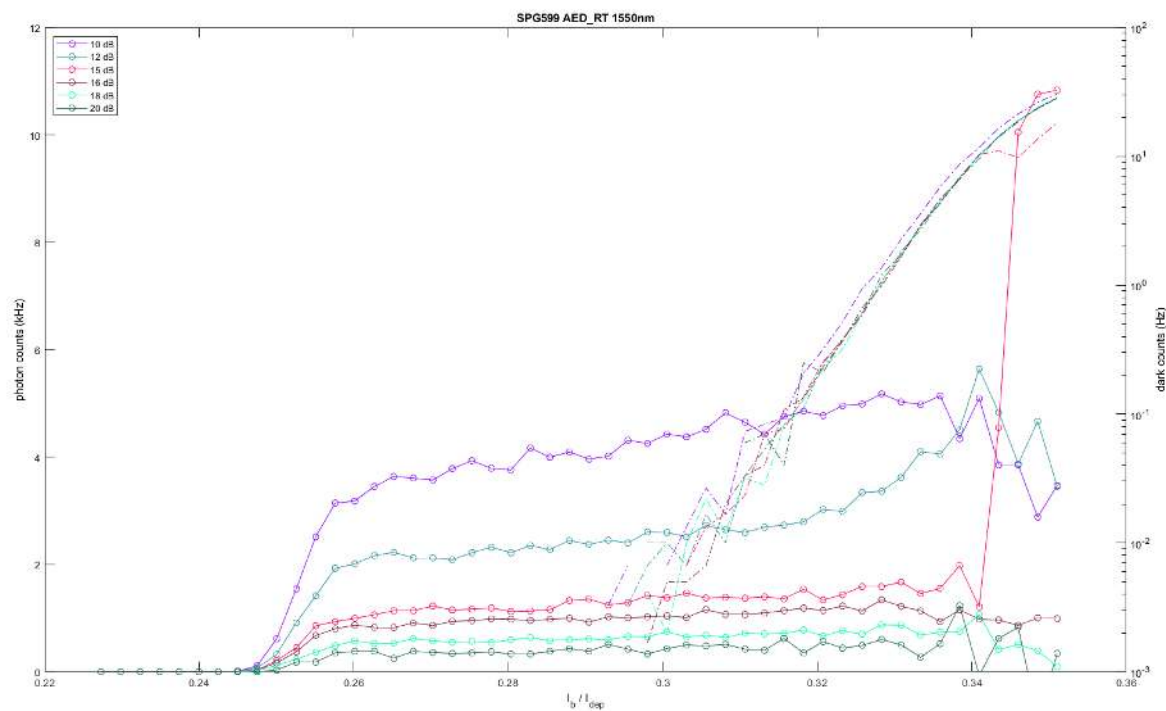
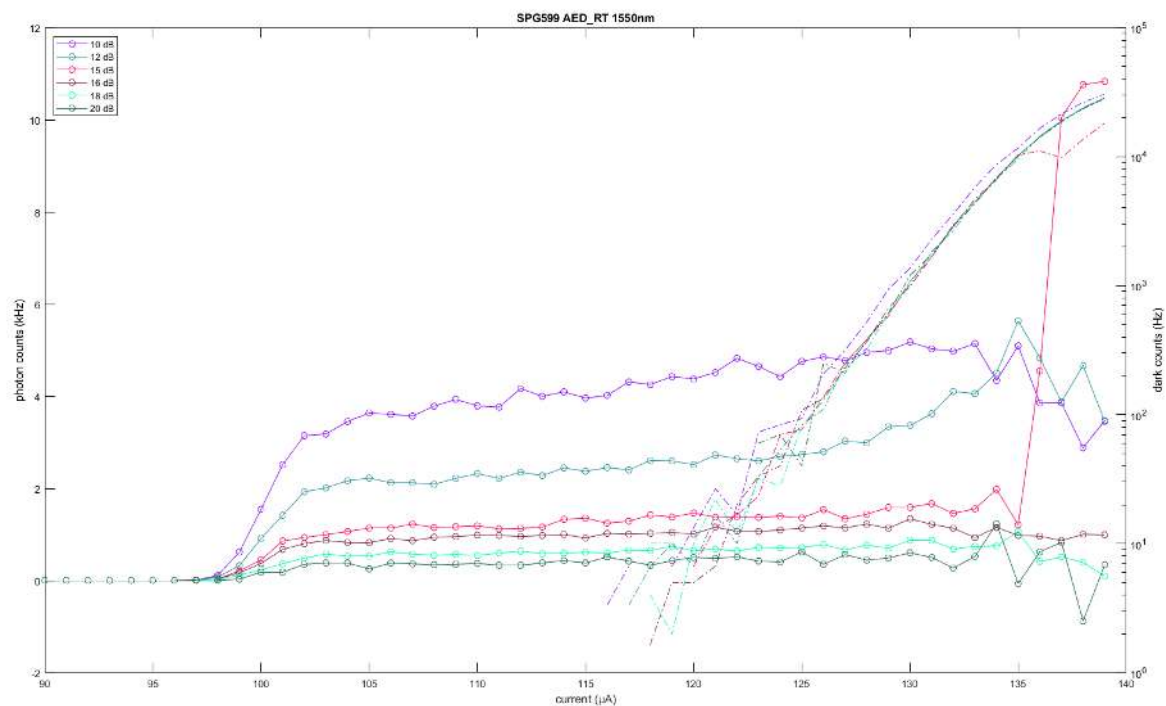
1.35mm², 3um wide, 20% fill factor, 31633squares, 3.764μH

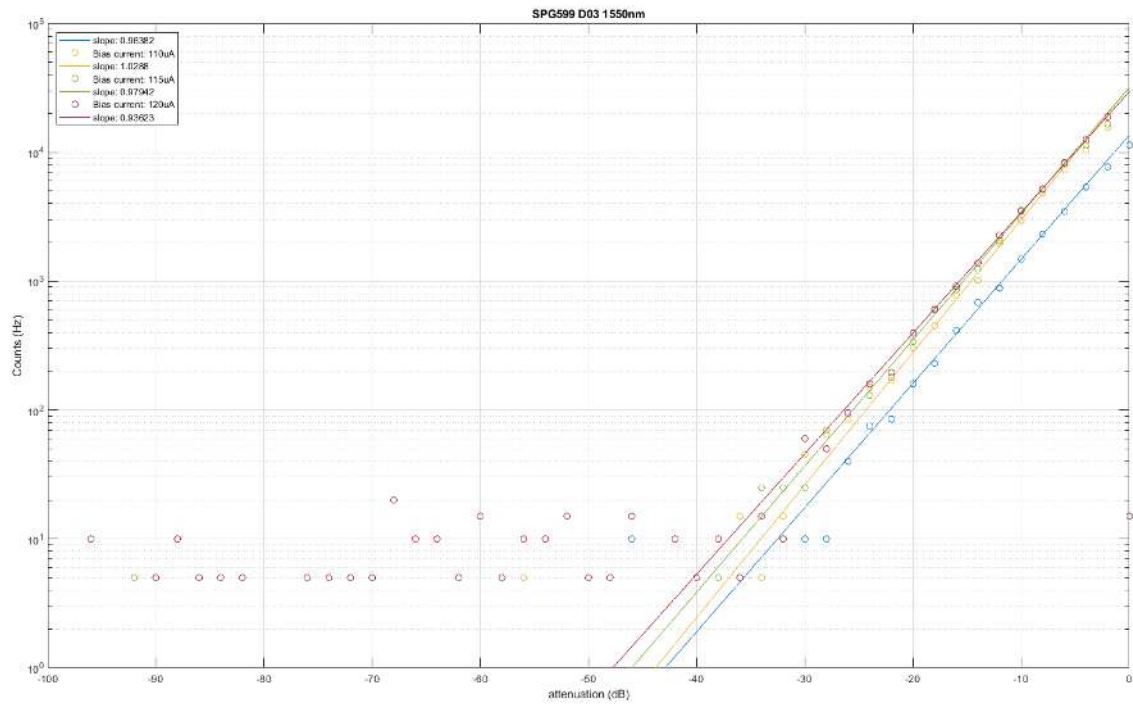
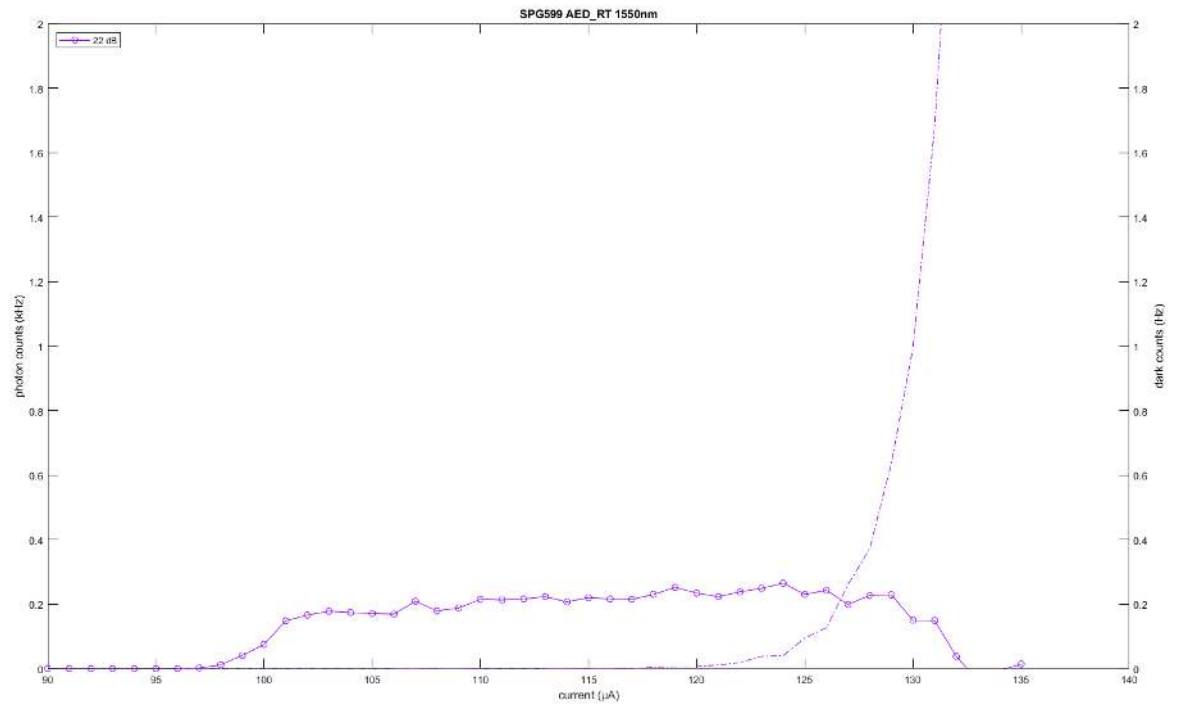
L/R = 3764ns

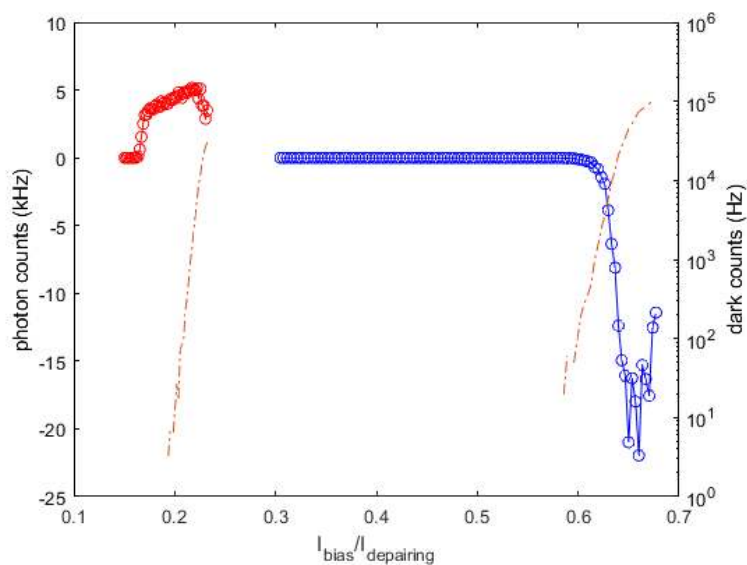
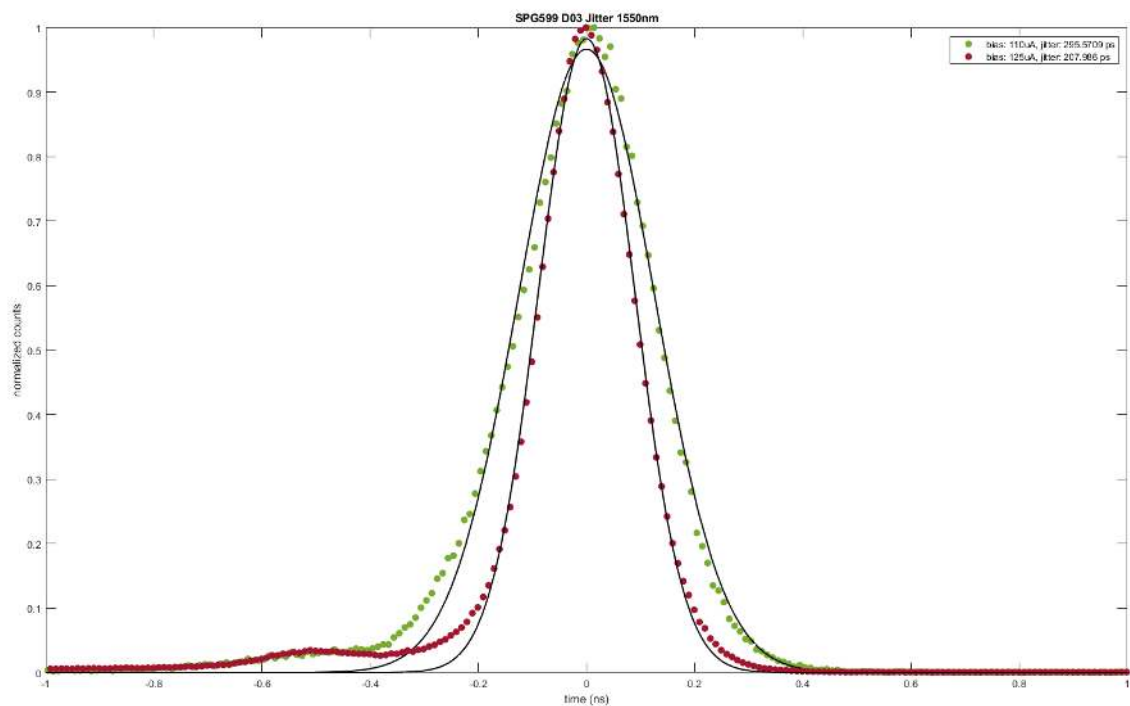
For SPG600 : (200pH/sq*31633)/3764ns = 1.64Ohms











RED: SPG599 D03 (the device presented above) BLUE: SPG600 D03.

It does not show any photon counts under the same illumination

however, the dark counts appear at a much higher bias current.

Devices C-D are all $3\mu\text{m}$ wide. with the following number of squares

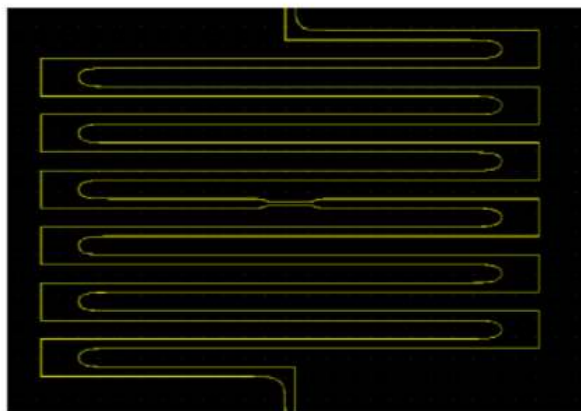
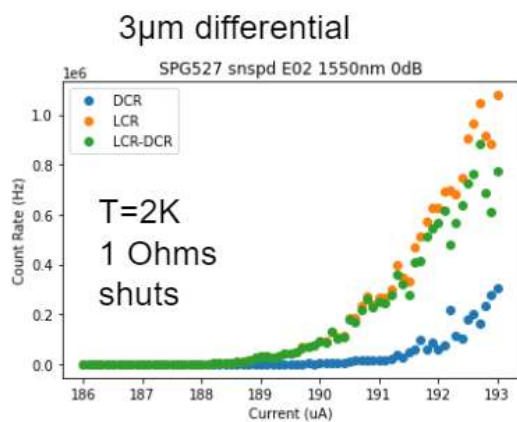
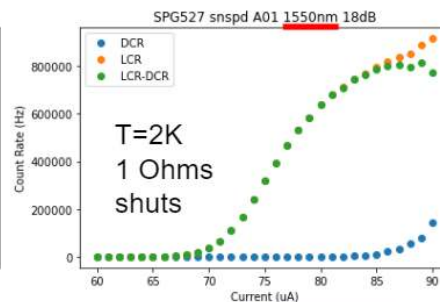
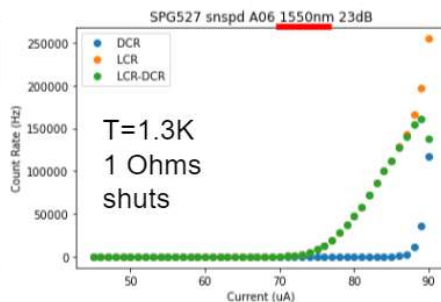
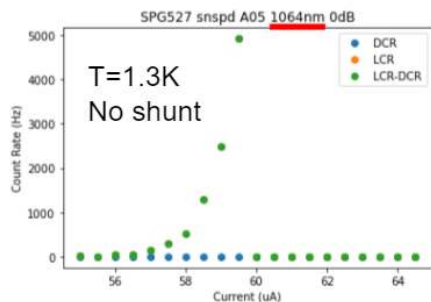
C;D

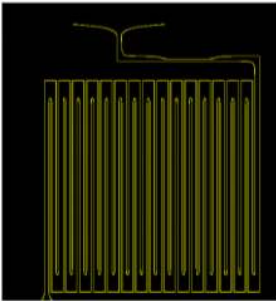
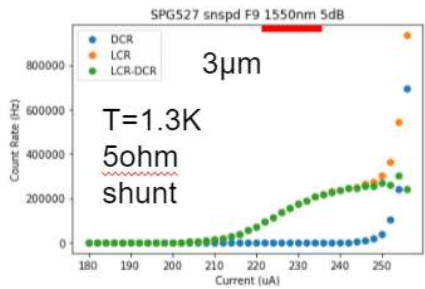
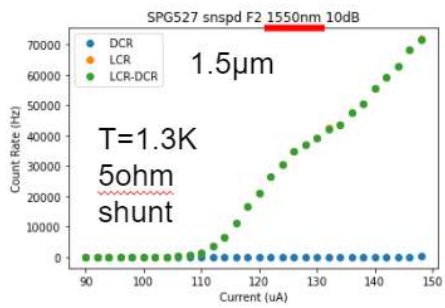
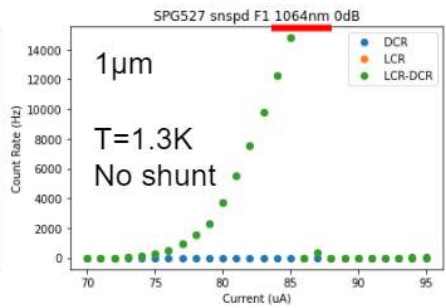
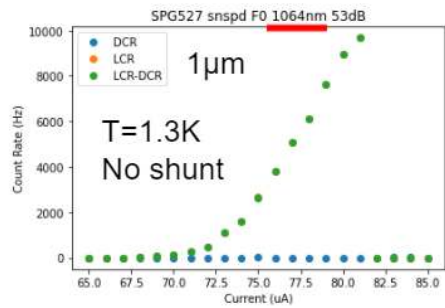
SPG527 wide wire nbn – part 2

October 26, 2021

Categories: General

[Previous post](#)





n

Wide Wire Deep Dive

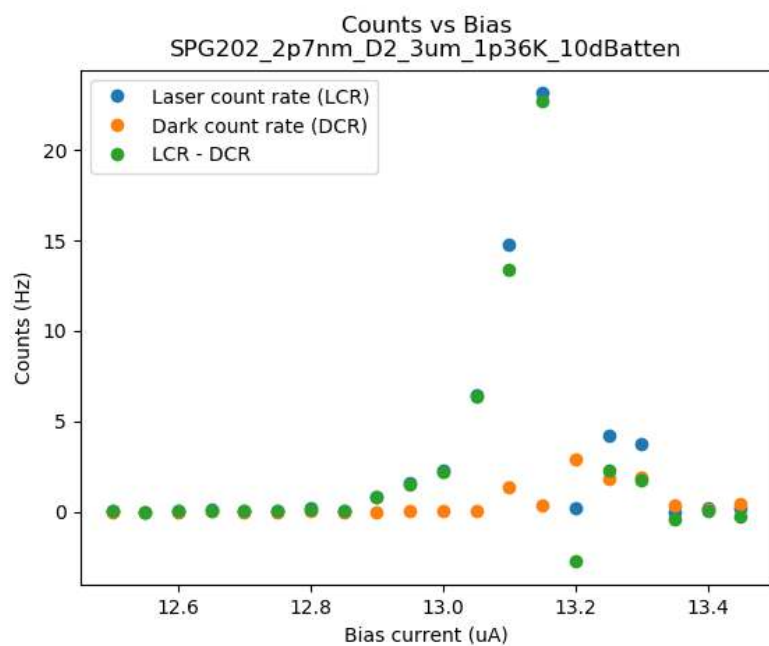
October 26, 2021

Categories: SNSPD

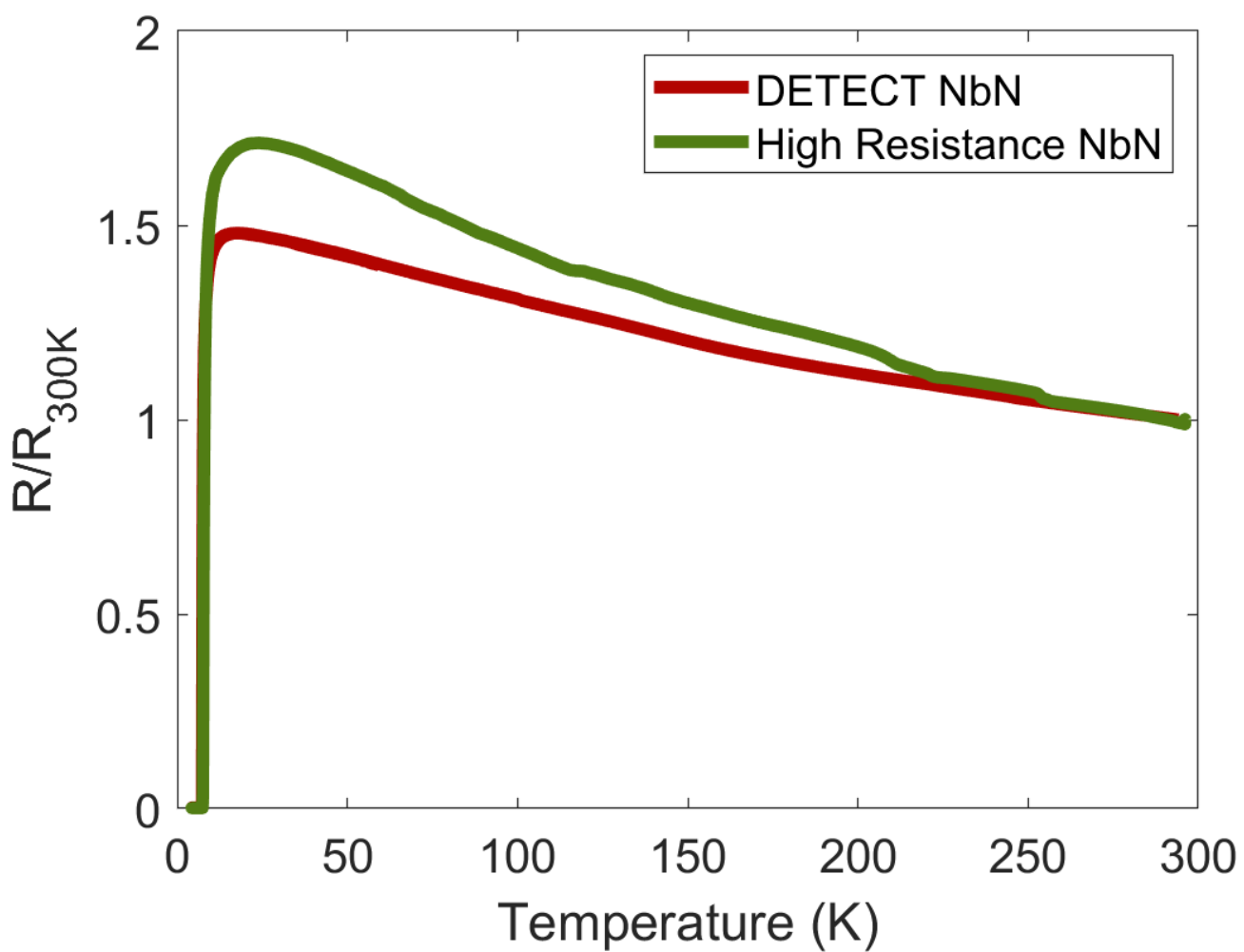
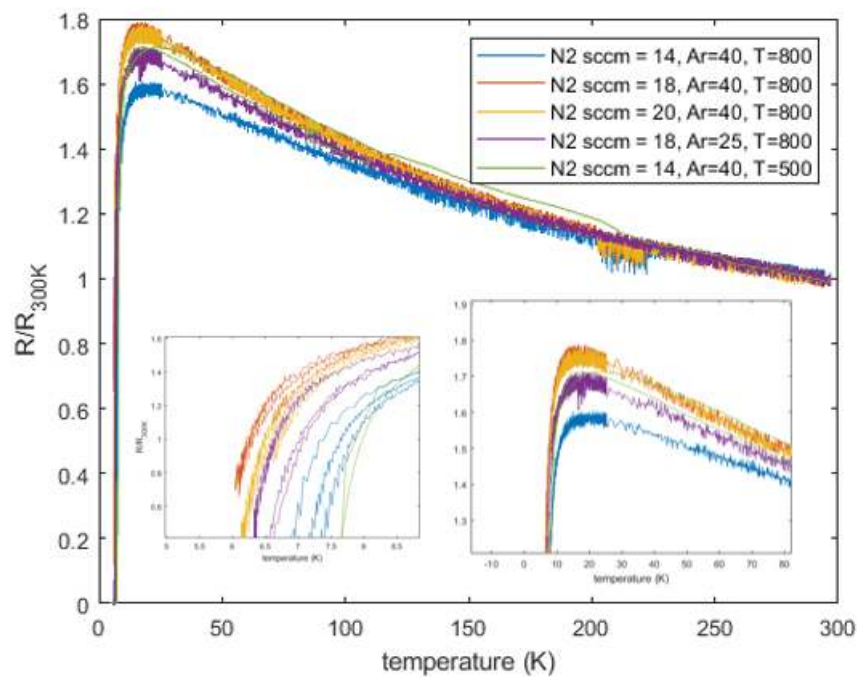
Wide wire table

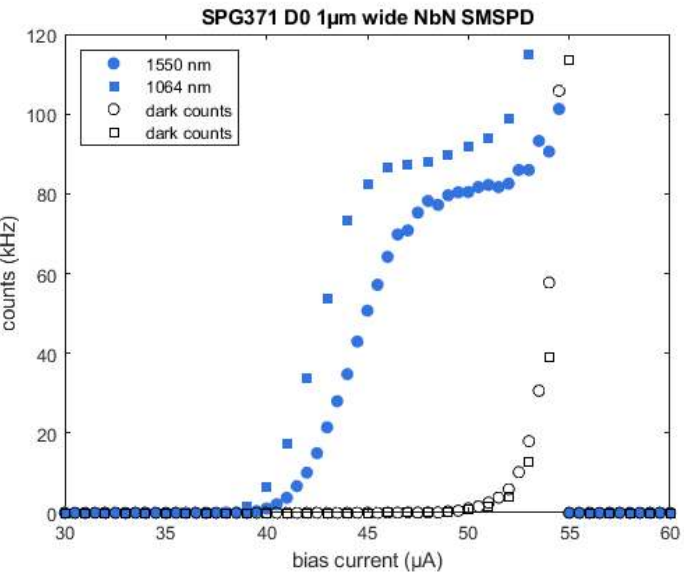
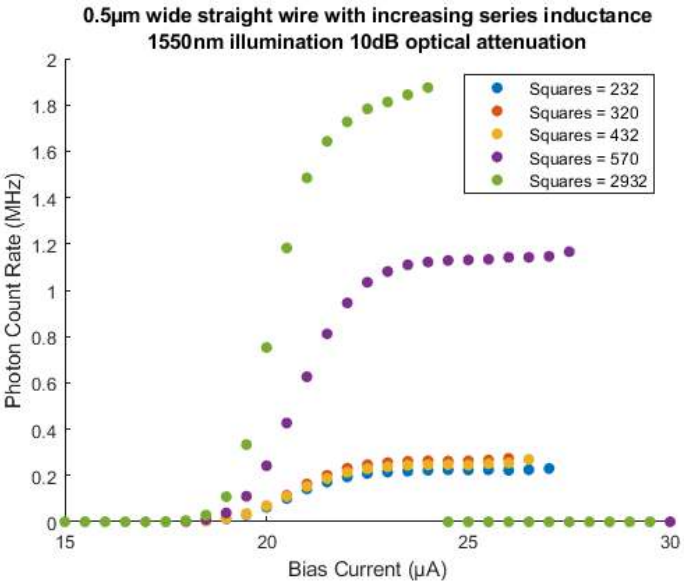
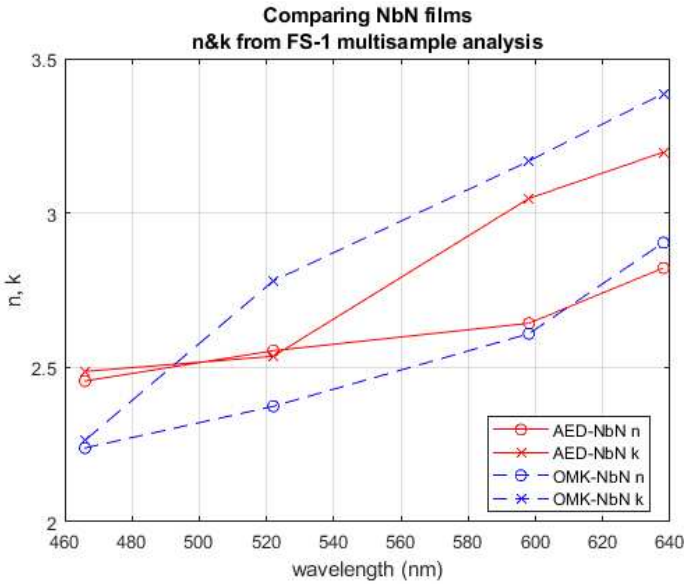
Film Characteristics													
Affiliation	Material	Substrate	Sputtering conditions	Film Thickness (nm)	Capping Layer	Capping Layer thickness	Tc (K)	Tc method	Rs (300K) (Ohms/sq)	Rs method	ρ (Ω nm)	ρ^*T_c (Ω nm K)	Jc (MA/cm ²)
MIT/Chalmers	MgB2	SiC(6H)	HPCVD	5	-	-	37	50% max	15	FPP after	75	2775	
MIT	MoSi			3	aSi	2	3		585		1755	5265	
NIST (AEL)	MoSi		compound target 75/25	2.1	aSi	2	3	50% max	1015	FPP after	2132	6395	
MIT	MoSi	Si/SiO2	Mo+Si+Ar	2	aSi	2	2.4	50% max	899	FPP after	1798	4315	
MIT	NbN		ALD	5			7.2		817		4085	29412	
MIT	NbN	SiO2	Nb+Ar+N2	4.3			4.5	50% max	982	FPP after	4236	19063	
MIT	NbN	SiO2	Nb+Ar+N2	5.5			4.14	50% max	877	FPP after	4824	19969	
MIT	NbN	SiO2	Nb+Ar+N2	4.4			7.8	50% max	550	FPP after	2420	18876	1
MIT	NbN	SiO2	Nb+Ar+N2	4.4			7.8	50% max	550	FPP after	2420	18876	1
MIT	NbN	SiO2	Nb+Ar+N2	4.4			7.8	50% max	550	FPP after	2420	18876	1
MIT	NbN	SiO2	Nb+Ar+N2	7			7.6		425		2975	22610	
Moscow	NbN		Nb+Ar+N2	7.5			9.1		514		3855	35081	
Moscow	NbN		Nb+Ar+N2	5.8			8.35		686		3980	33233	3
Moscow	NbN	Al2O3	Nb+Ar+N2	6.8			9		575		3910	35190	
Shanghai	NbN	SiO2/Ta2O5	Nb+Ar+N2+He Ion Irradia	7			6.4		1036		7252	46413	
NIST (JTC)	WSi		co-sputtering	2.1	aSi	2	2.5		1220		2562	6405	
JPL	WSi (JPL)	SiO2	Compound target 50/50	3.2	SiO2 (exSitu)	10+55	4.1		570	FPP no/cc	1824	7478	
JPL	WSi (JPL)	SiO2	Compound target 30/70	4.7	SiO2 (exSitu)		1.8		750	FPP no/cc	3525	6345	
JPL/NIST	WSi (NIST)	Si		< 3 nm	aSi / SiO2(exSitu)	2/55					#VALUE!	#VALUE!	
JPL/NIST	WSi (NIST)	Si		< 3 nm	aSi / SiO2(exSitu)	2/55					#VALUE!	#VALUE!	
JPL/NIST	WSi (NIST)	Si		< 3 nm	aSi / SiO2(exSitu)	2/55					#VALUE!	#VALUE!	
NIST/JPL	WSi (NIST)			2-3			2.62				0	0	
JPL	WSi(JPL)	SiO2	Compound target 30/70	3.6 nm	SiO2 (exSitu)		1.2		1150		#VALUE!	#VALUE!	

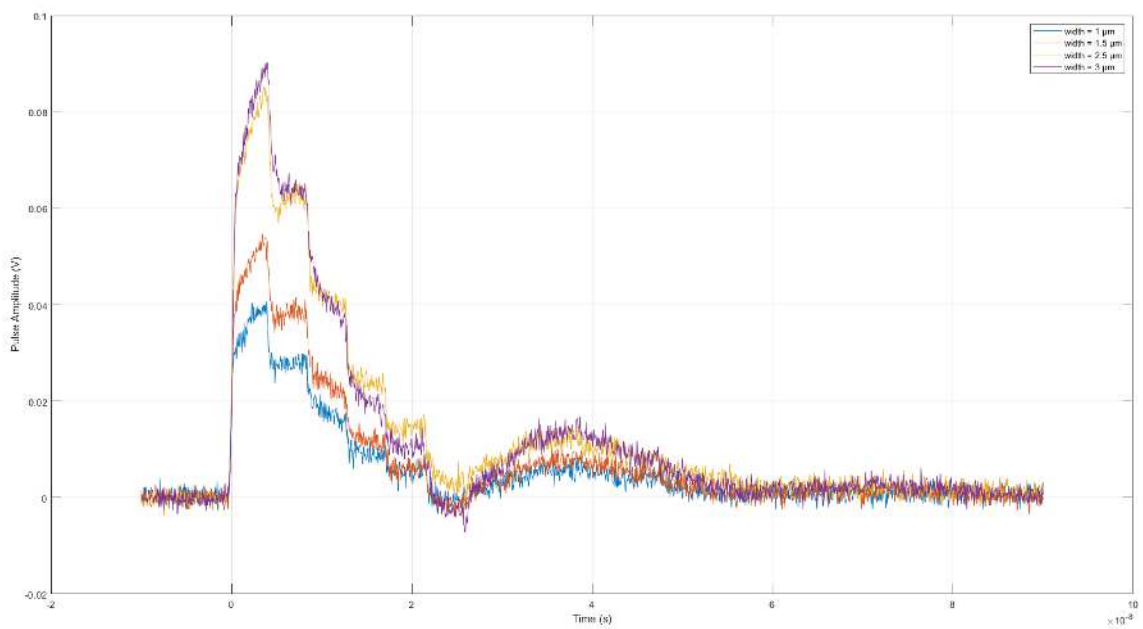
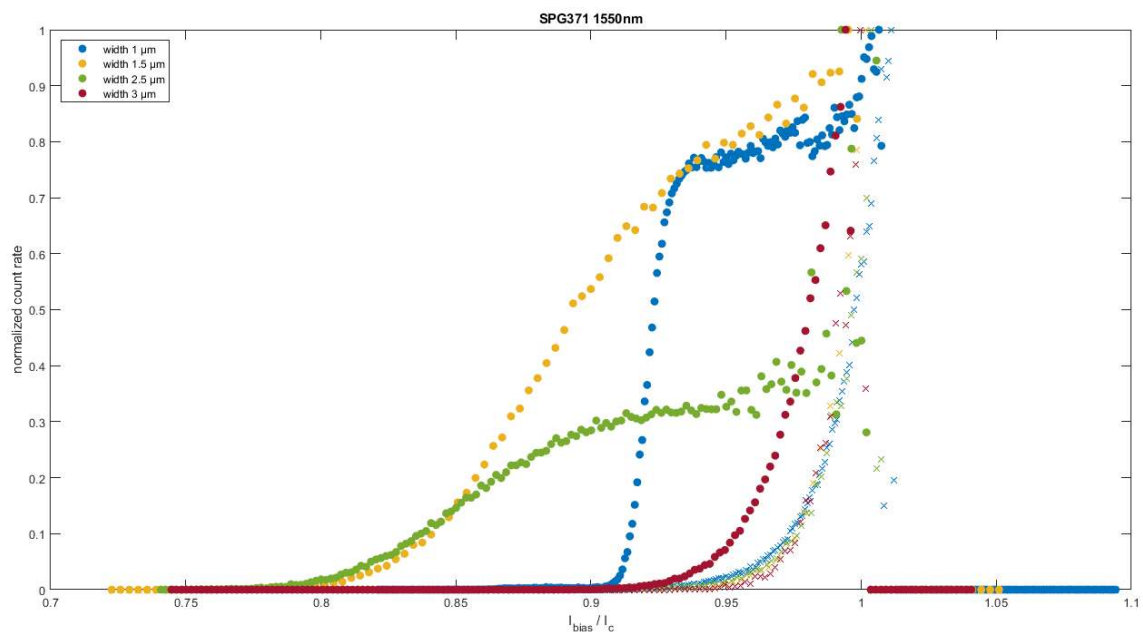
Initial NbN Tests (AED_RT)

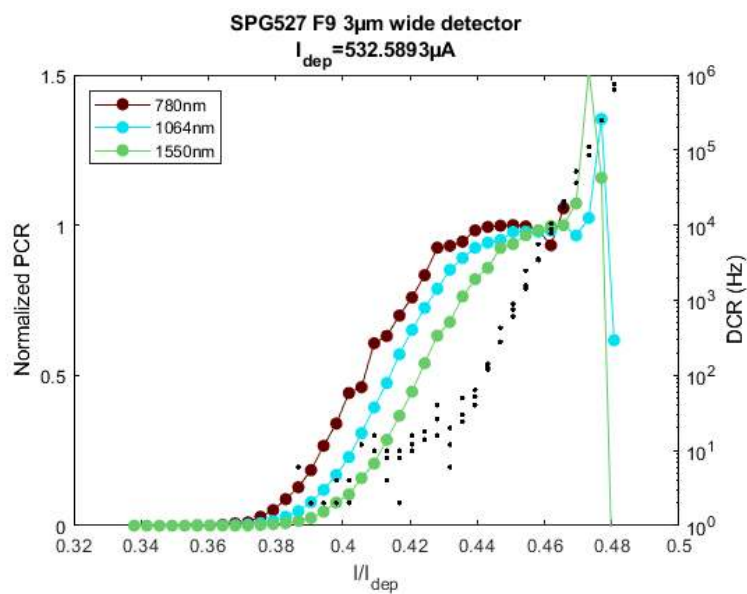
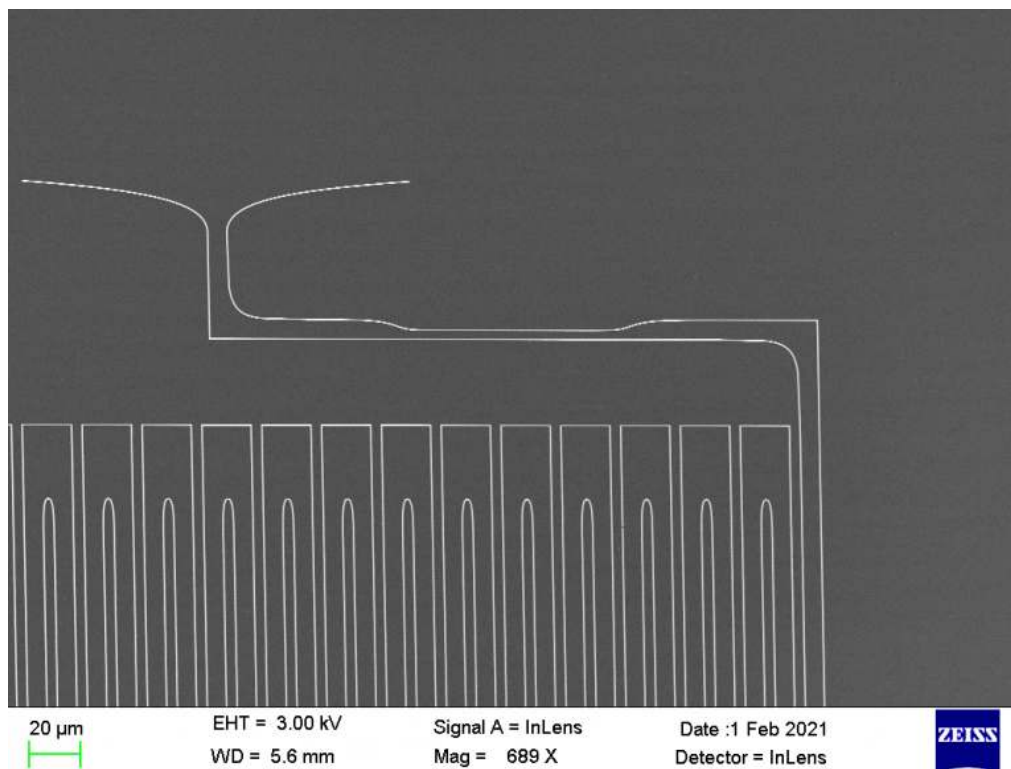


High resistivity NbN (OMK_noRFBias)



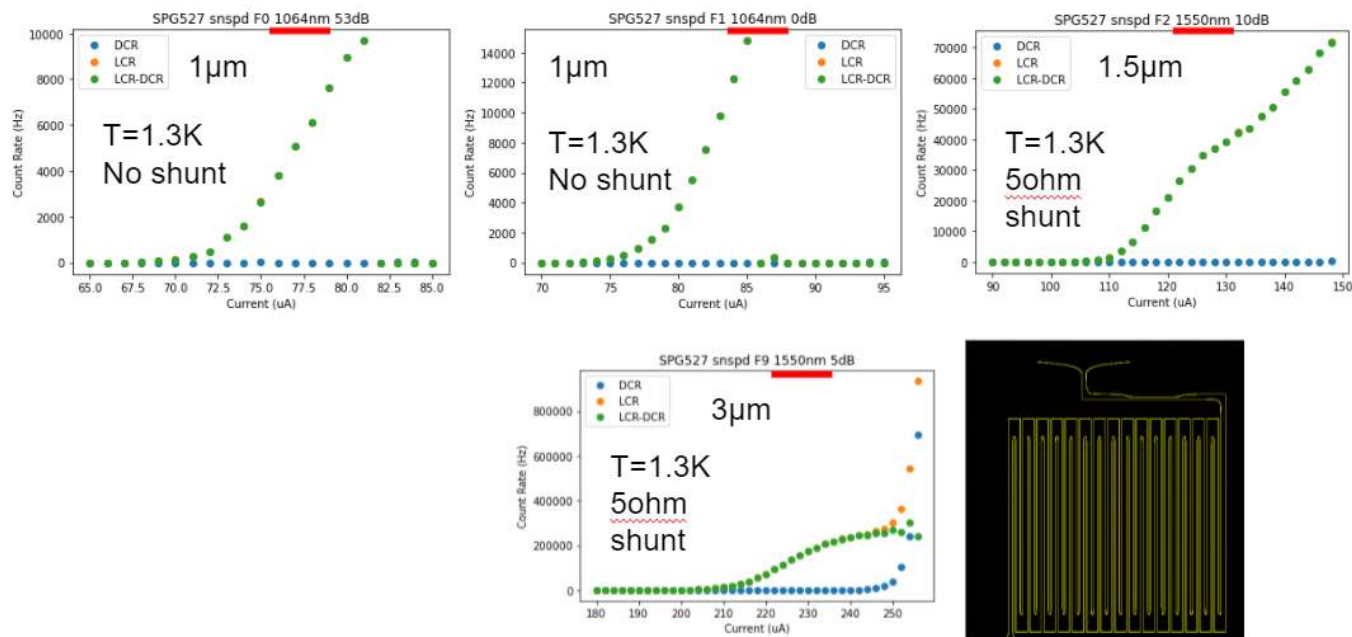




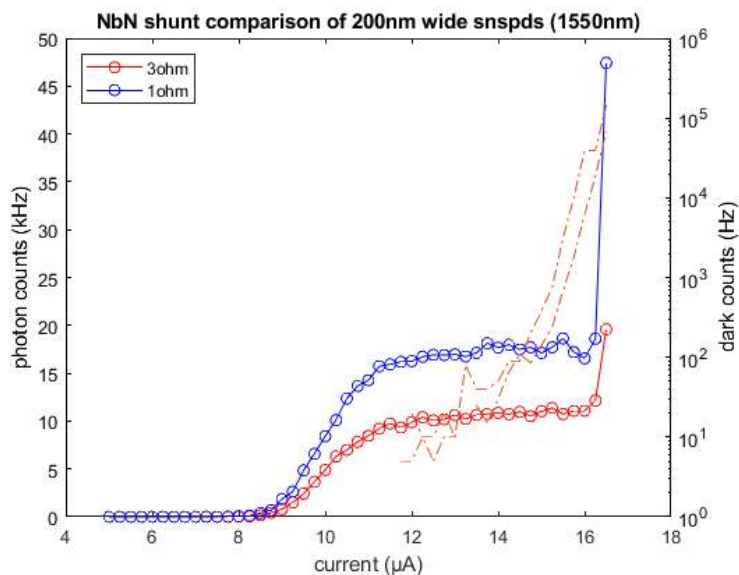


Fraction of the depairing current is still too low.

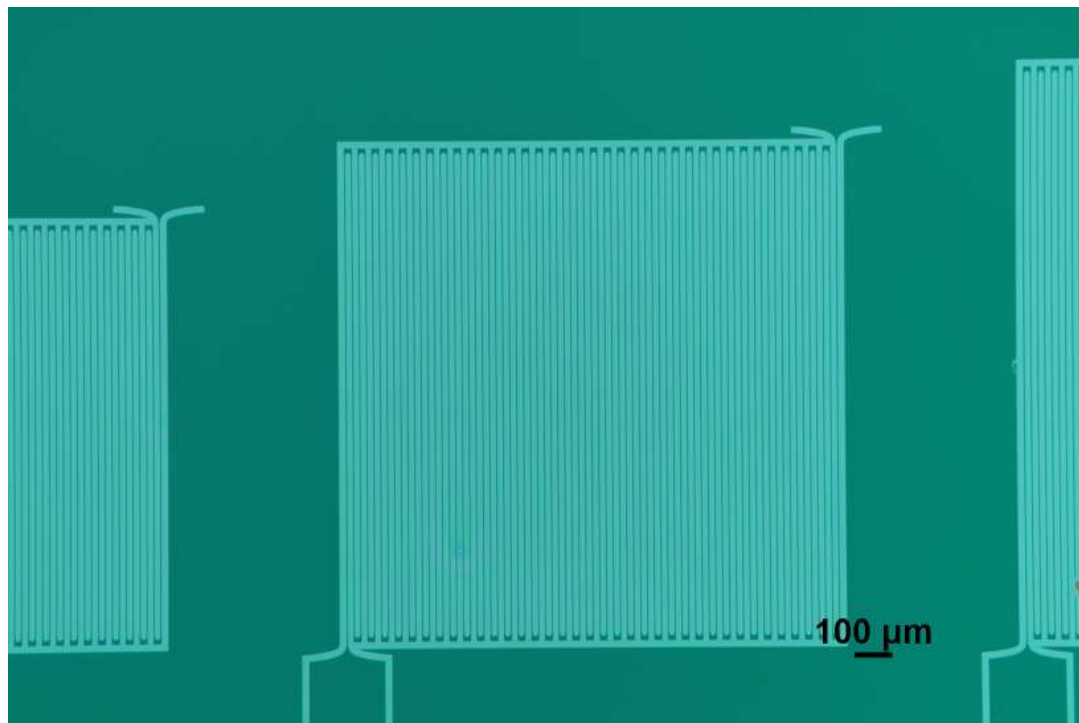
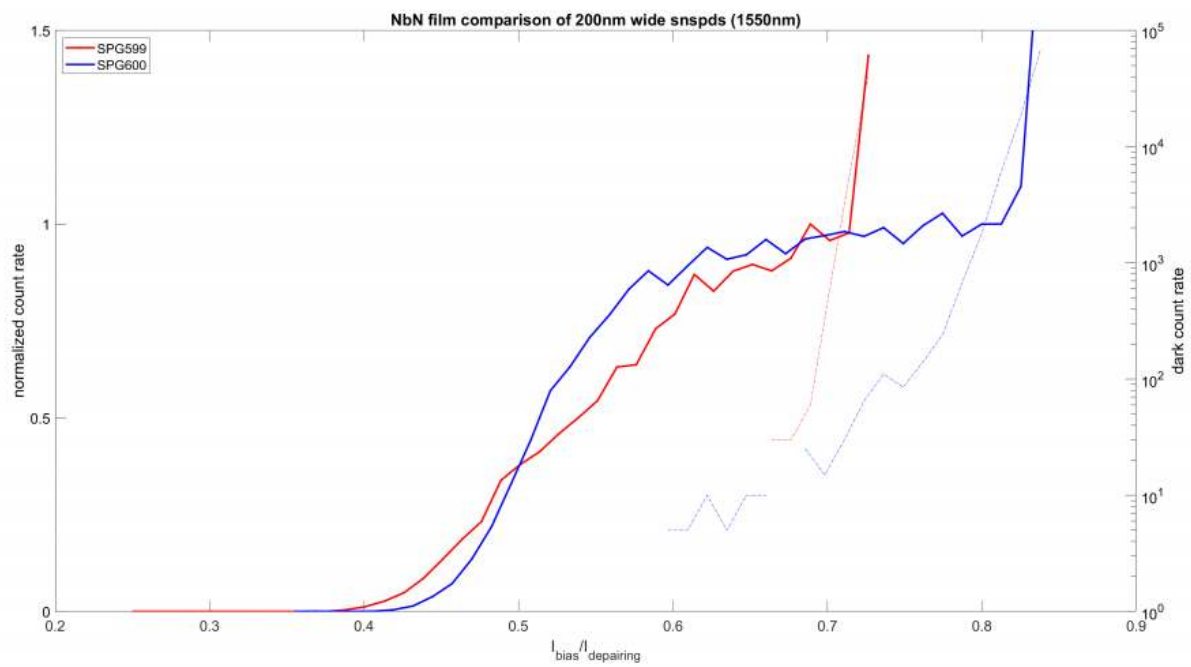
Shunting

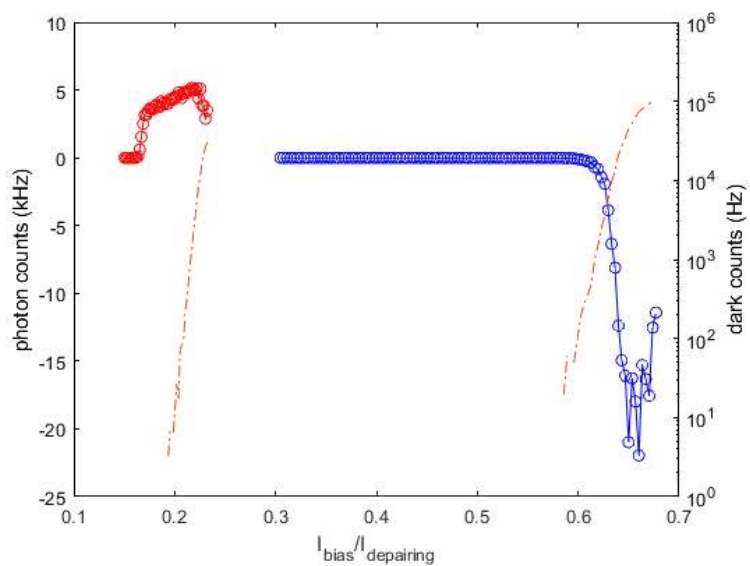
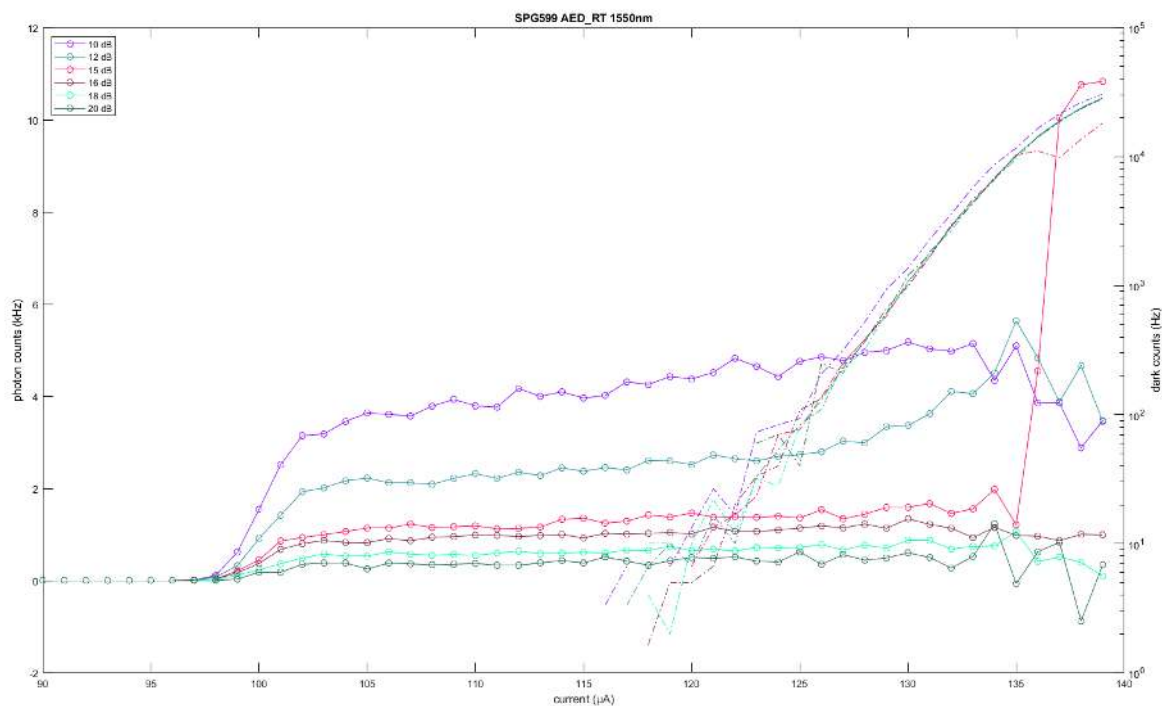


Bump in top right plot indicates counts could be coming from the inductor. Would indicate that the 7μm wide section is active



Depairing current





Probe Station Motorized Micrometer Heads

October 31, 2021

Categories: General

Specs on probe station arms. <https://www.lakeshore.com/products/product-detail/cryogenic-probe-stations/probing-configurations>

Y, Z axis can be replaced with 1" travel heads.

Thor labs options has mostly 3/8" OD Mounting. https://www.thorlabs.com/newgrouppage9.cfm?objectgroup_id=1883

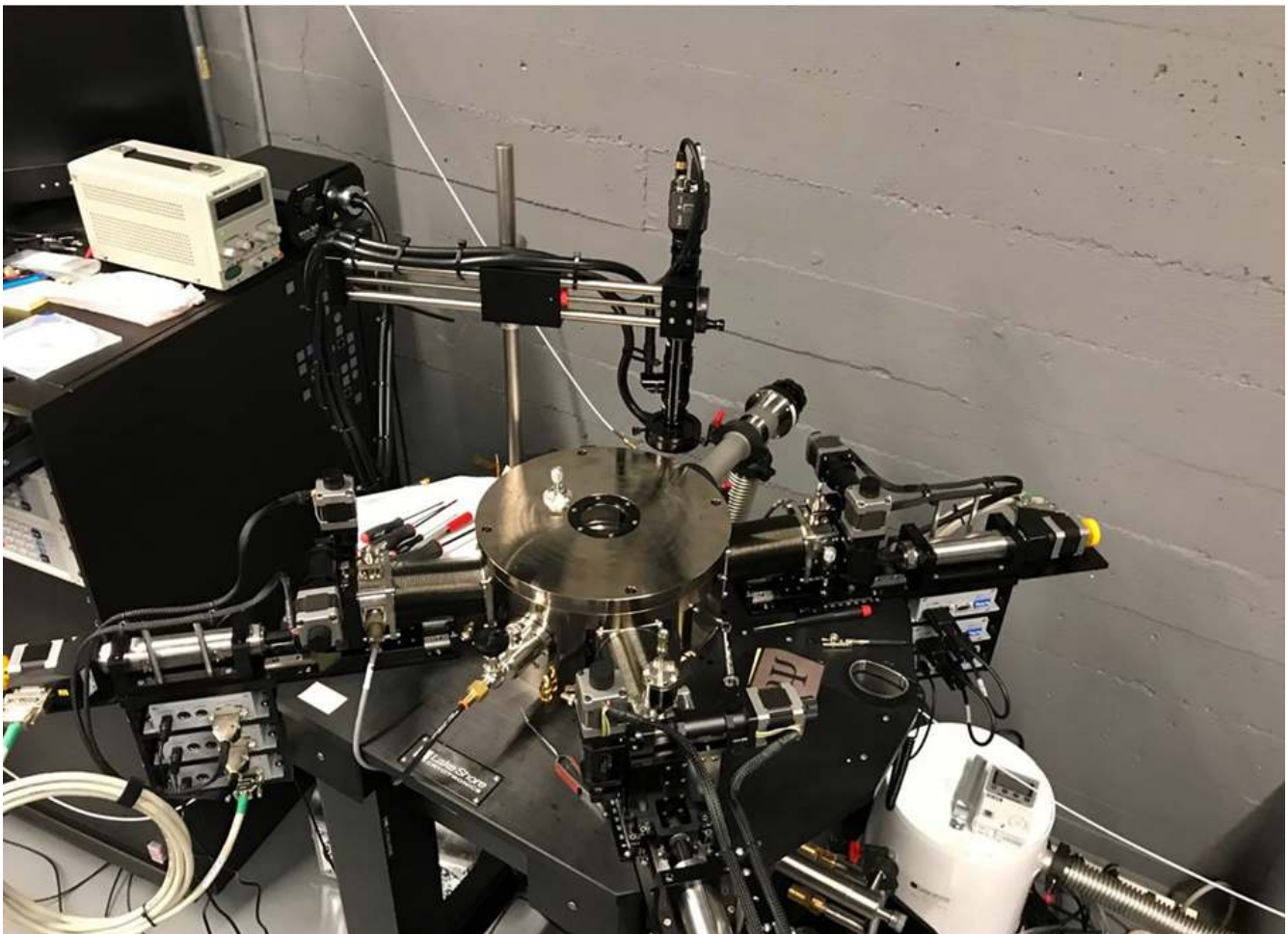
Newport also has 3/8" <https://www.newport.com/f/compact-motorized-actuators-tra-series>

all are ball tip.

NOTES FROM LAKESHORE/JANIS CALL

David Daughton (tech), Alex Tabar (sales) alex.tabar@lakeshore.com

- Ship CPX back. 1W cooler, ~4K with multiple arms. 2W is an option 3.3-3.5K. Mostly new, not much is reused. 1μm lateral, 100nm vert movement from GM cooler. pulse tube is only tip down.
- Automation. motorized stage. 1" Ø probing area. Vision tracking.
- motorized arm. slides into existing slot.



As of October 2021 they have not yet finished their design and are unwilling to sell to us.

Via process development

October 31, 2021

Categories: General

In order to create larger ntron-based circuits, specifically for the readout of SNSPD arrays, a via process is necessary to make high fidelity circuit connections on chip.

Our ability to use PECVD SiO₂ in MIT.nano is limited as our "exotic" NbN is not permitted. Evaporated SiO₂ in the NSL often has pin hole defects that cause electrical shorts.

This process will focus on using HSQ. As HSQ is spun on its thickness is well controlled and pin hold defects are not present. However curing/exposing the resist such that any further processing does not degrade the layer (unless desired) is critical. I previously used this for the RF toolbox that used HSQ as a spacer between a ground plane and a device layer had problems with long/high temp bakes (~hours, 250°C). HSQ can be cured using UV illumination and Karl suggested that O₂ plasma ash should produce plenty of heat/UV to cure the hsq. Here are the resulting thickness measurements from this analysis.

2% HSQ 5kRPM 60s

Sample	d1 (nm)	Bake Temp (°C)	Bake time (min)	d2 (nm)	Asn Power (W)	Ash Time (min)	d3 (nm)	Develope TMAH (min)	d4 (nm)
0	26.524	180	2	25.361	0	0	25.361	2	1.77
1	26.426	180	2	25.799	100	5	24.513	2	24.932
2	26.542	180	2	25.813	100	10	24.688	2	25.432
3	25.497	180	2	25.480	200	5	23.625	2	24.075
4	26.689	180	2	25.575	400	5	23.677	2	23.962

baked for 26s by accident before measuring

~zero

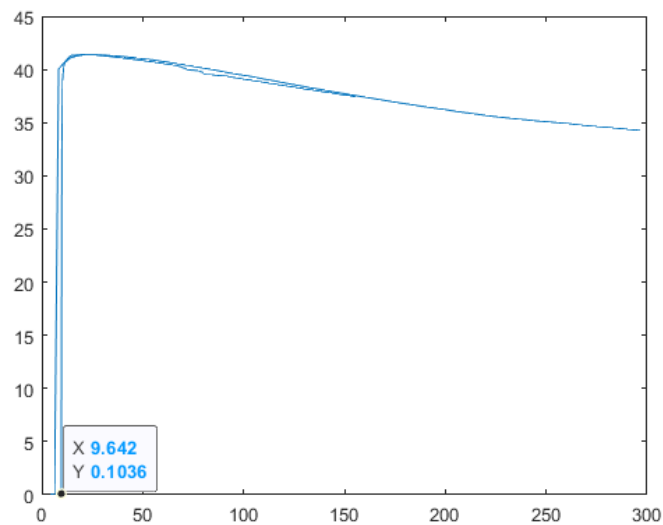
The decrease in thickness could be real. Or could be a change in the HSQ refractive index after curing. Or a combination of both.

I was really thinking that the TMAH would remove the HSQ so I was very aggressive with the O₂ plasma ash, but even the lowest settings seemed to work. I repeated the process for 6% HSQ, there was some erosion of the HSQ for 5 minutes ash (which could be due to: chips on the edge of the hand-diced die, or detritus, that allowed TMAH to get under certain sections) but 6 minutes worked well. I would think that longer bakes/ash would be needed as there is more material.

6% HSQ 3kRPM 60s

Sample	d1	Bake Temp	Bake time	d2	Asn Power	Ash Time	d3	Develope TMAH	d4
0	101.31	180	2	98.317	100	5	98.737	2	101.07
1	103.02	180	2	100.37	100	6	97.301	2	98.184

It is important to check that this will not degraded the NbN film underneath. I tested the process with an older calibration chip SPG401 which had a T_c of 9.1K. After Spinning 6% HSQ at 3kRPM, baking at 180°C for 2 min and plasma O₂ ash at 100W for 6 minutes the T_c curve is shown below. It is slightly higher... probably just measurement error as the ramp speed.



The next step would be to pattern the HSQ, making via holes to the metal layer underneath. As a first pass I will borrow the process specifications for Voltan fab process from Jeff Shainline.

2.5 Layer m2 (Nb ground plane)

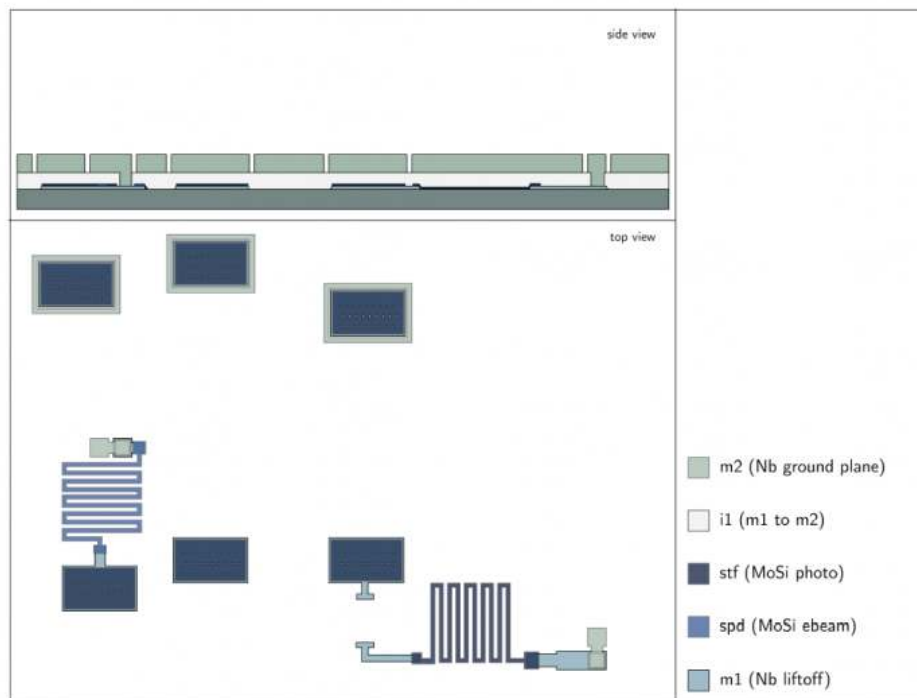


Figure 5: Deposit m2 (Nb ground plane) and etch features and flux moats.

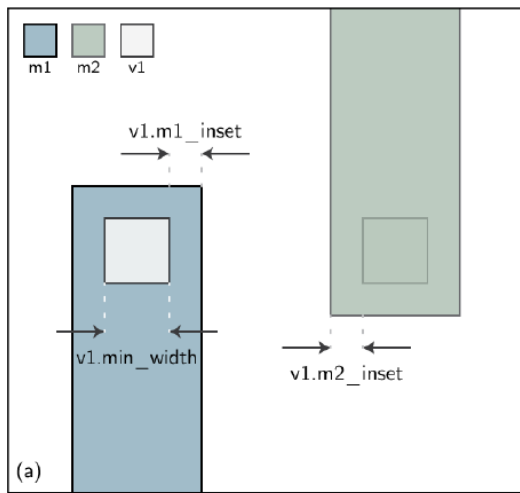
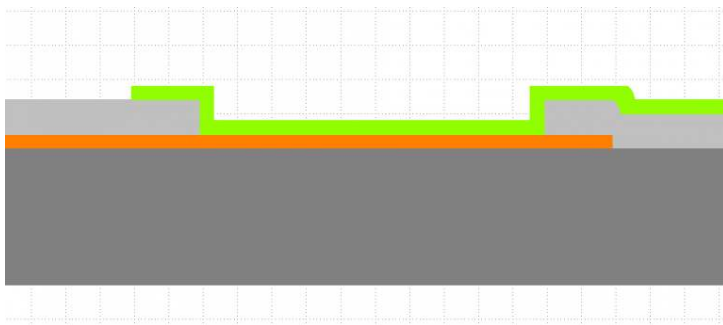
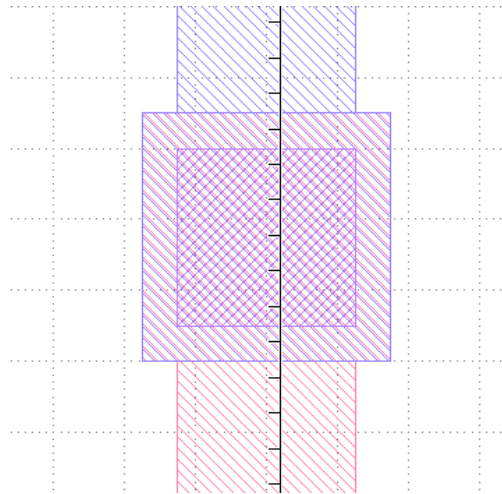


Table 4: Design rules for via layers

Layer	min_width	min_gap	inset
v1	1 μm	4 μm	m1_inset = 1 μm m2_inset = 1 μm
v2	1 μm	4 μm	m2_inset = 2 μm jj1_inset = 2 μm
v3	1 μm	4 μm	jj1_inset = 1 μm jj2_inset = 300 nm
v1	10 μm	40 μm	r2_inset = 5 μm

For first pass tests I will try to write 2 μm -5 μm features using the uPG.

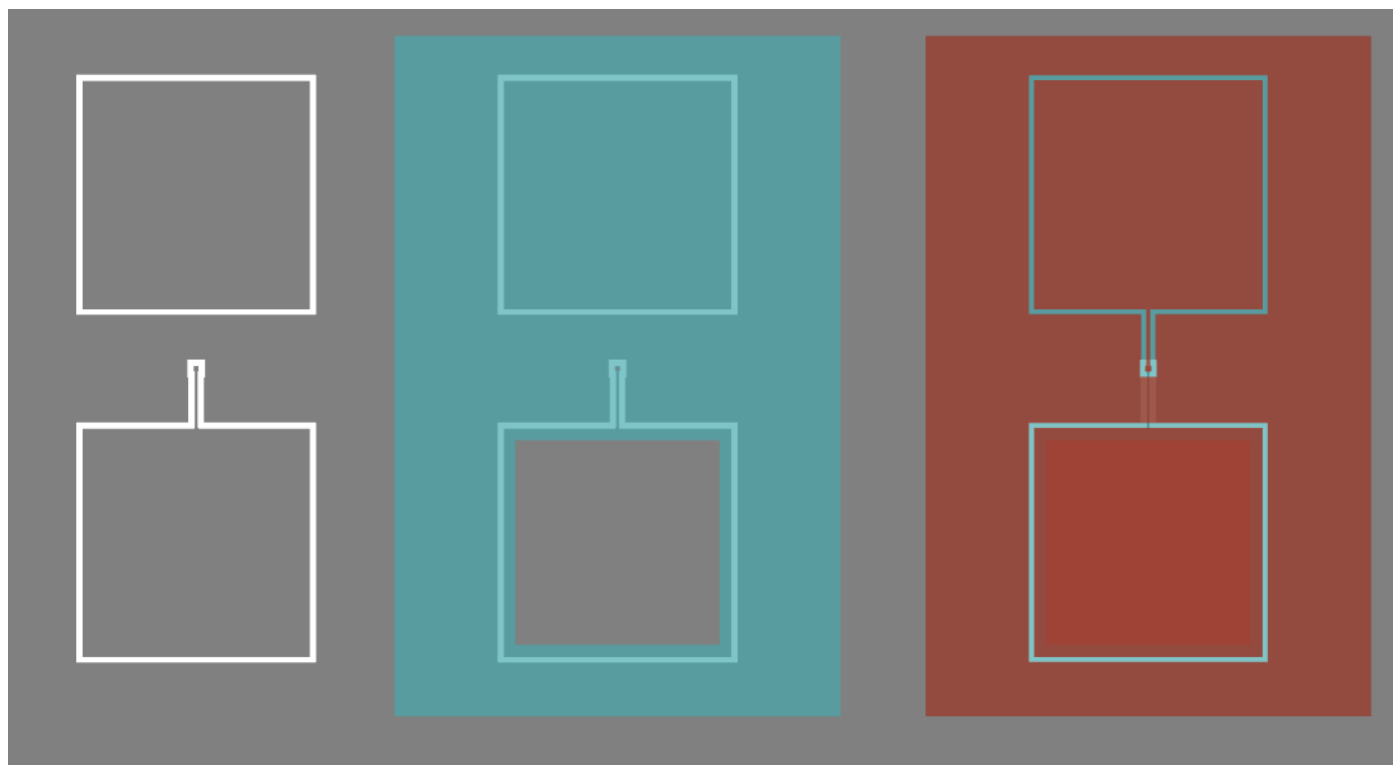
Using phidl and KLayout(with XSection)



Quick cross section. Mainly to test script. I acknowledge that the colors are ugly and layers are not to scale.

Process outline can be performed with either S1813 or ZEP

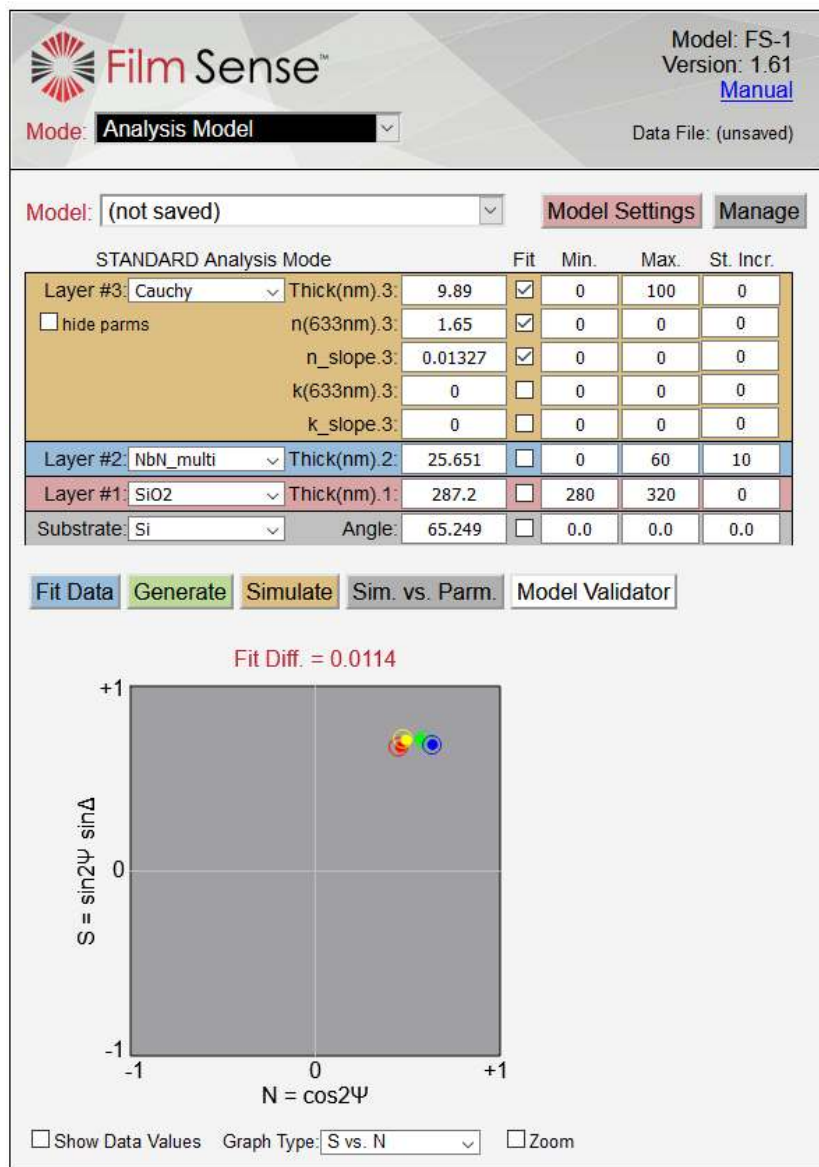
1. Deposit NbN
2. Pattern NbN positive tone
3. spin HSQ and ash
4. Pattern positive tone as etch mask, etch into HSQ
5. deposit top metal, sputtered NbN
6. Pattern top NbN positive tone.



HSQ mask: S1813 @4.5kRPM ($\sim 1.2\mu\text{m}$)

HSQ etch rate.

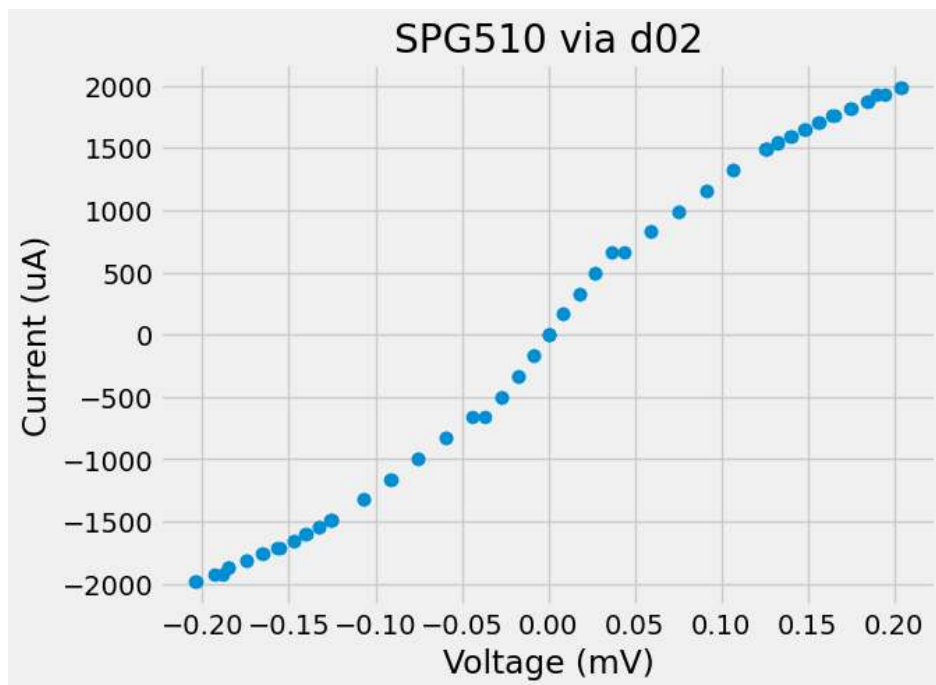
Etched 100nm HSQ for 7 minutes and 9.89nm of HSQ were remaining.



Etched for another 2 minutes because I wanted to be sure all the HSQ was gone and a thinner film would be fine. The extra 2 minutes etched into SPG401 (25nm) 7nm. Leaving 18nm shown below. So 8 minutes sounds ideal.

Fit_Diff	0.0130
SiO2	289.76
NbN	18.103
Nb2O5	0.85331

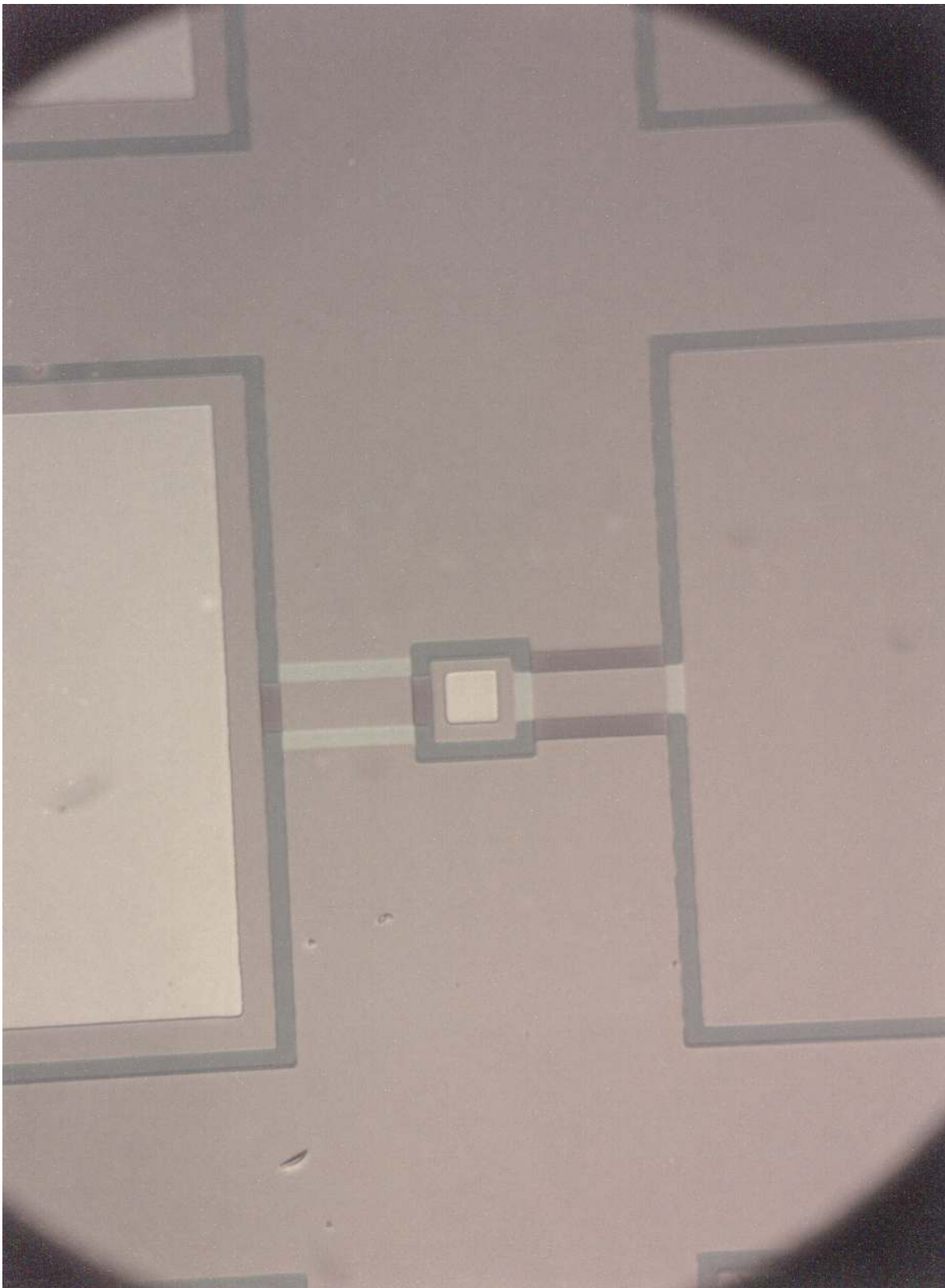
First result



This is a IV curve of one of the vias. It is not exactly clear but there is no switching in this image. I could not source more than 2mA from the SRS and did not switching to a different current source. But it is expected to have a very high I_c , $\sim 20\mu\text{m}$ wide and 15nm thick. Resistance starts at $\sim 50\Omega$ and peaks at $\sim 100\Omega$.

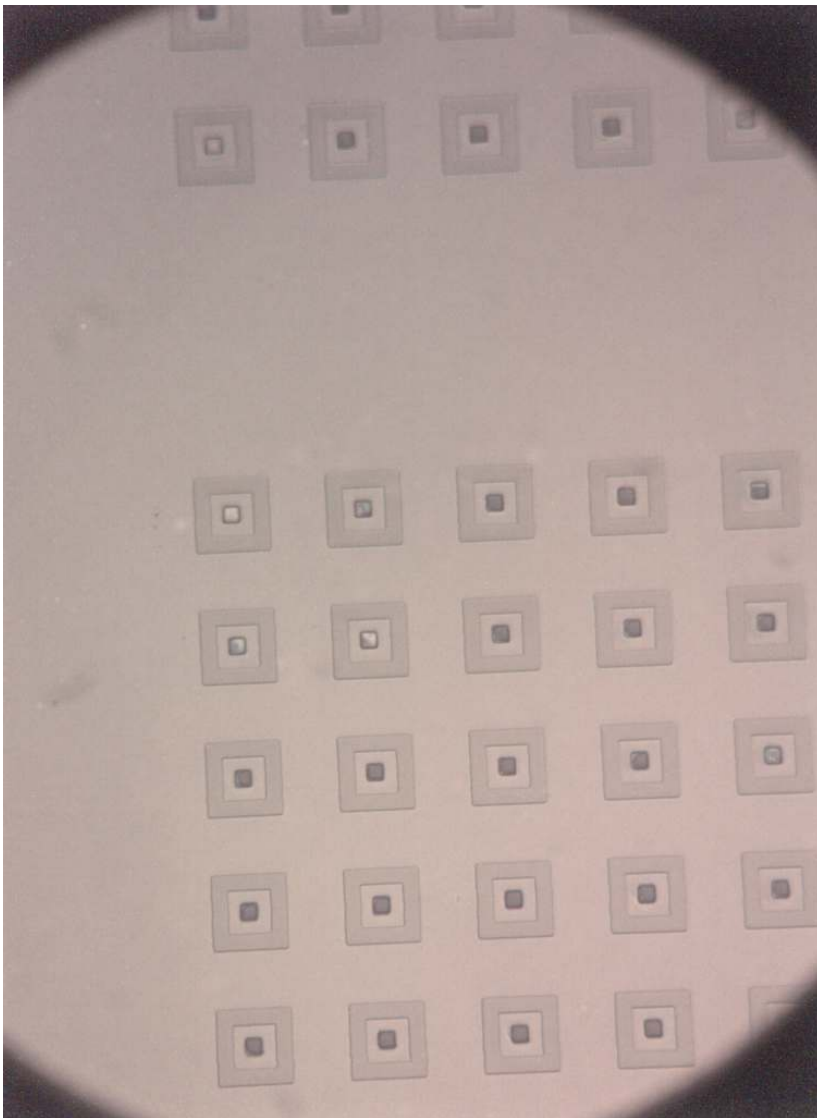
Would see $k\Omega$ for switching.

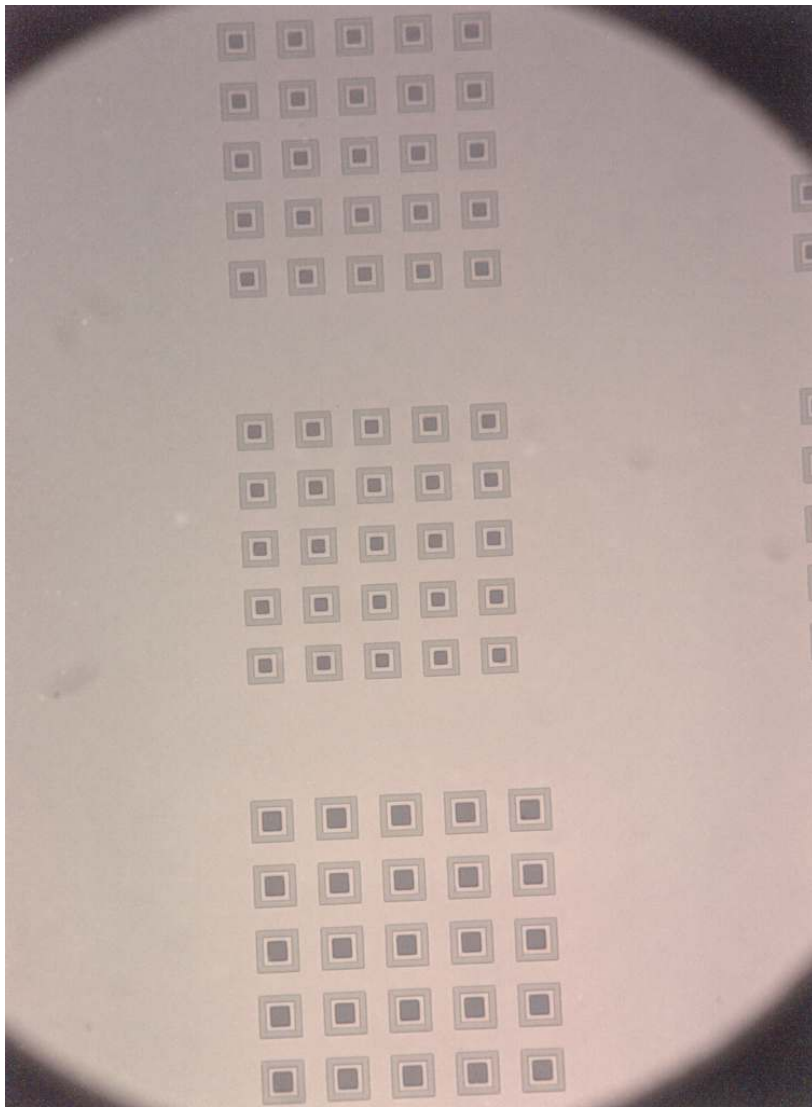
Fabrication



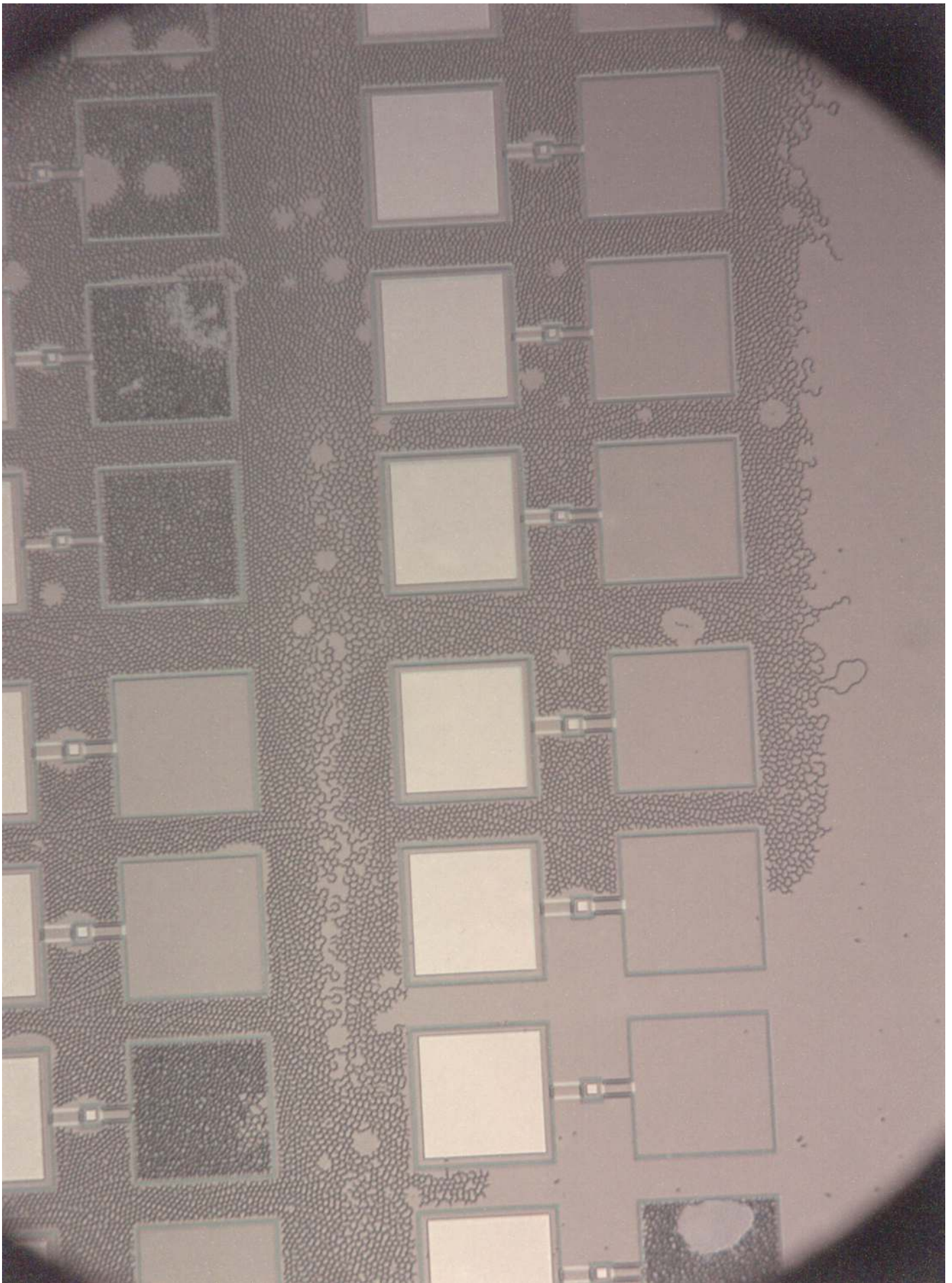
There were two issues with this initial process test.

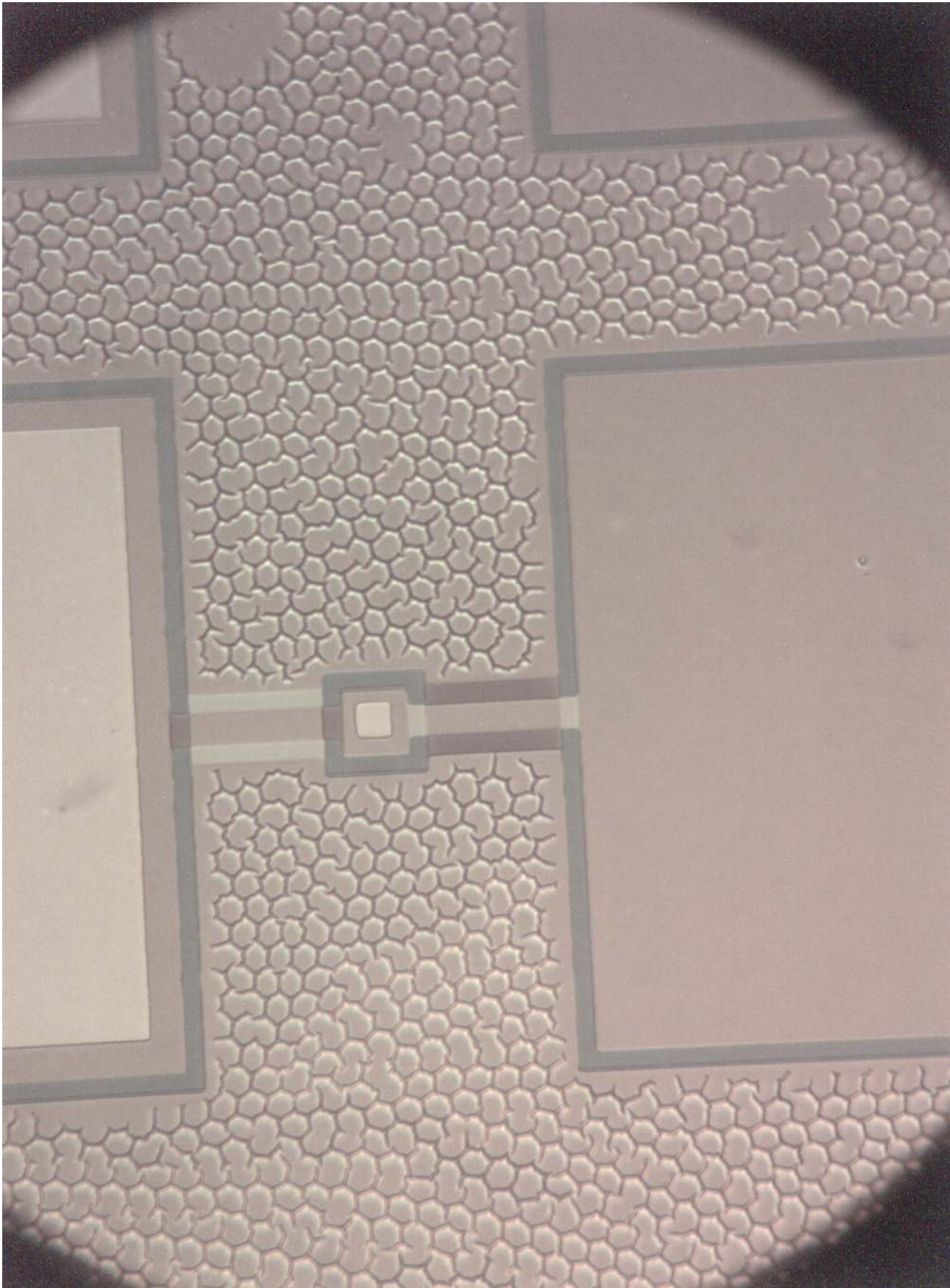
1) Small feature sizes had a wetting problem, where the developer (CD-26) did not fully enter the small squares. The image below is with squares 5 μ m wide. I tried with small features first and had worse results.

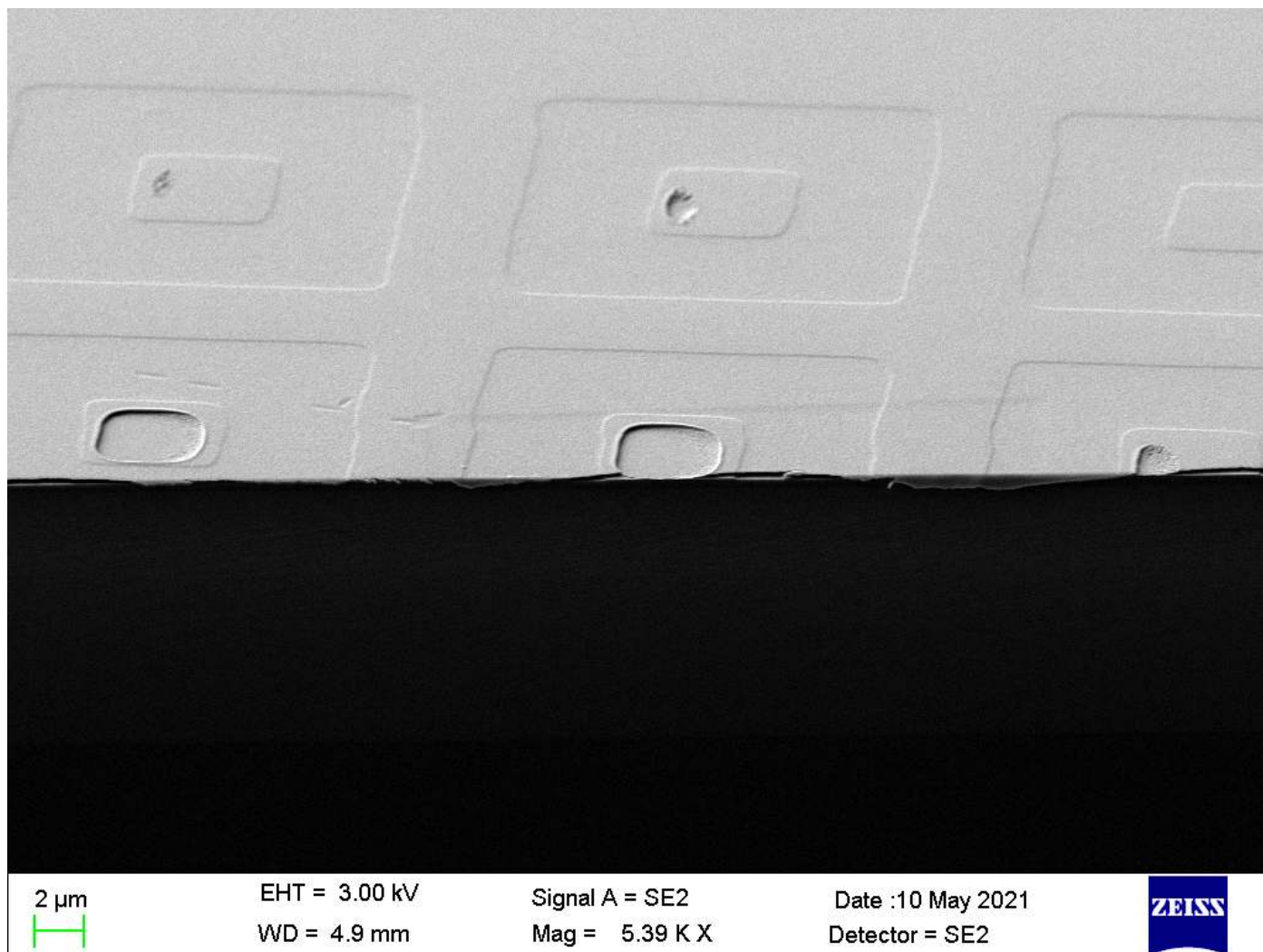


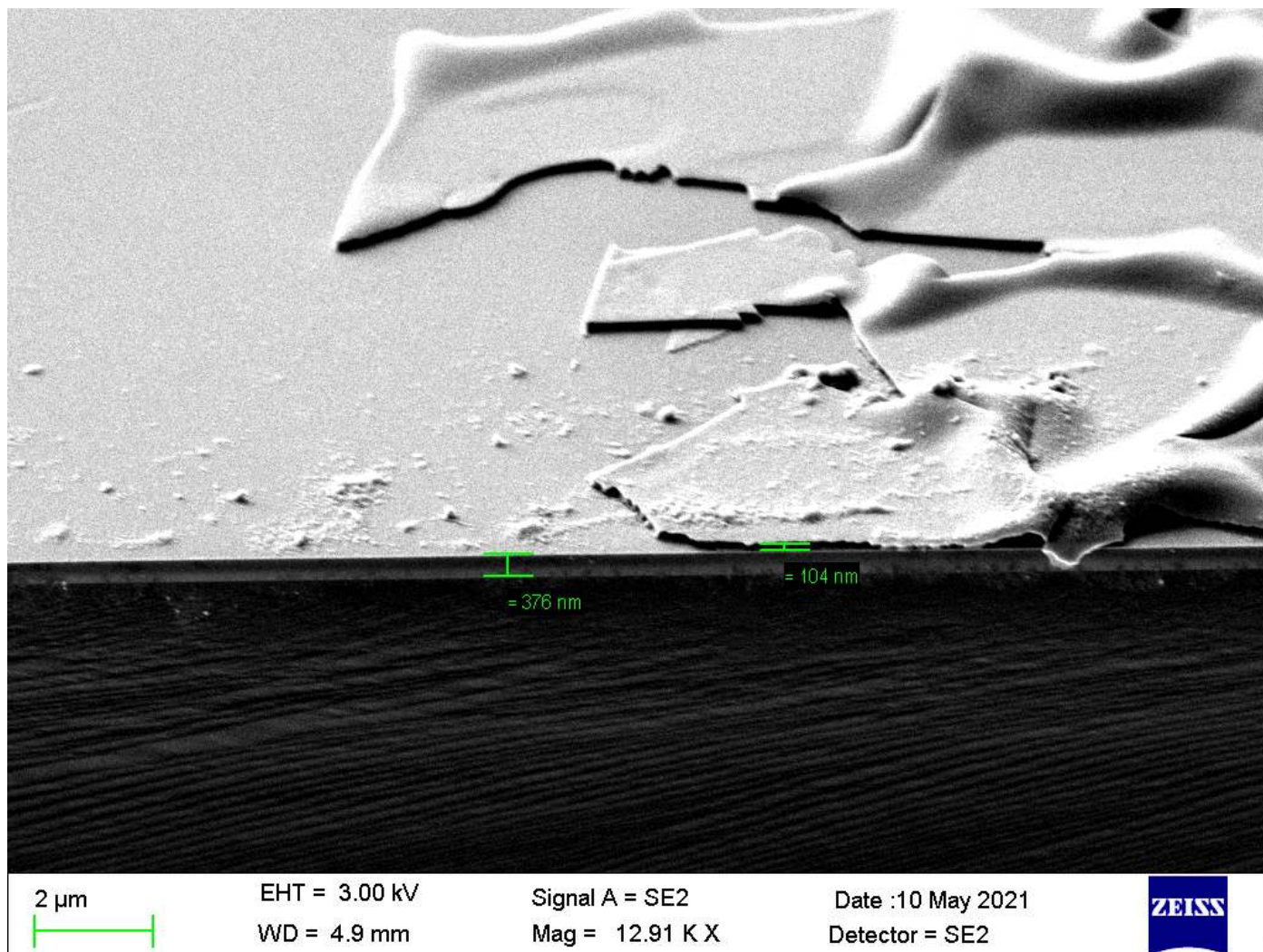


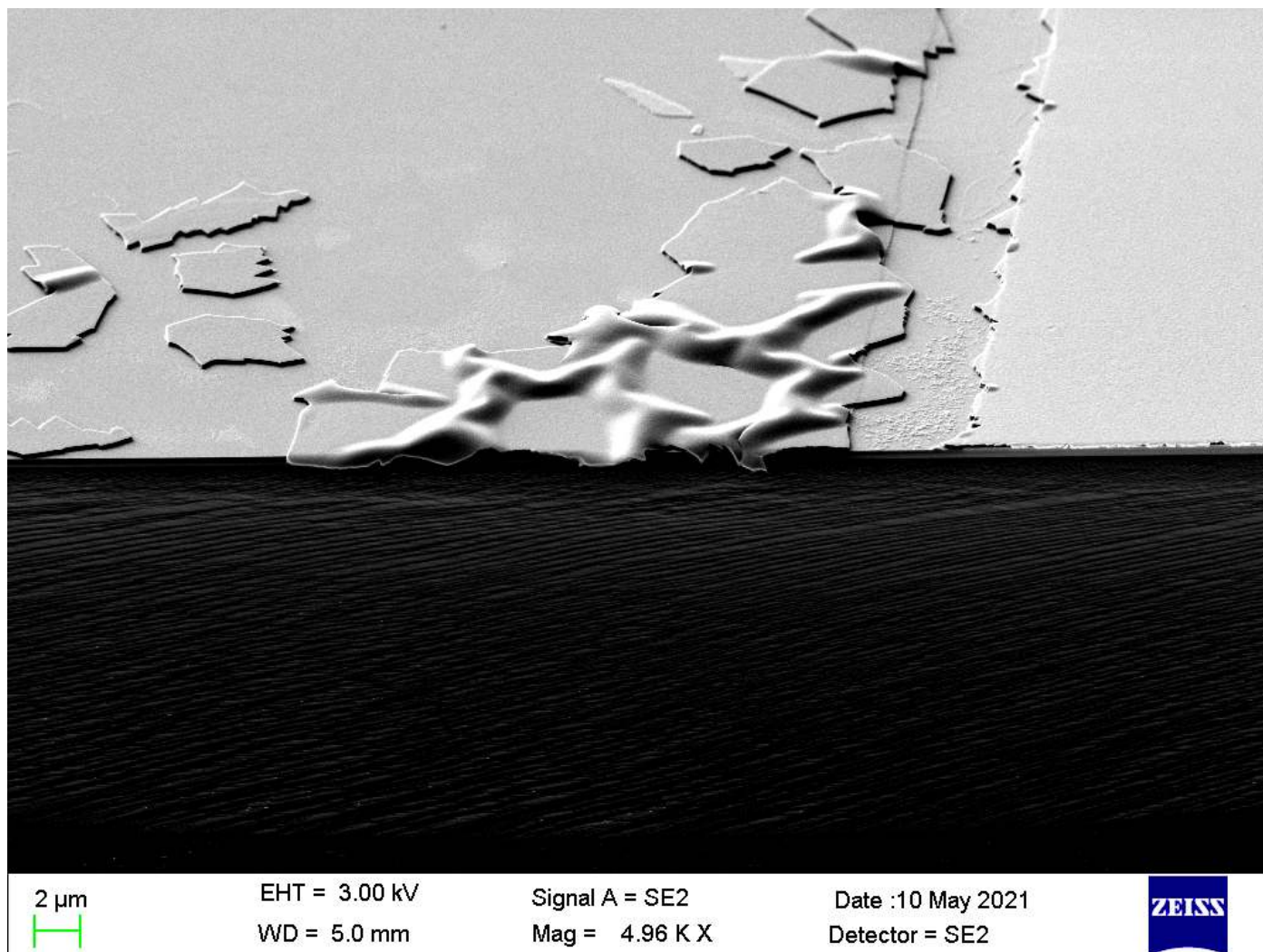
2) There was also an adhesion problem with the HSQ on the first metal layer.

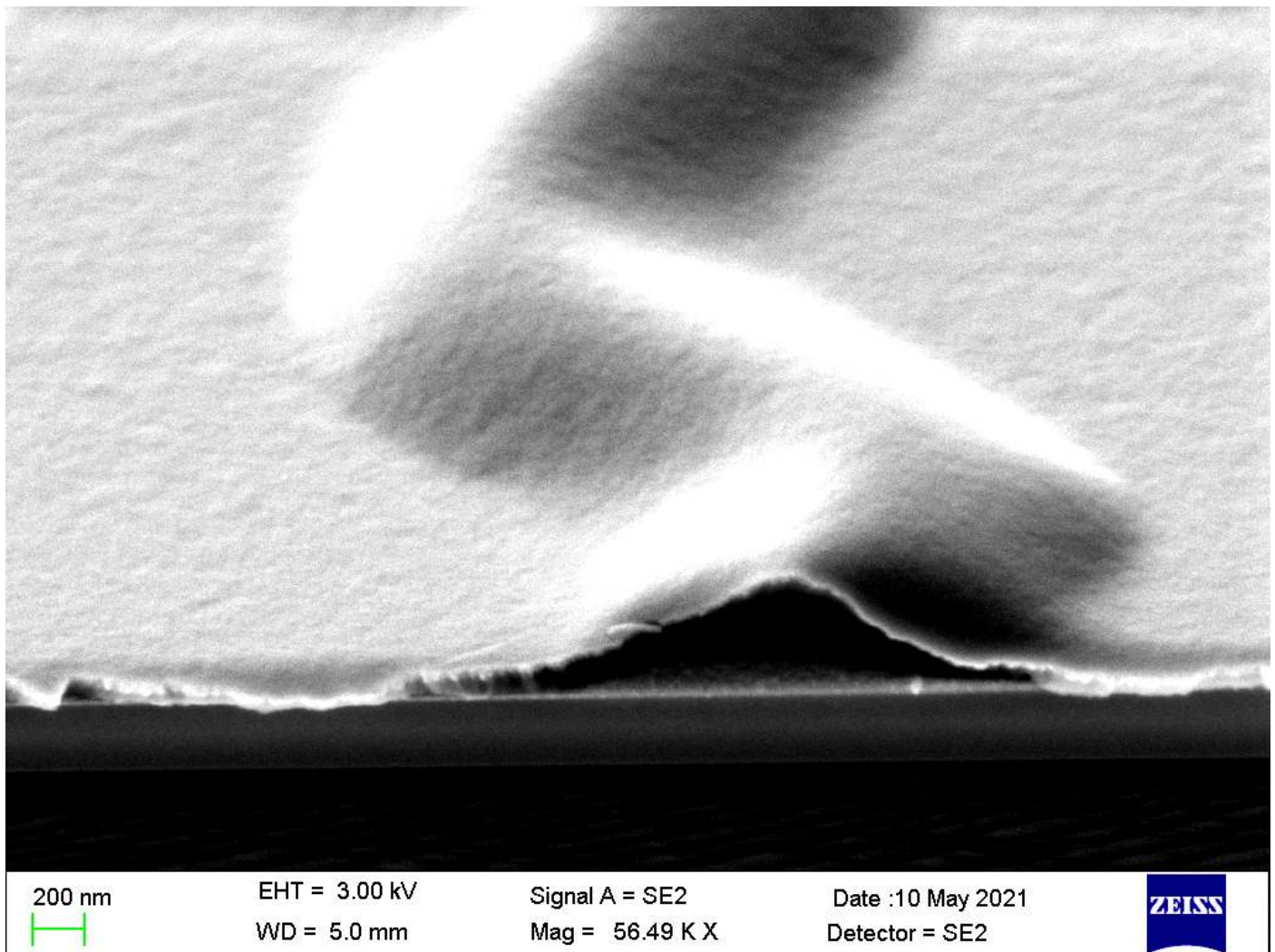






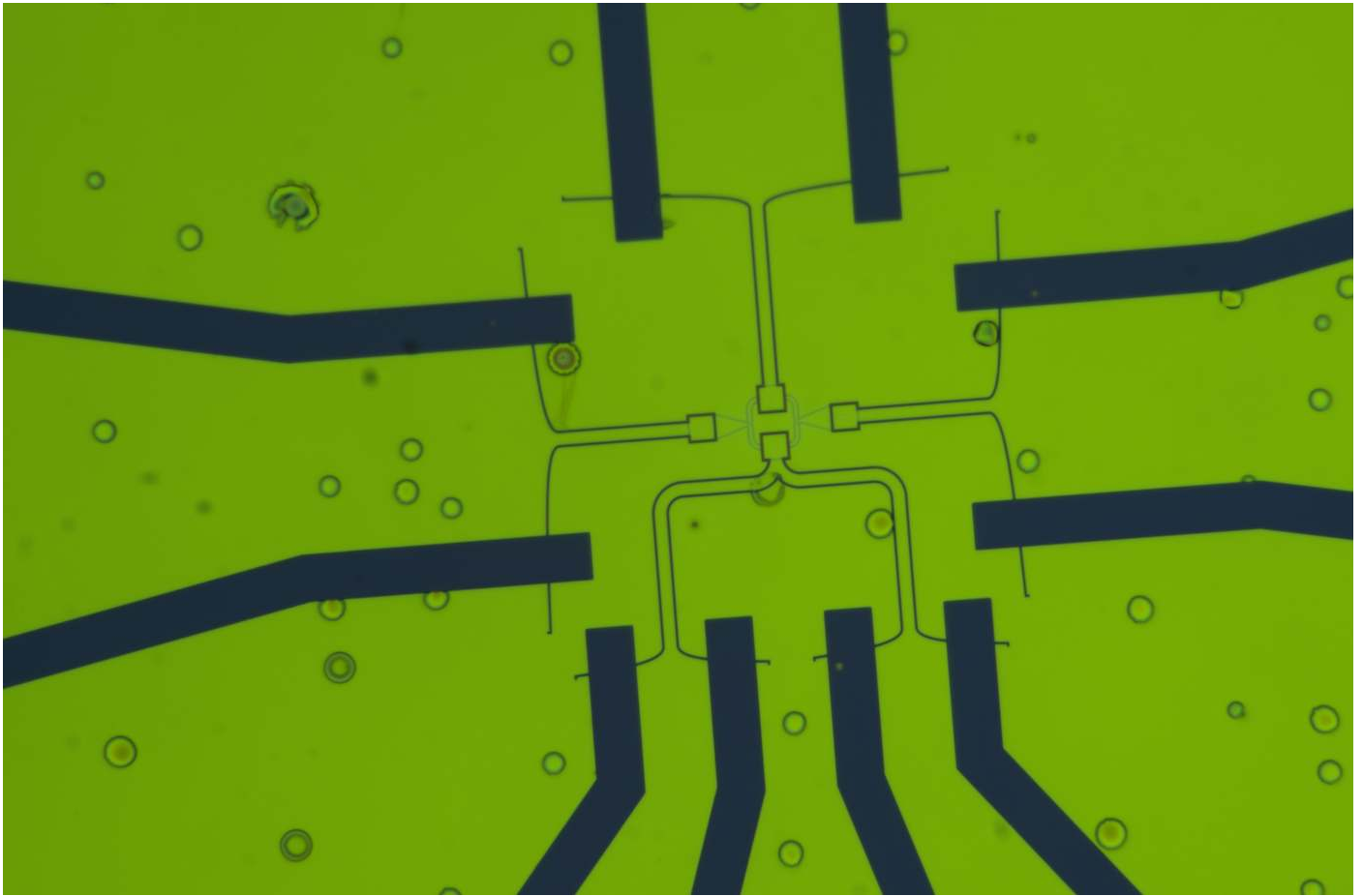


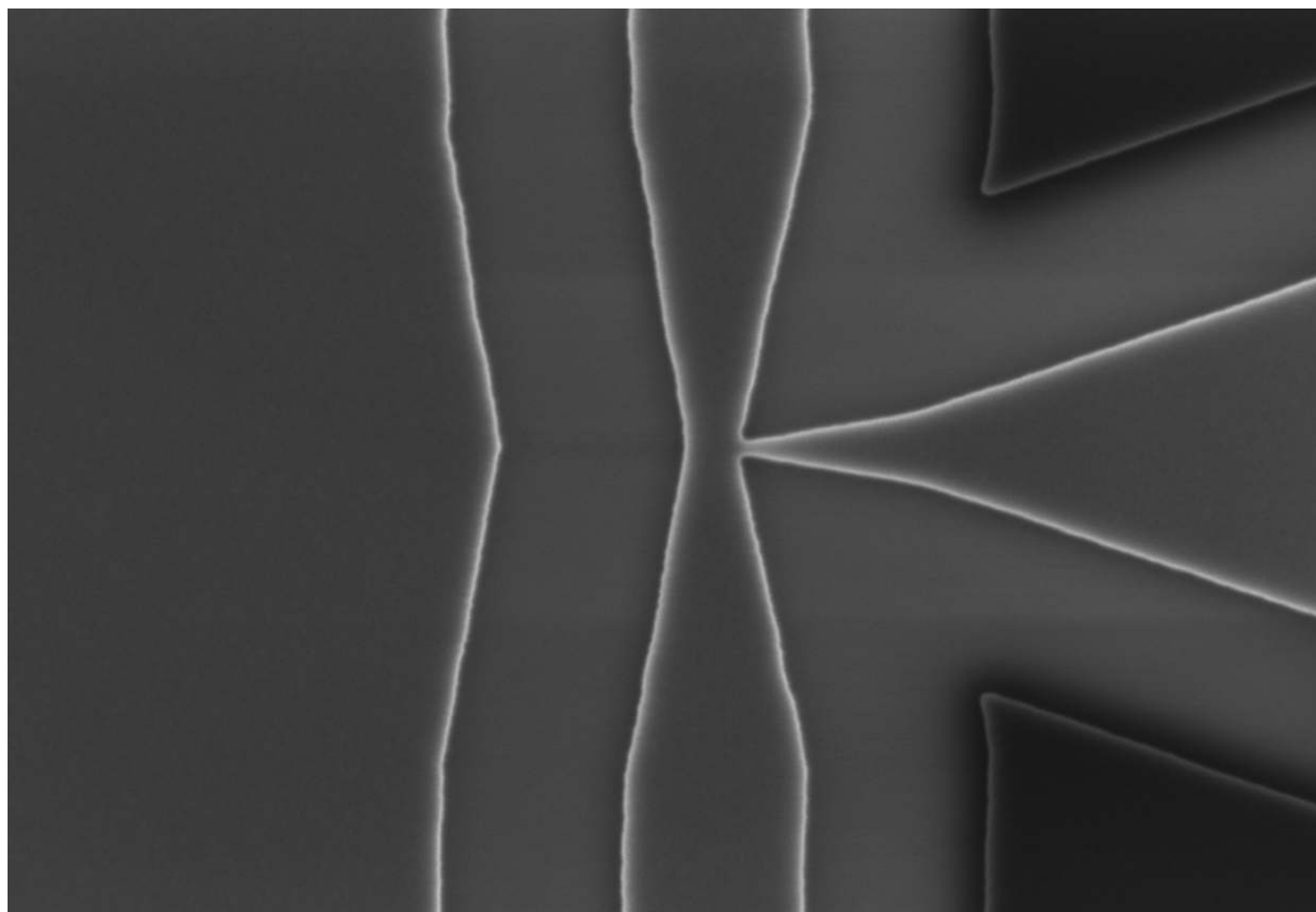




Assuming the problem is due to adhesion of HSQ to the first metal layer we might be able to reduce the compressive stress and improve adhesion by using a thinner layer.

I repeated the process using 2% HSQ and EBL ZEP530 for patterning. The results below show the same bubble issue I observed during the trilayer process development. I am thinking that the bubbles and the hexagonal cracks stem from the same issue: **There is still MIBK left in the HSQ.** I tried to test this thought by spinning HSQ, plasma ashing, and then spinning zep. But there were not any bubbles. This matches with the ability to pattern the 2% HSQ using ZEP without having any bubbles. So the issue likely lies with the second metal layer trapping the evaporating MIBK and forcing it to collect into spots/bubbles/hexagons. With resist on top of HSQ the MIBK is able to escape through the resist.





200 nm


EHT = 3.00 kV
WD = 5.0 mm

Signal A = InLens
Mag = 77.17 K X

Date :25 May 2021
Detector = InLens



Appendix

[pdk_votan.pdf](#)

ntron snspsd chip notes

October 31, 2021

Categories: nTron

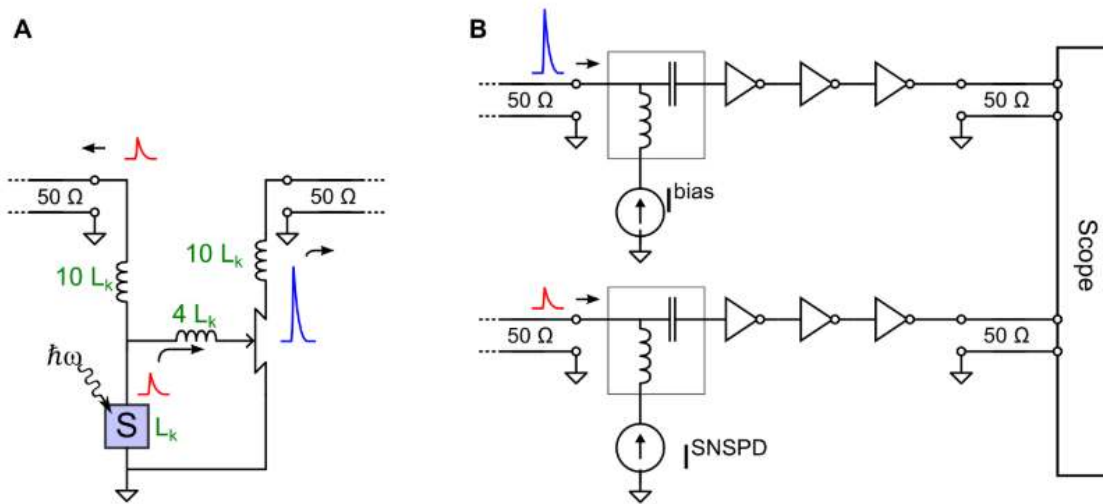
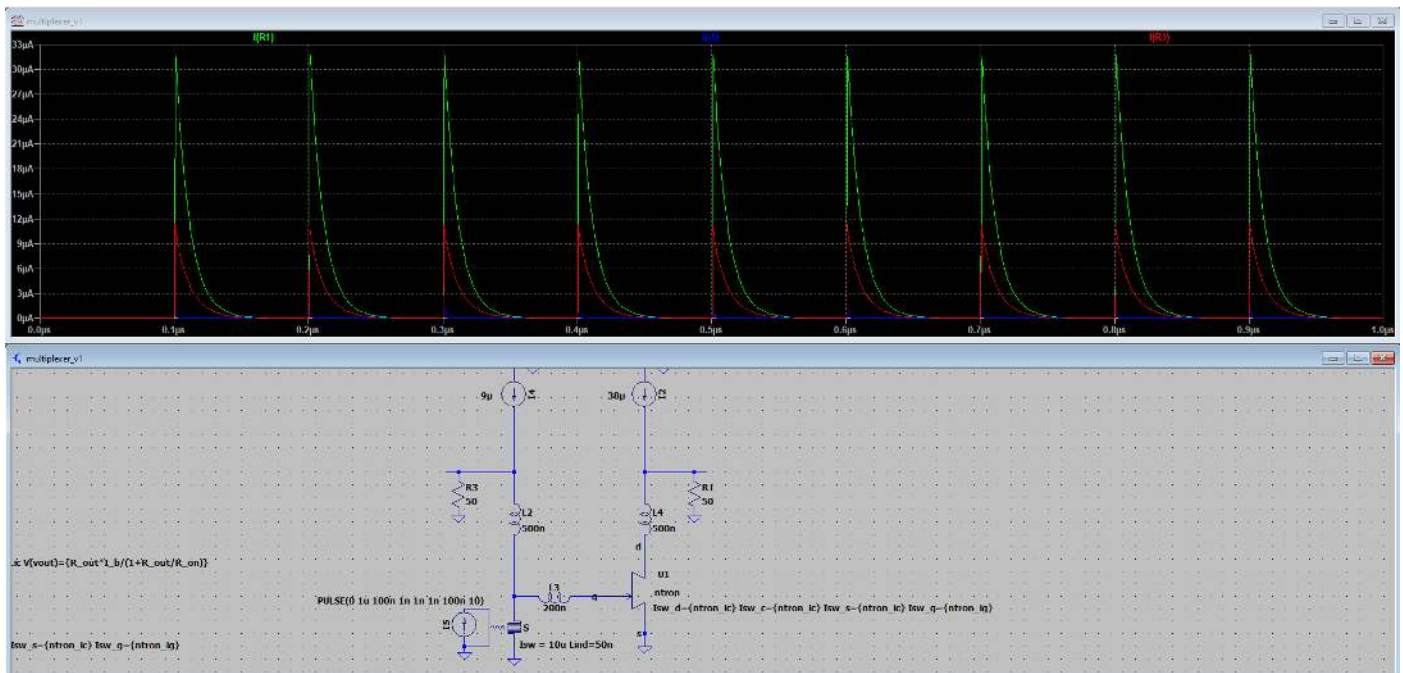
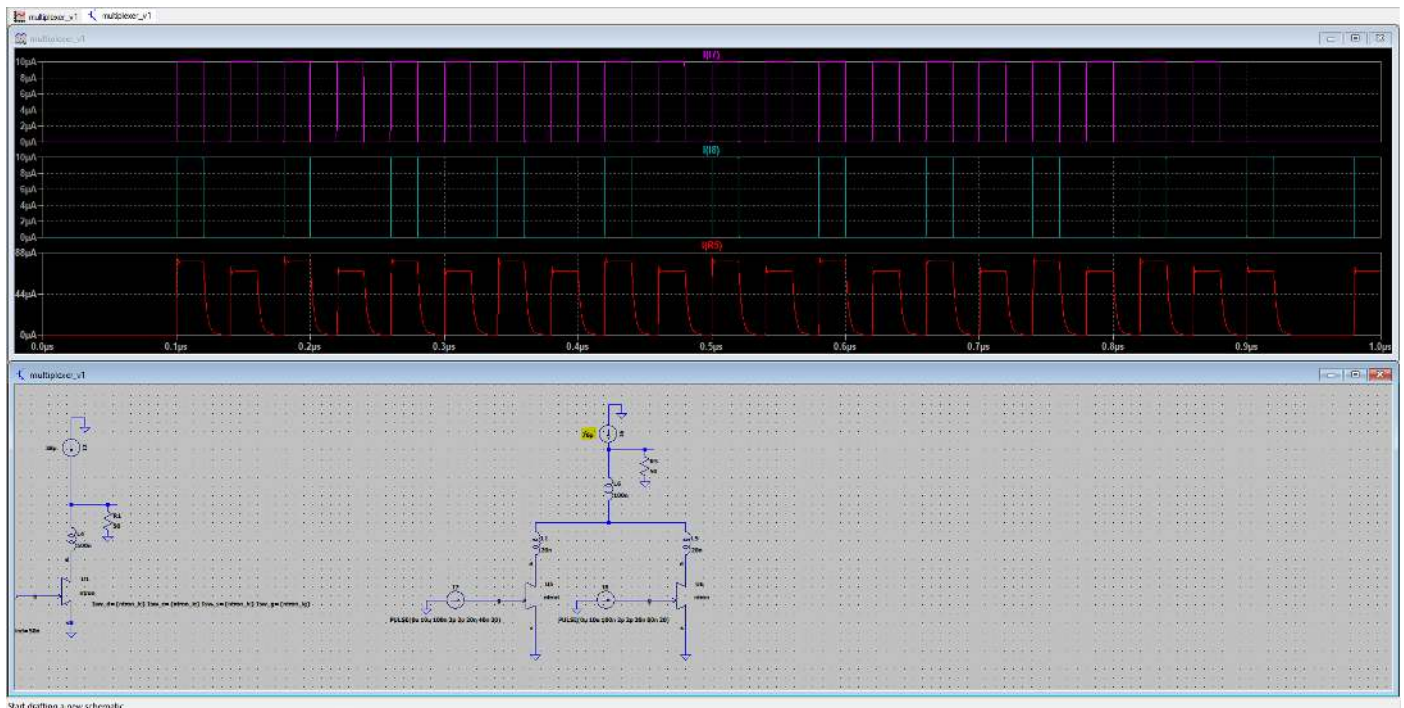


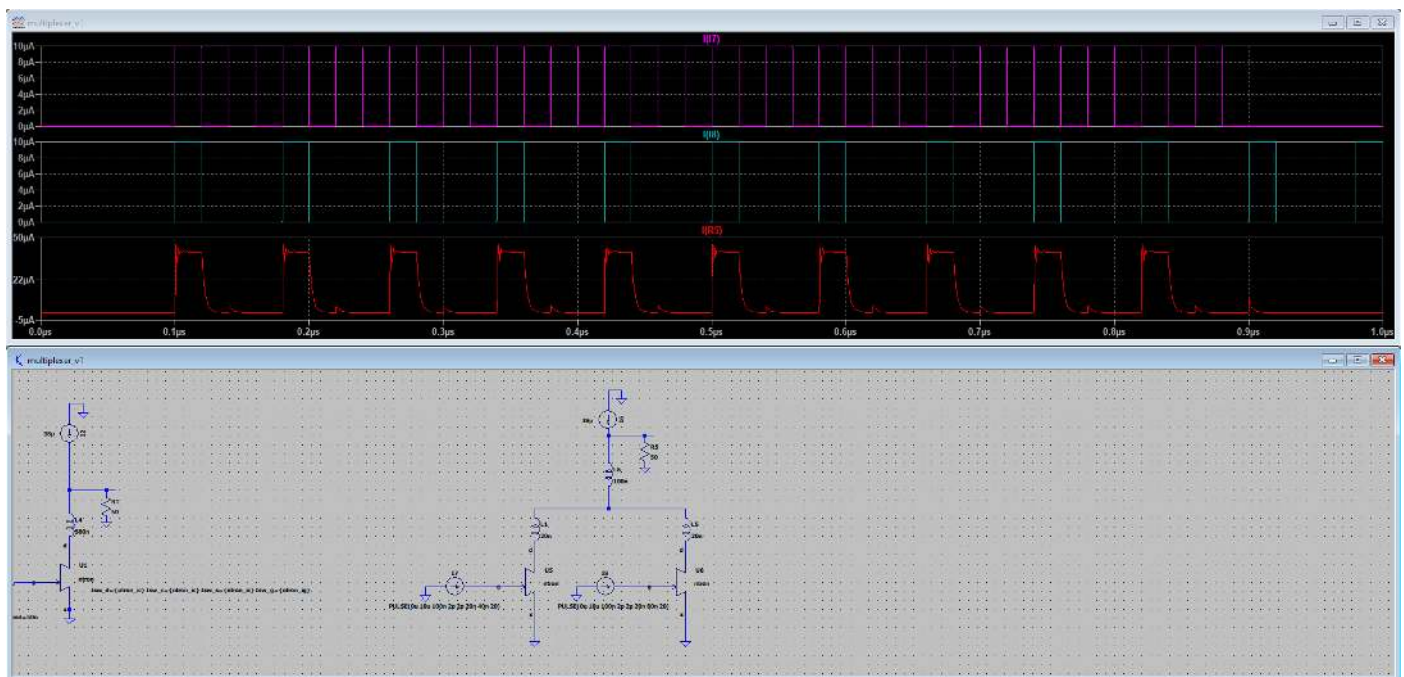
Figure 5-9: Circuit schematic for the SNSPD and nTron pulse amplifier experiment. (A), Device circuit schematic. The inductors were made by patterning long nanowires, which intrinsically produce kinetic inductance. The length of the inductor nanowires (and thus their total inductance) were scaled against the SNSPD, which had an approximate kinetic inductance of $L_k \approx 25$ nH. (B) Room-temperature readout and bias electronics. Pulses generated from the device and output to the coax in (a) arrived at the other end of the coax, shown in (b), where they were amplified with three 20-3000 MHz amplifiers in series before being input to the scope.



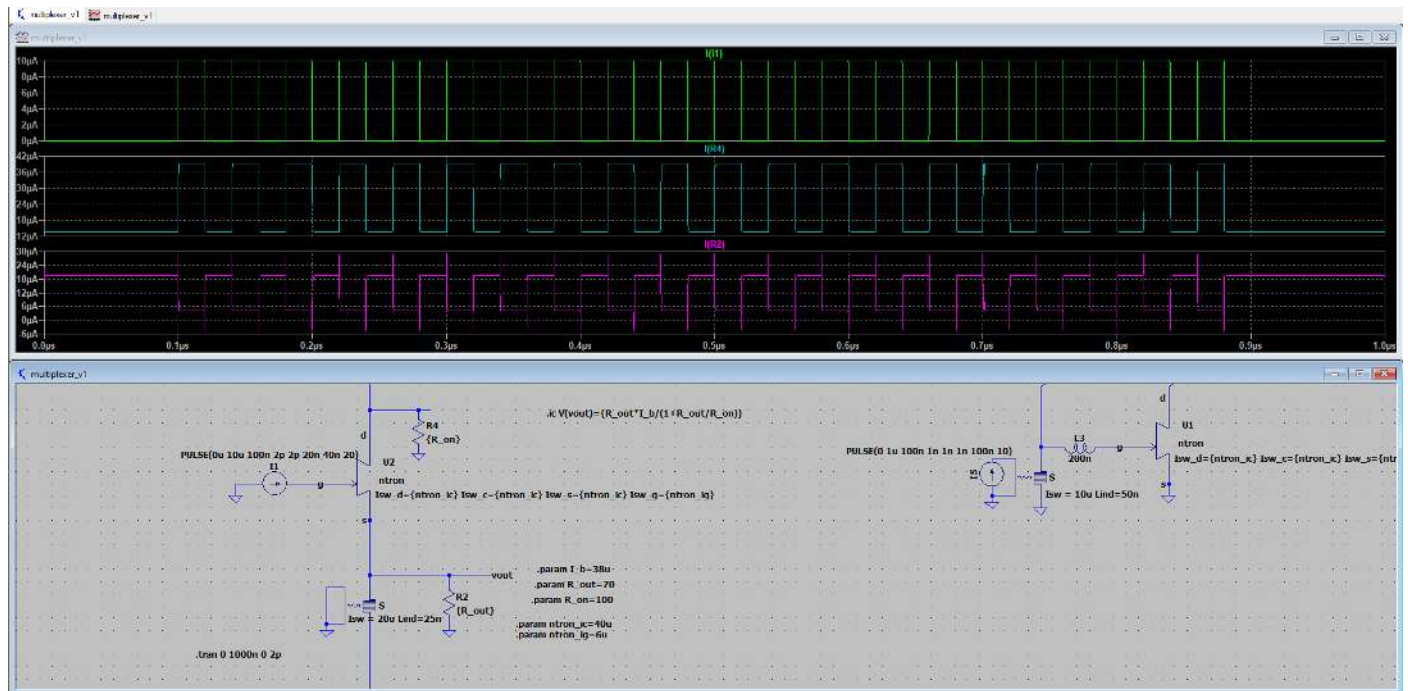
SNSPD AMP



OR GATE



AND GATE



NOT GATE

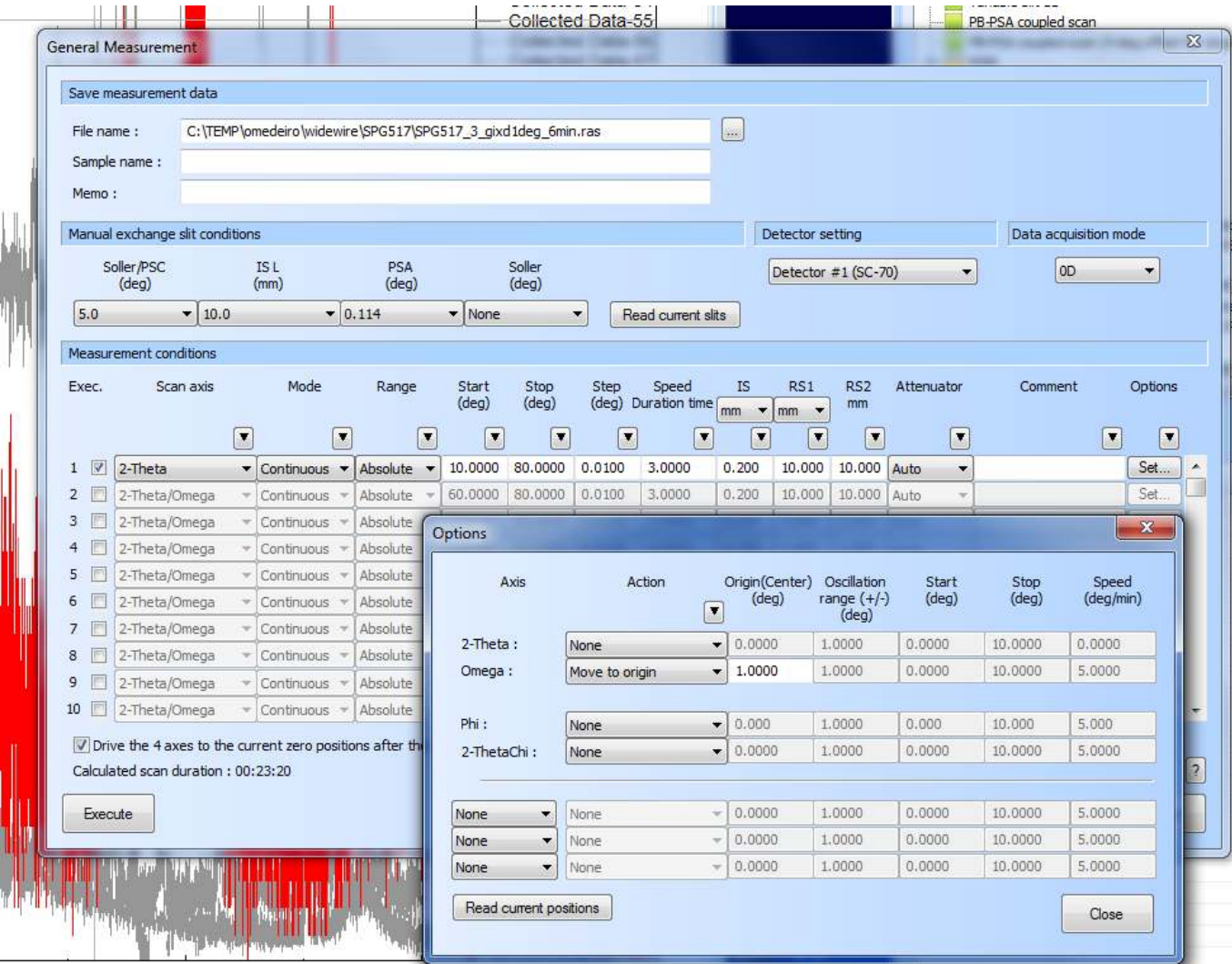
wide wire nbn XRD measurement

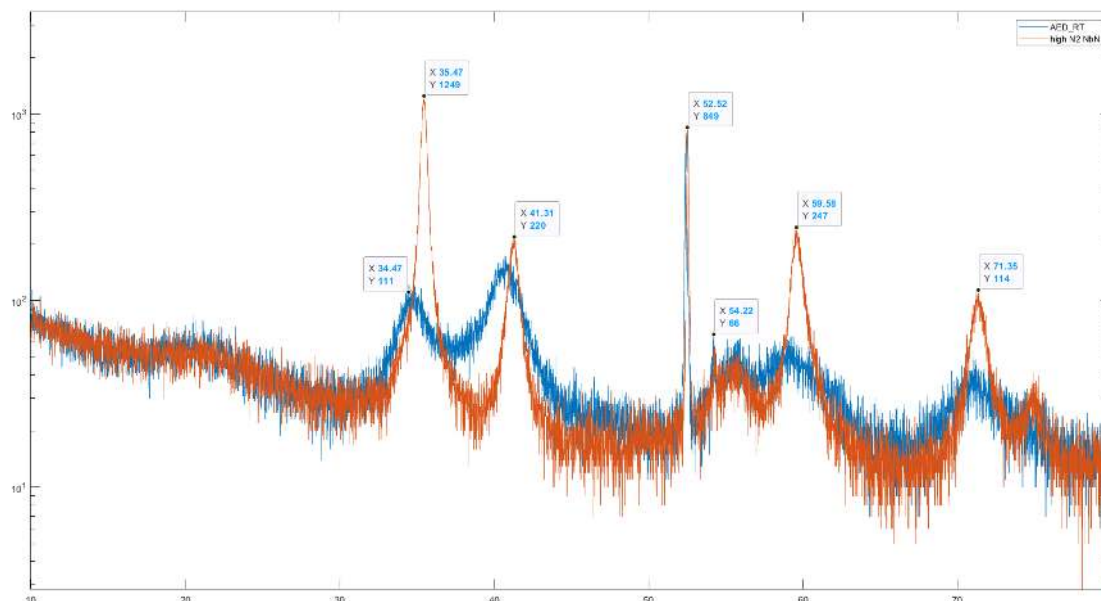
October 31, 2021
Categories: General

2-theta/omega scans the vertical axis of your film. So for thin films this is useless.

2-theta scan with a 1deg incident angle is GIXD measurement. the correct way to measure thin films.

On Smartlab: PB-PSA GIXD





4

S. Kalal et al. / Journal of Alloys and Compounds 851 (2021) 155925

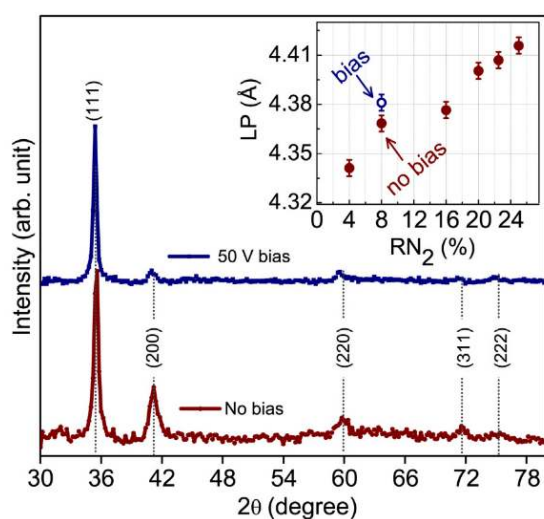


Fig. 3. XRD patterns of NbN sample grown with 50 V substrate rf-biasing and without biasing. Inset shows variation in LP with R_{N_2} .

increase in LP is an indication of lattice expansion caused by excess N within NbN. The inset of Fig. 3 compares variations in the LP of NbN thin films with R_{N_2} and applied bias. The LP increases signif-

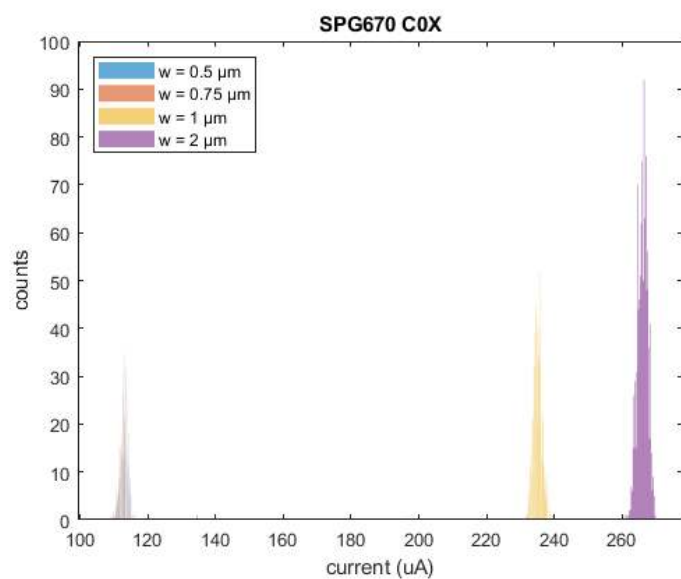
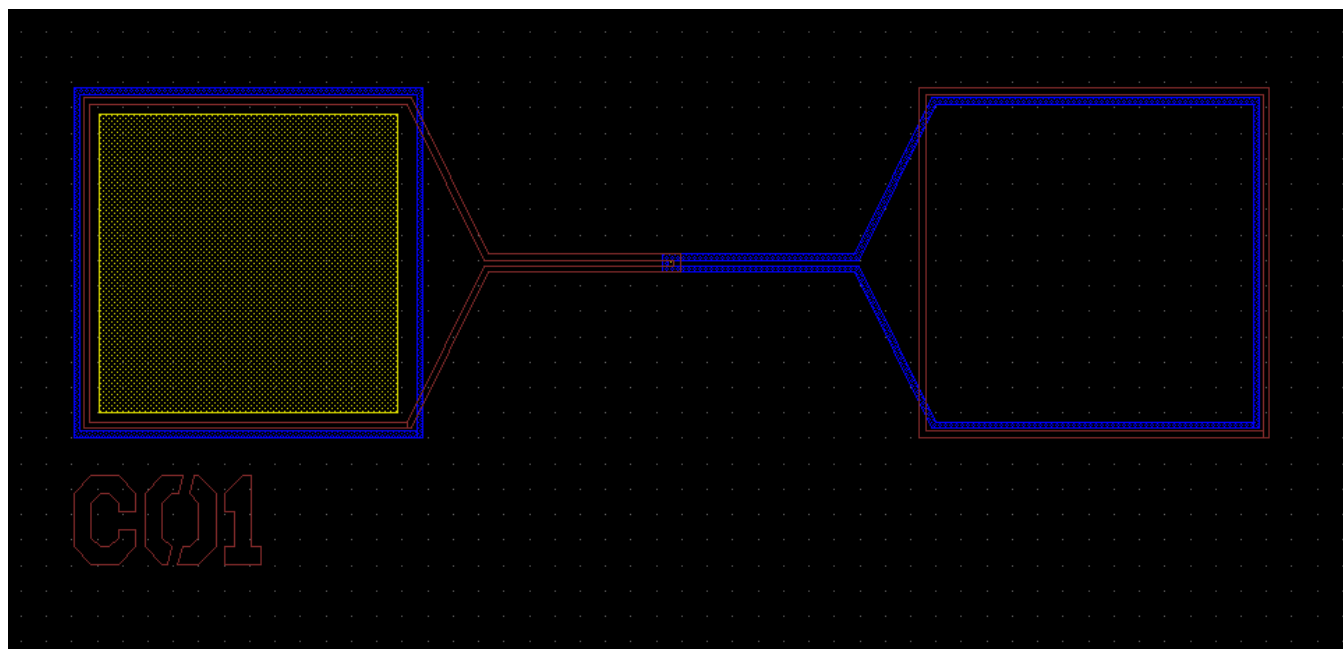
in $R_{N_2} = 1\%$ sample can be explained due to presence of stronger disorder. Here, it may be noted that the particle size in $R_{N_2} = 0.5$ and 1% samples were found to be almost similar.

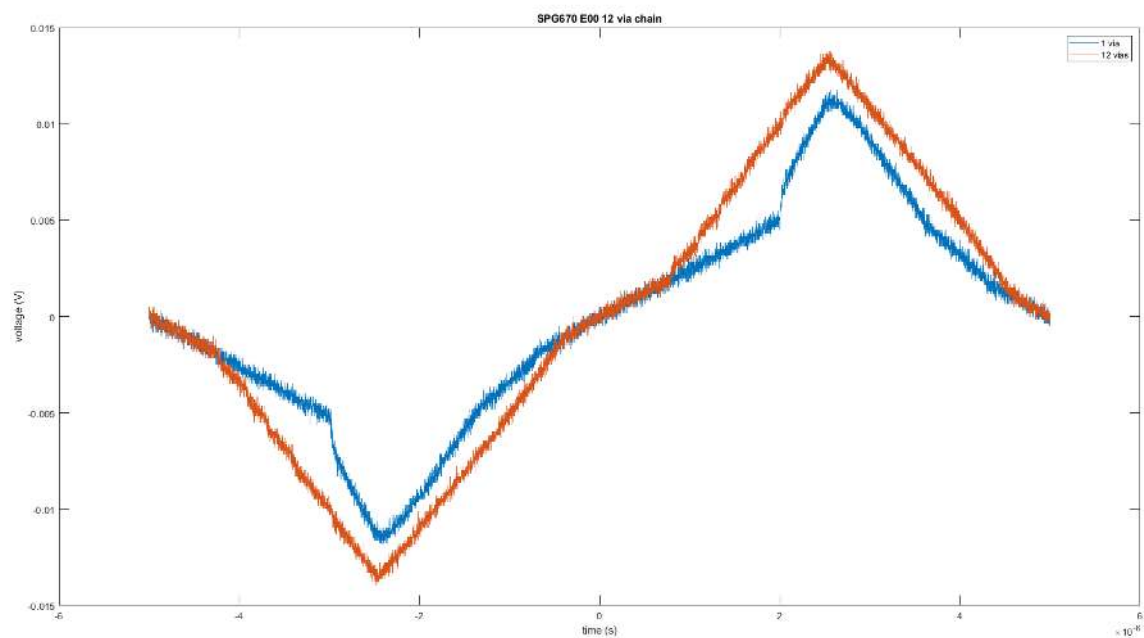
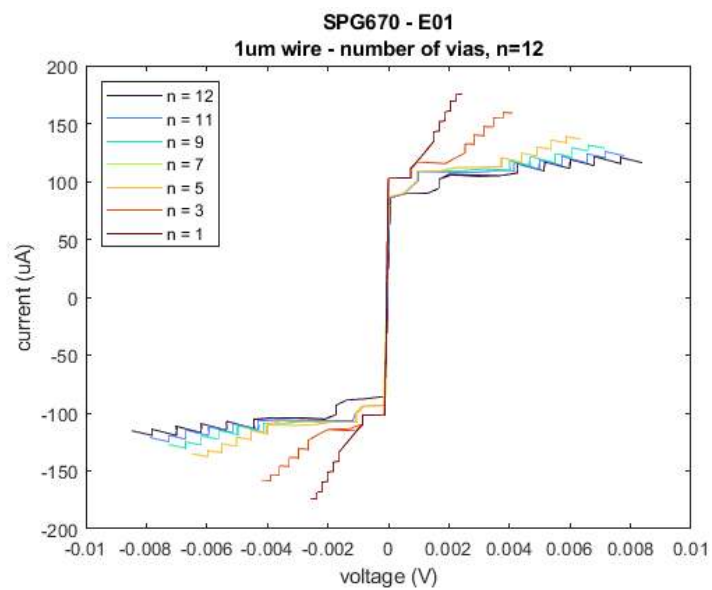
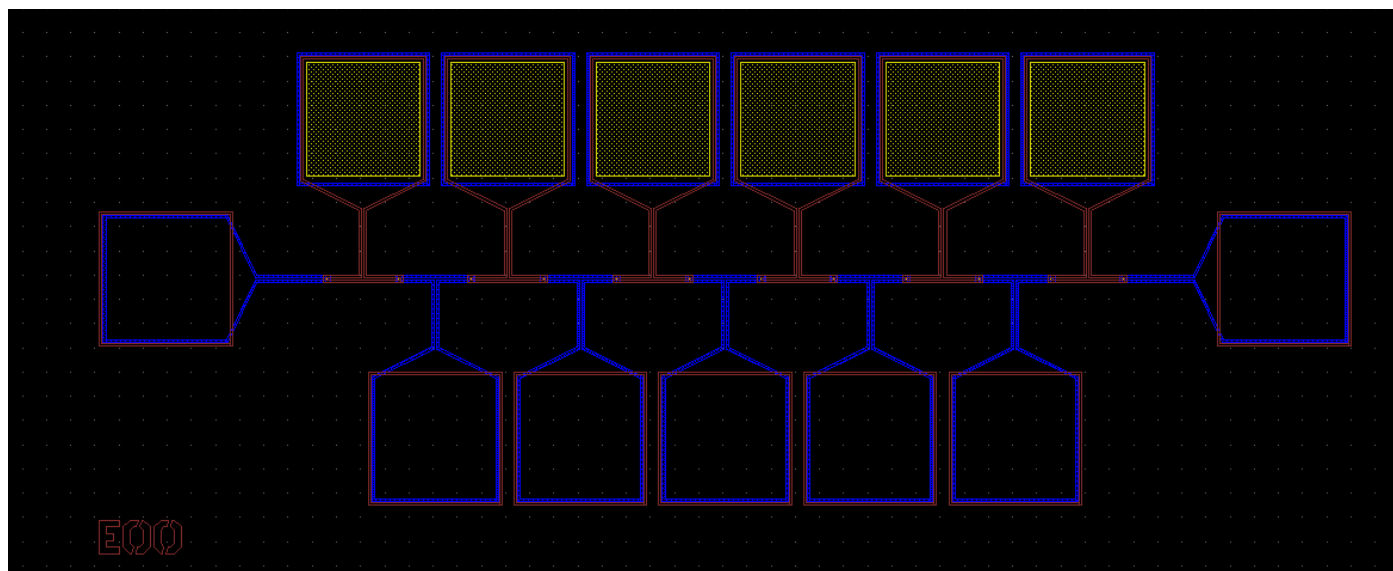
When the R_{N_2} was increased to 4%, again a superconducting transition was observed at 9.39 K as shown in Fig. 4(a). It is worth to mentioning here that this sample contains a mixture of Nb(N) and NbN phases. With a further rise in R_{N_2} values to 8 and 16%, the T_C increases significantly to 12.24 and 12.83 K, respectively. With an applied bias voltage also the T_C increases marginally to 13.2 K (see Fig. 4(a)). However, when we increased the R_{N_2} to 20, 22.5 and 25%, the T_C get reduced to 7.91, 7.24 and 6.87 K, respectively. The values of T_C are also listed in Table 2. It may be noted that the highest experimental T_C value found so far in NbN was 17.3 K (see Table 1). Further, the sample grown at $R_{N_2} = 30\%$ did not reveal any superconducting transition down to 3 K (see Fig. 4(b)). In $R_{N_2} = 65\%$ sample, the resistivity takes an upturn at low temperatures, mimicking an insulator like transition which may stem due to disorder caused by the excess N in NbN [52]. Correlating the structure and superconductivity of NbN, it can be observed that the T_C of NbN is highly sensitive to N concentration. Between $R_{N_2} = 8$ to 16%, the T_C maximizes around ≈ 13 K and below and above these R_{N_2} values, the T_C decreases. This behavior is amply demonstrated in the Fig. 4(c). From here it appears that the stoichiometric NbN phase can be obtained between $R_{N_2} = 8$ to 16%. The reduction of T_C for $R_{N_2} < 8\%$ was due to N deficiency in NbN. Similarly, NbN films have excess N when R_{N_2} exceeds 16%. The incorporation of N atoms results in a continuous increment in the LP as shown in the inset of

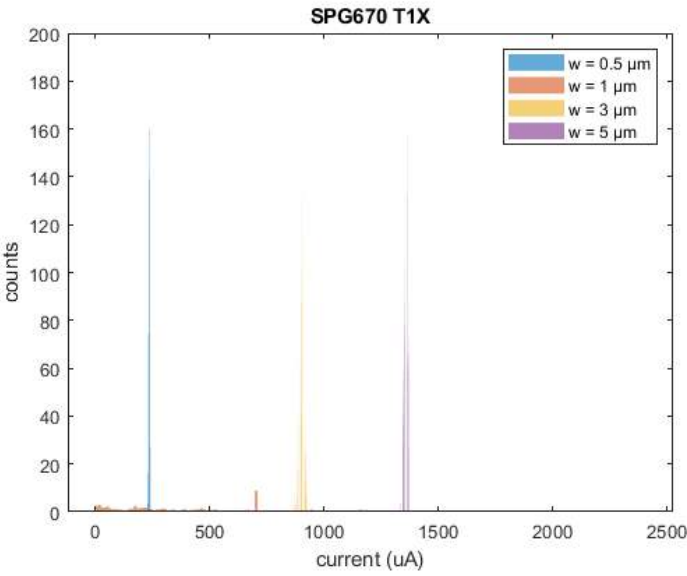
Superconducting vias

January 5, 2022

Categories: Electronics, Fabrication





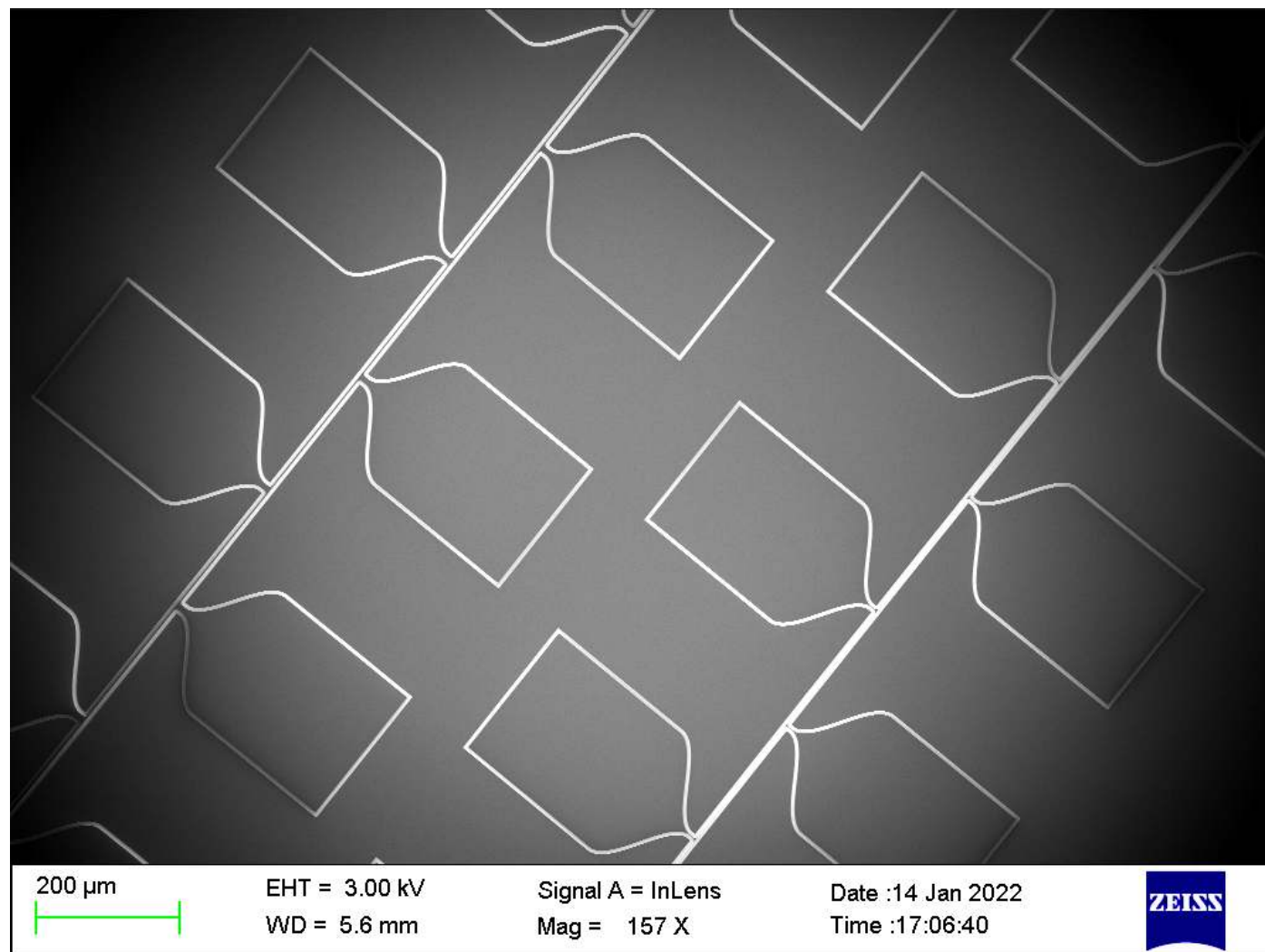


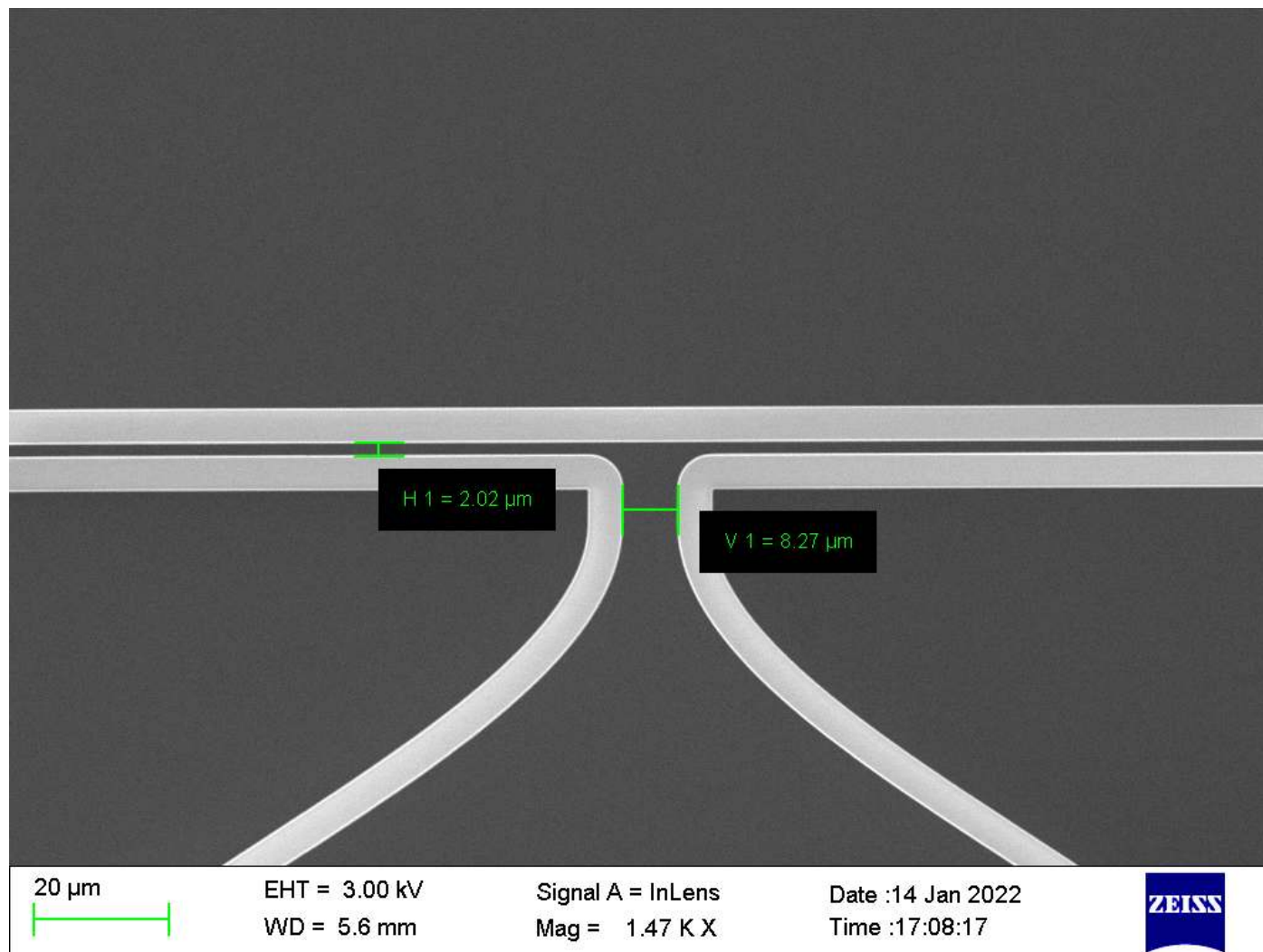
Long wire taps SPG678

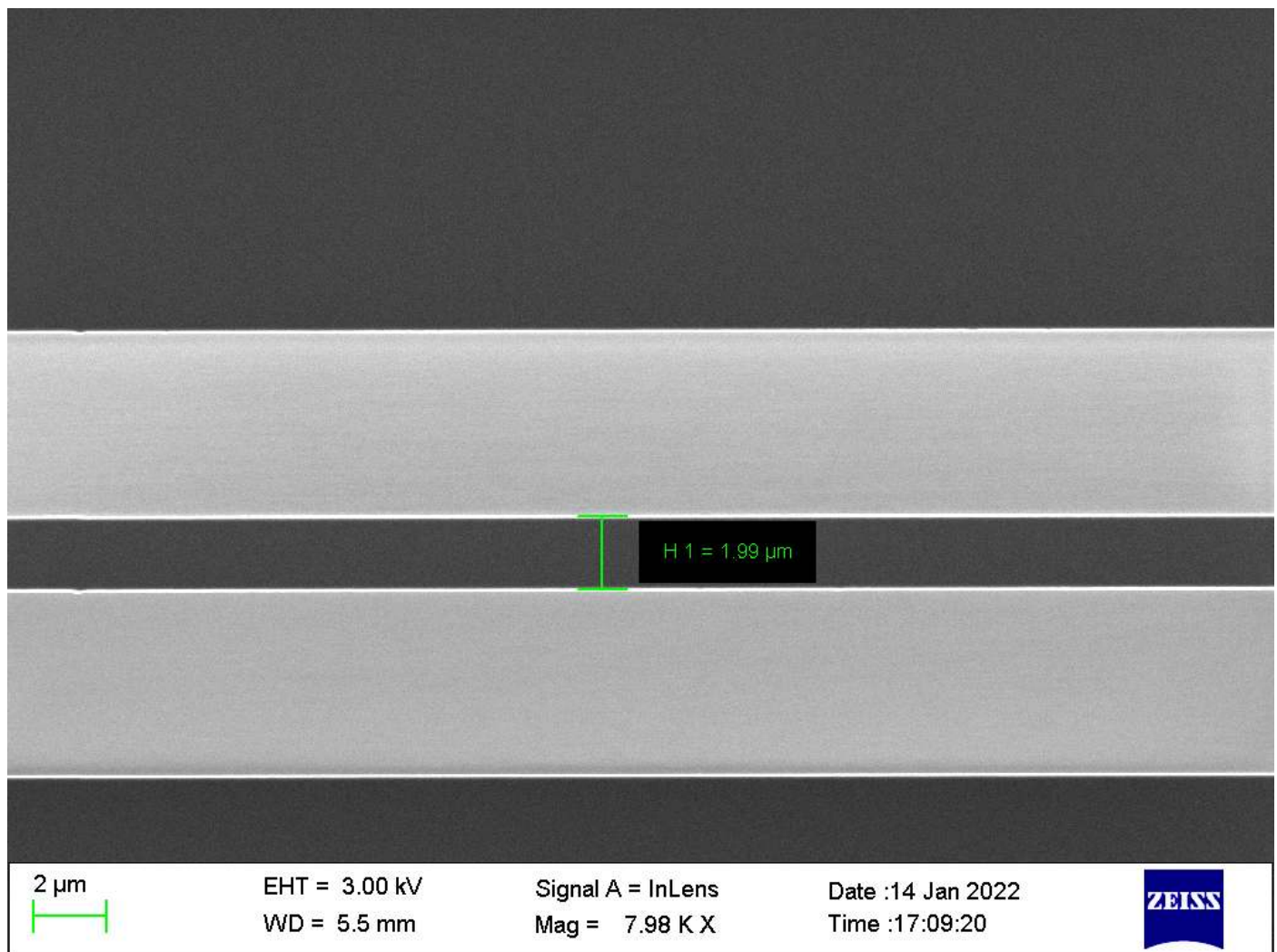
January 19, 2022

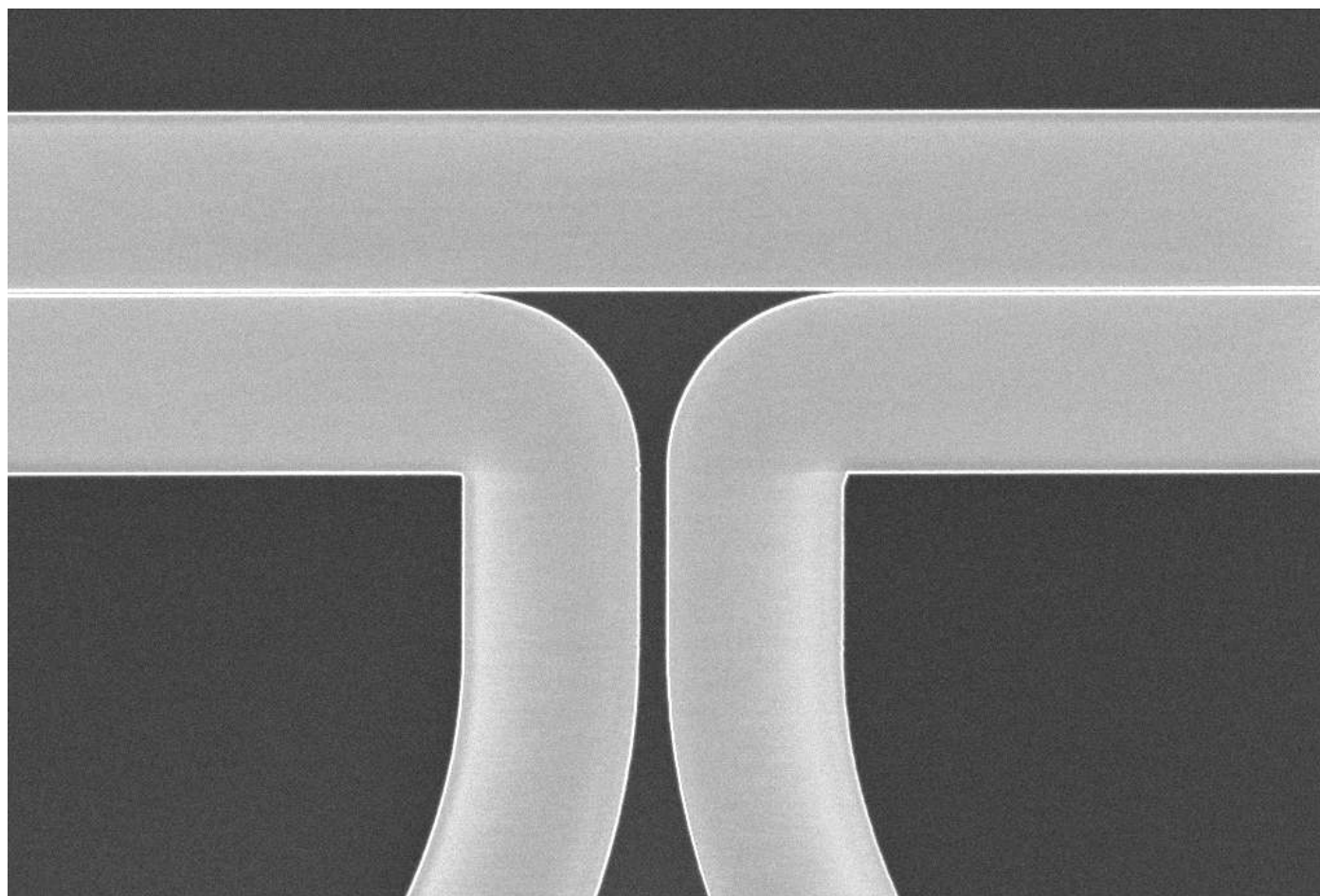
Categories: General

The purpose of this experiment is to see how switching current changes with wire length for two different widths. The switching current should decrease as a function of length as more constrictions (due to fabrication or material defects) are introduced. If a particular segment shows a large decrease it would be interesting to image that section and see if there is any obvious defect that would cause the decrease.









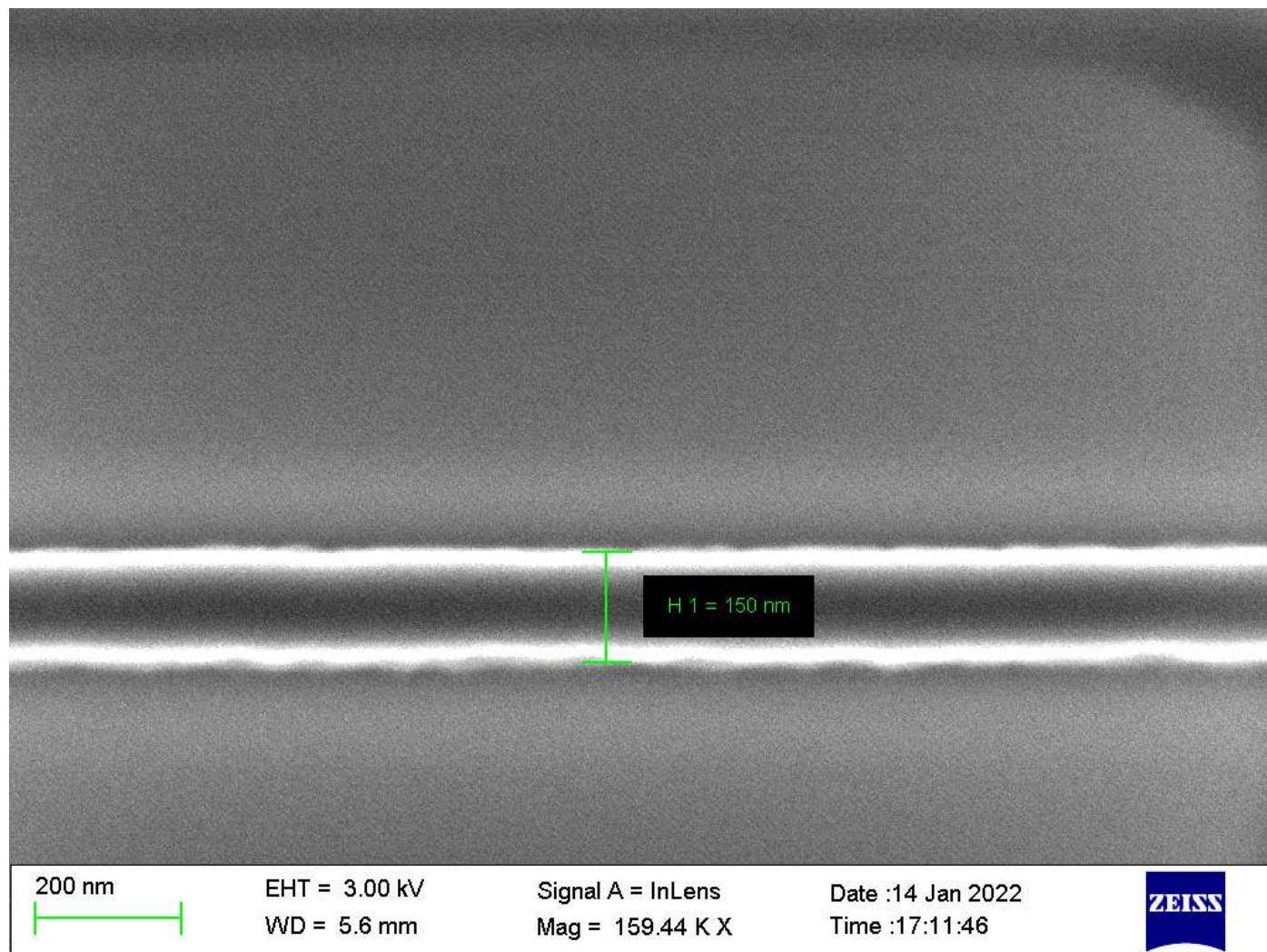
2 μm

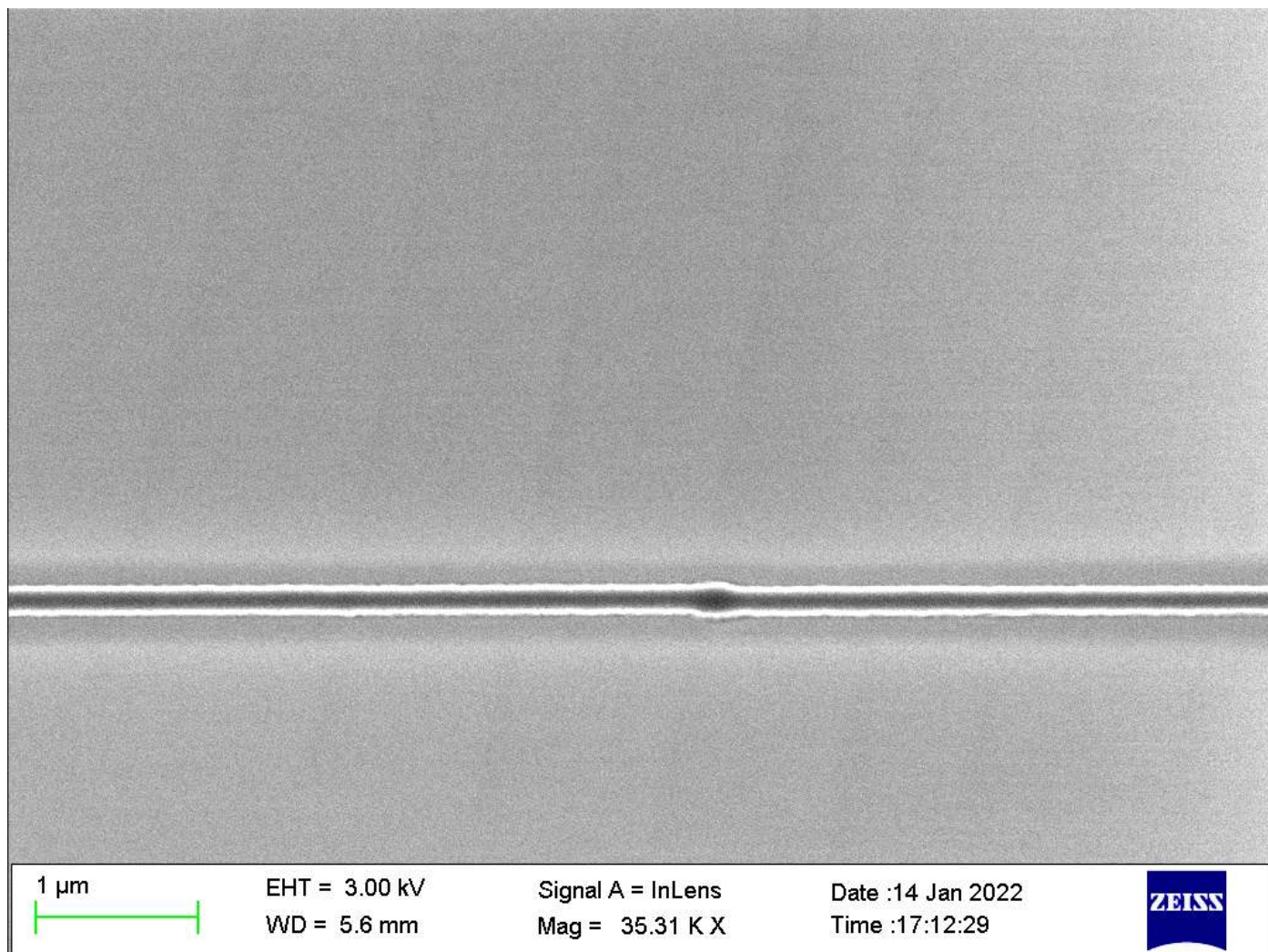
EHT = 3.00 kV
WD = 5.6 mm

Signal A = InLens
Mag = 7.27 K X

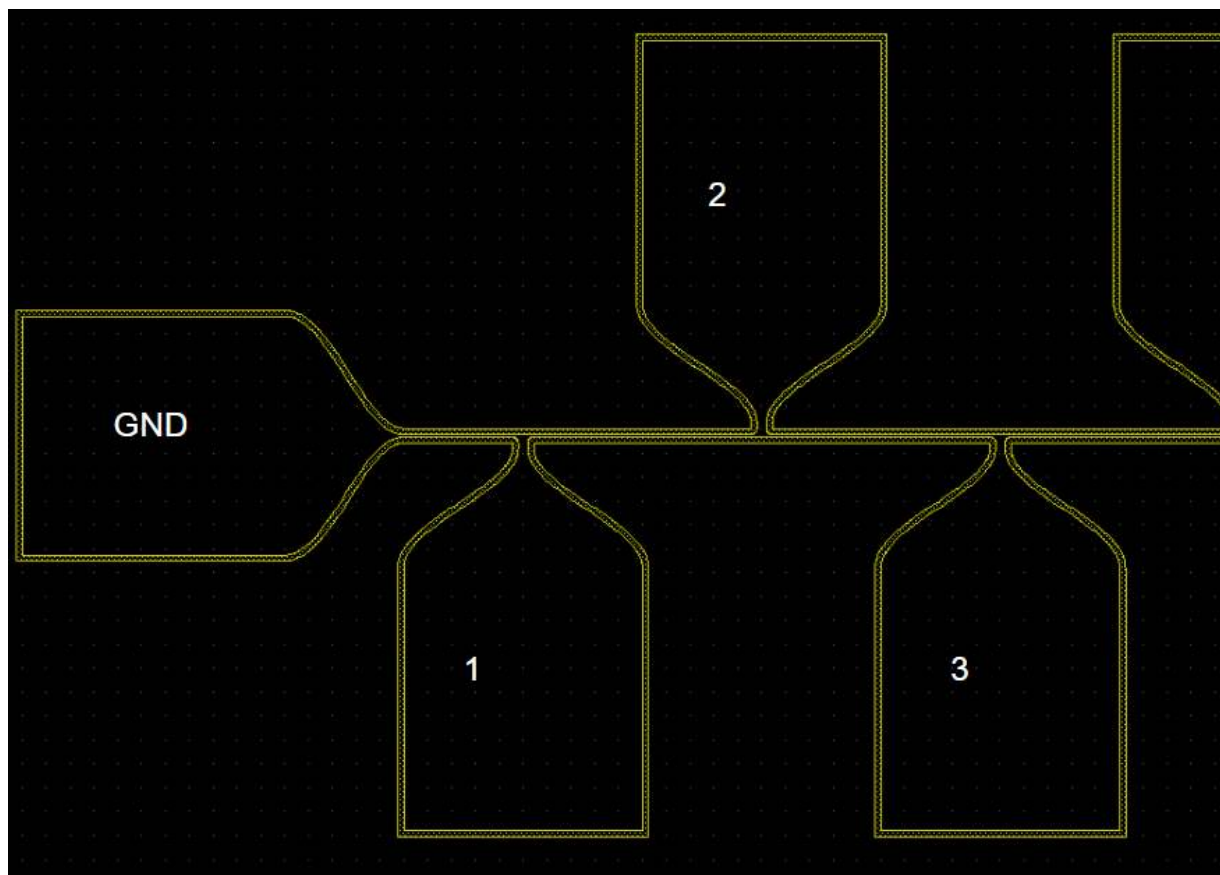
Date :14 Jan 2022
Time :17:10:16



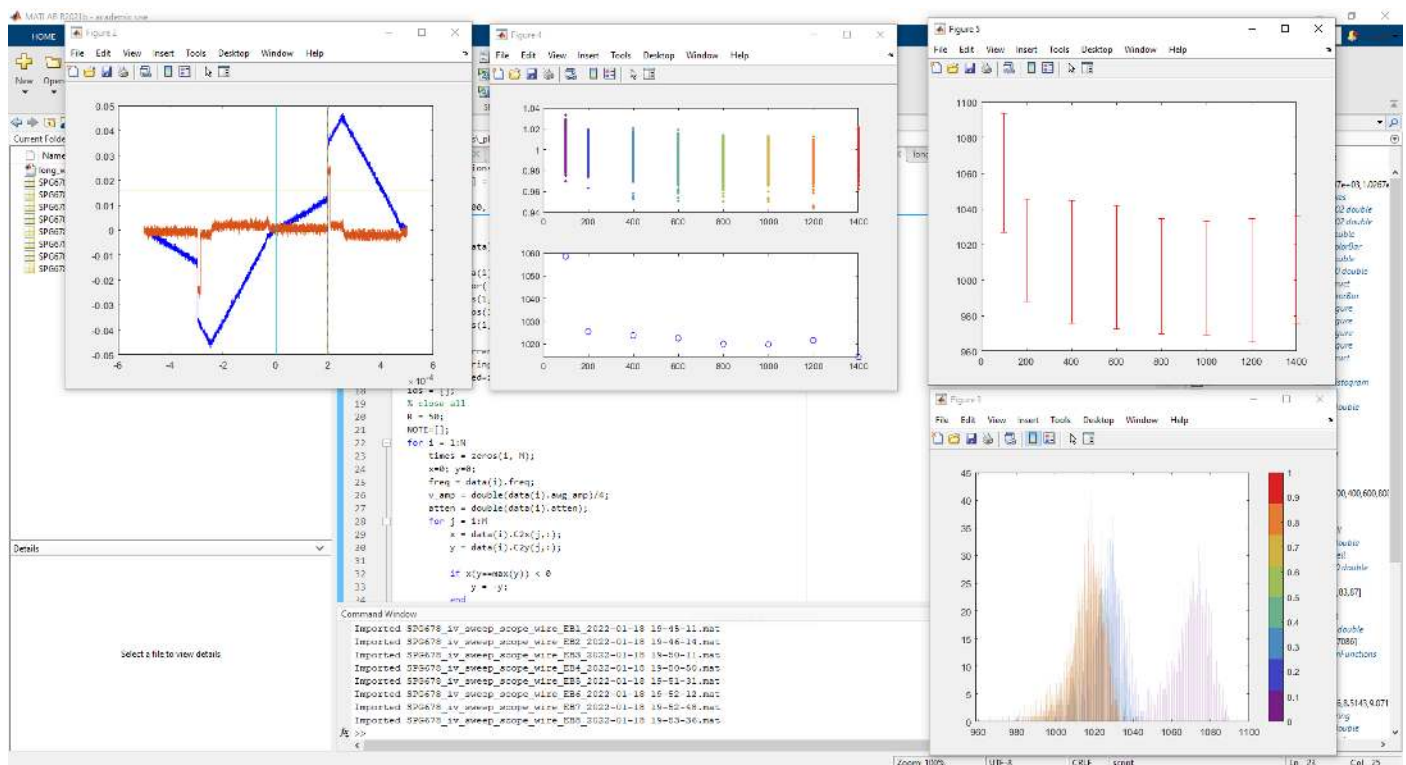


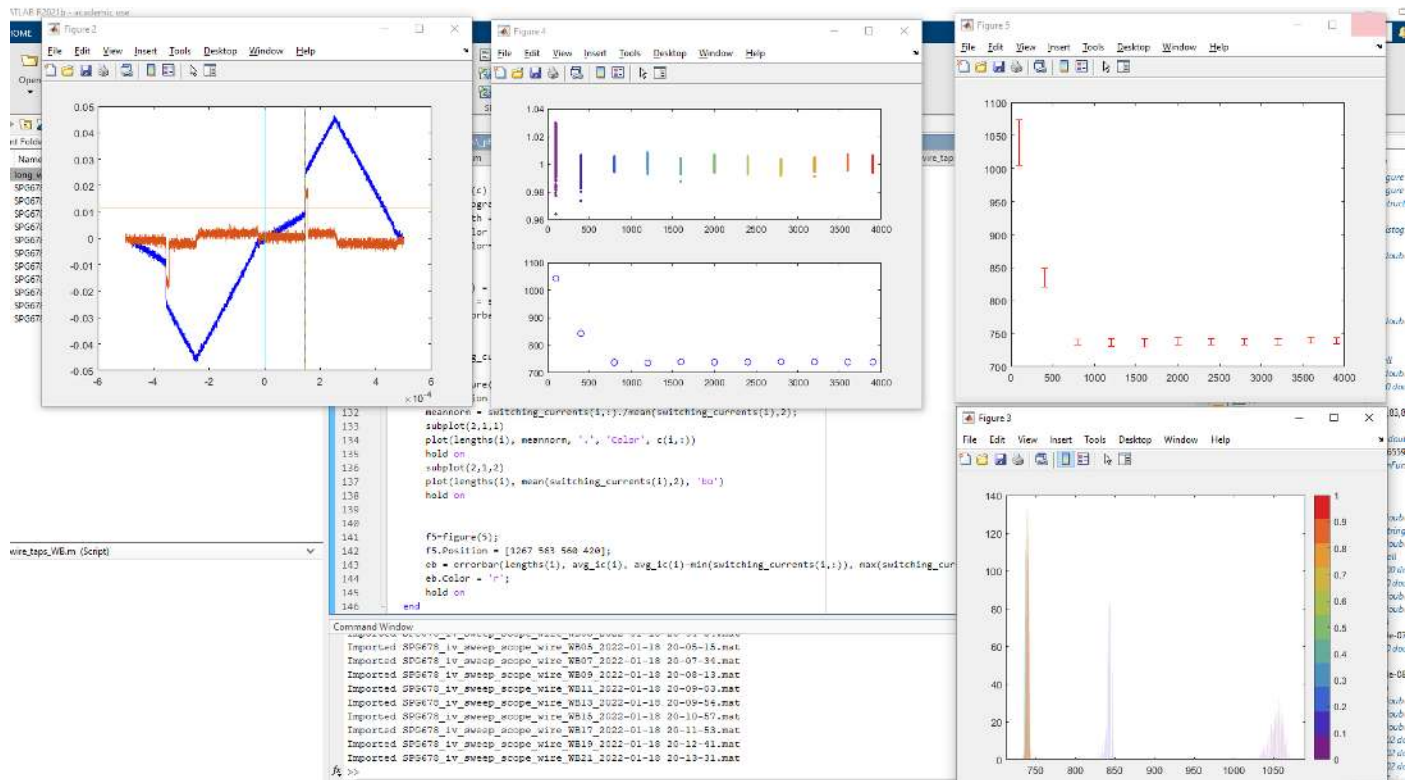


Typical multipass overlap error ^^^

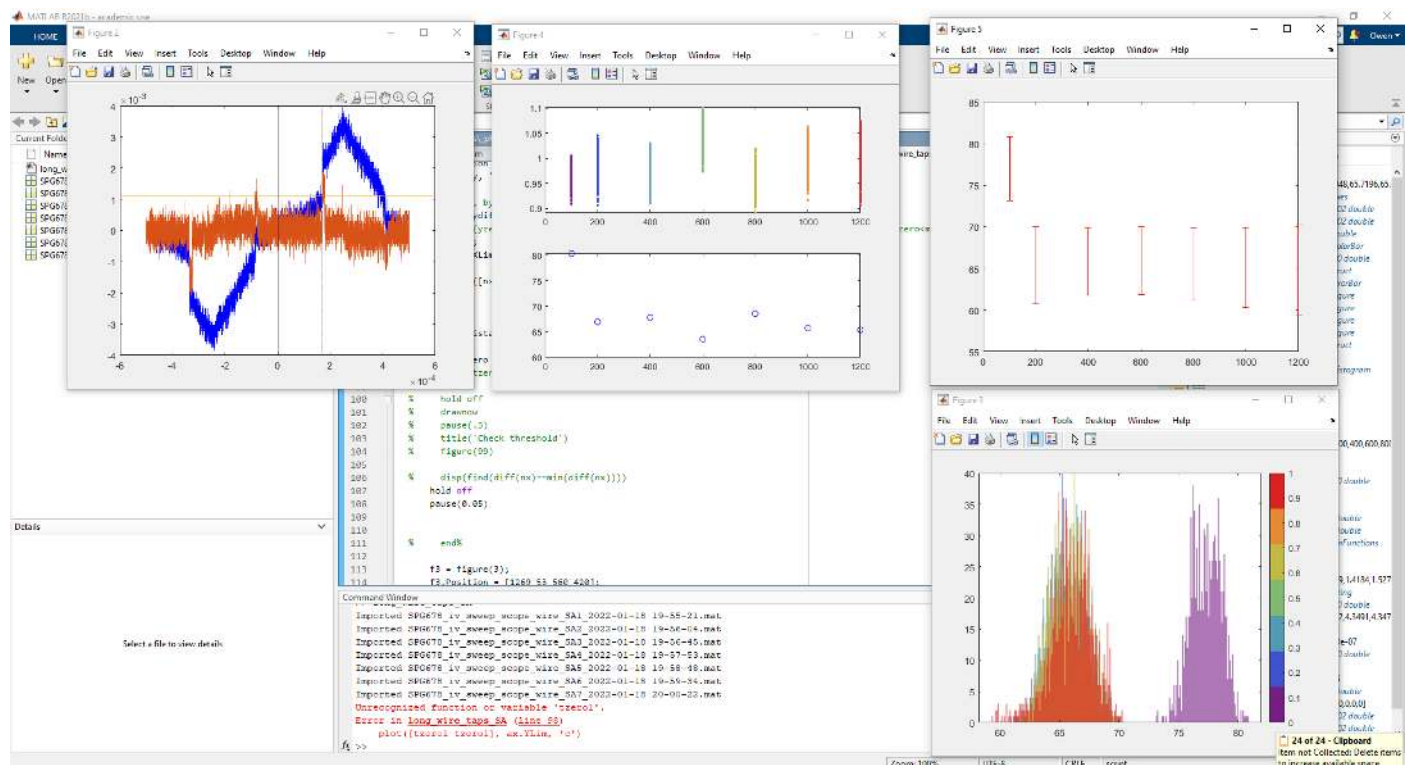


2um wide wire. Figure 4,5 axis is length (um).



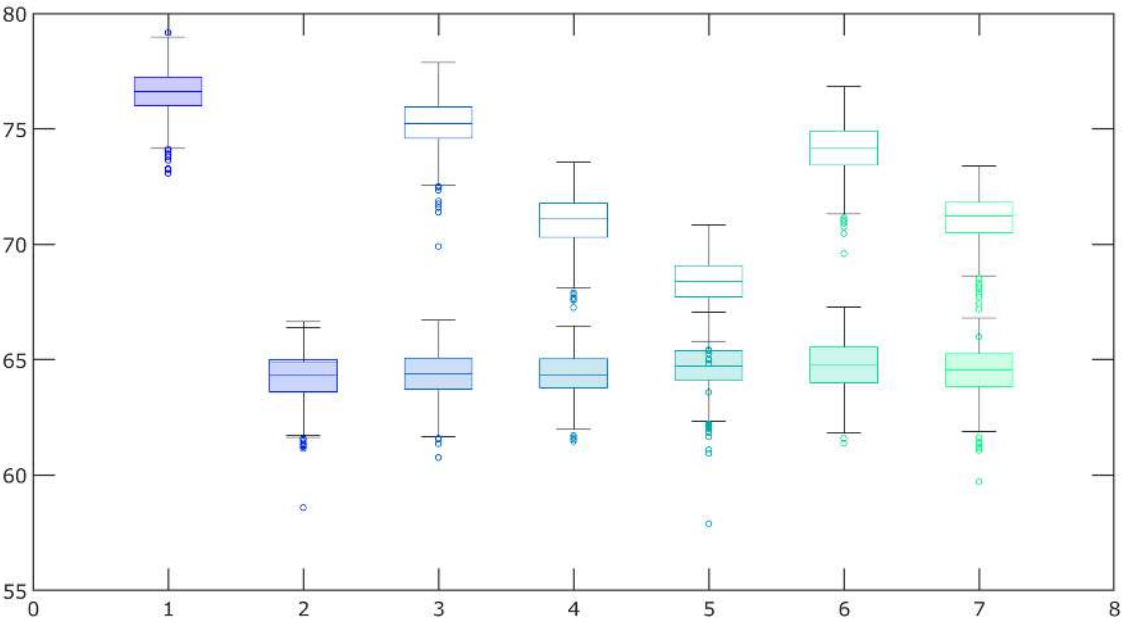


200nm (150nm actual) wire

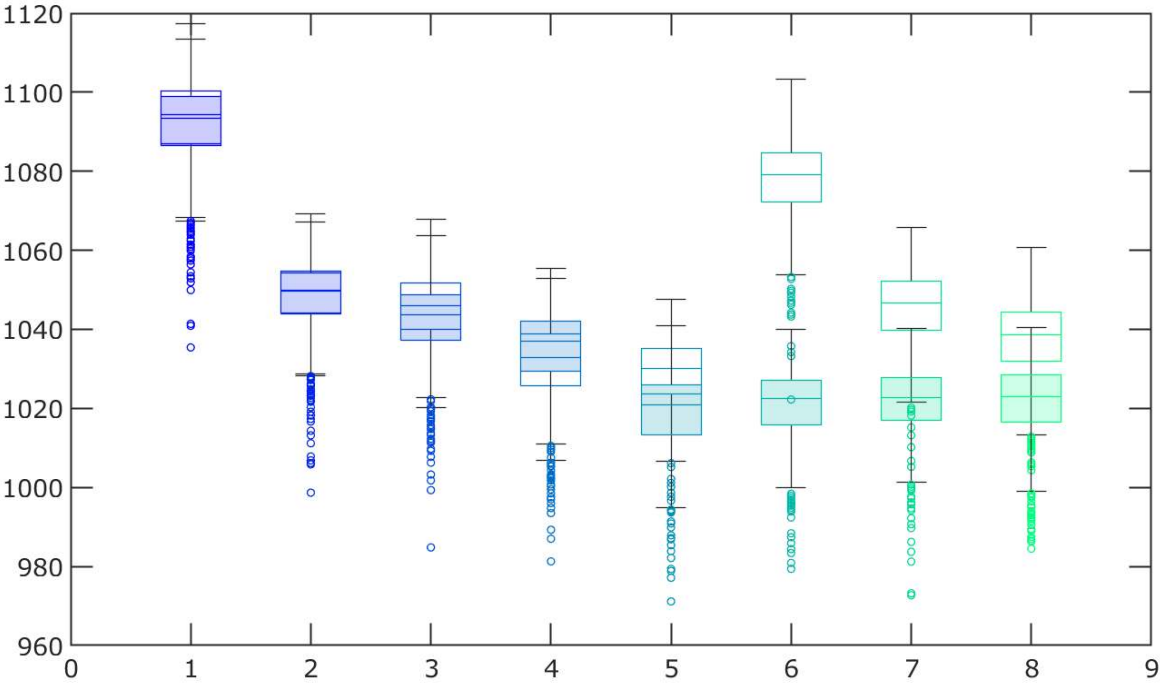


Both the 2um and the 200nm wires show a decrease after the first segment and flat I_c after. This could be that the edge/corner of the chip has more constrictions. It would be good to test center segments of increasing length. Also measure from the other end first to see if it is due to measurement/bonding.

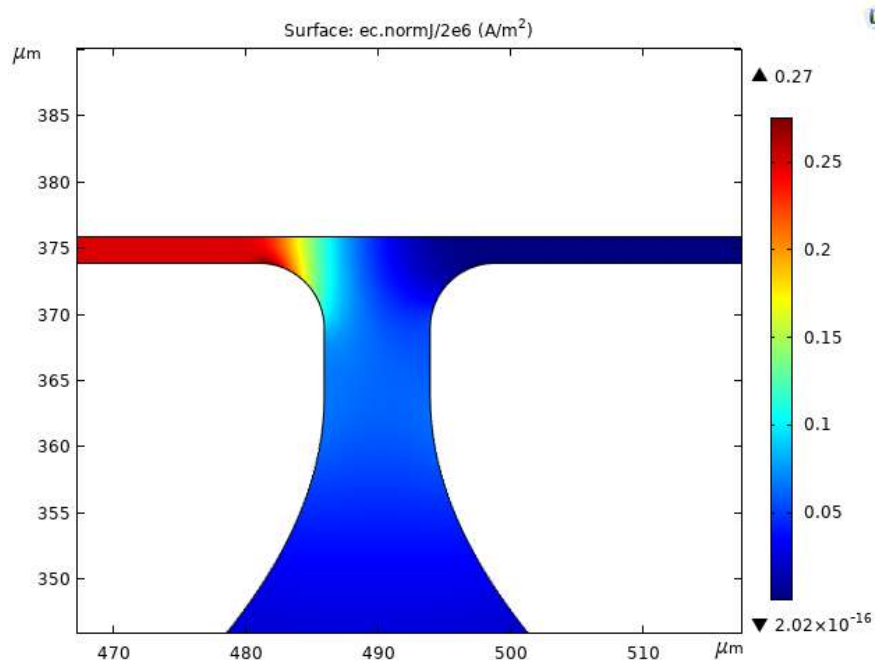
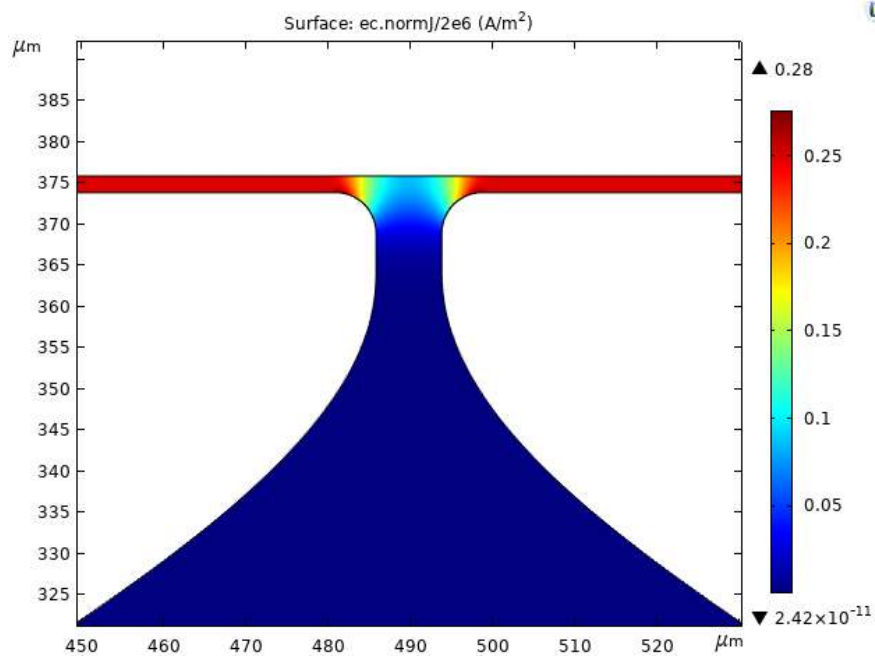
200nm device. This data set contains measurements from N-to-0 and N-to-N-1. For example. 1-0 is the same for both options. the data at 2 is 2-0 and 2-1, which is pretty much the same. the measured data beyond that the lower critical



2μm



Current density simulation



Max current density is the same (0.28, 0.27) for end to end vs end to side. ie no current crowding due to corners.

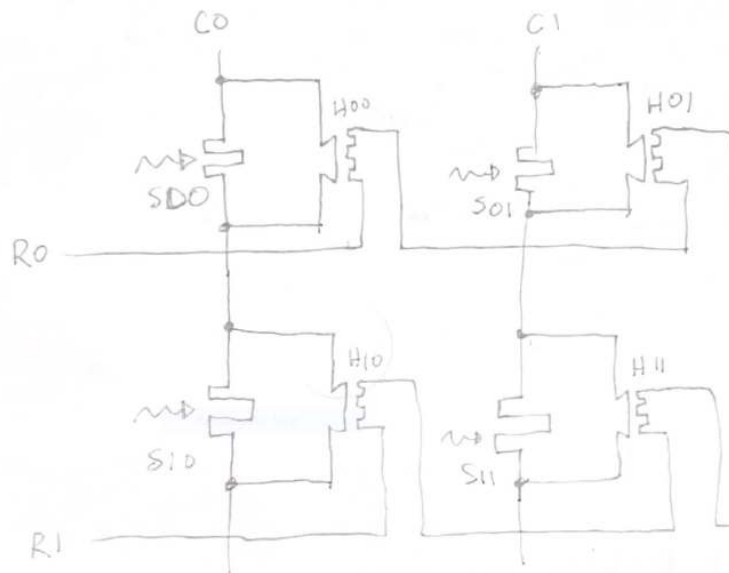
SNSPD 1-Bit array

January 26, 2022

Categories: Electronics, SNSPD, SPICE, Superconductivity

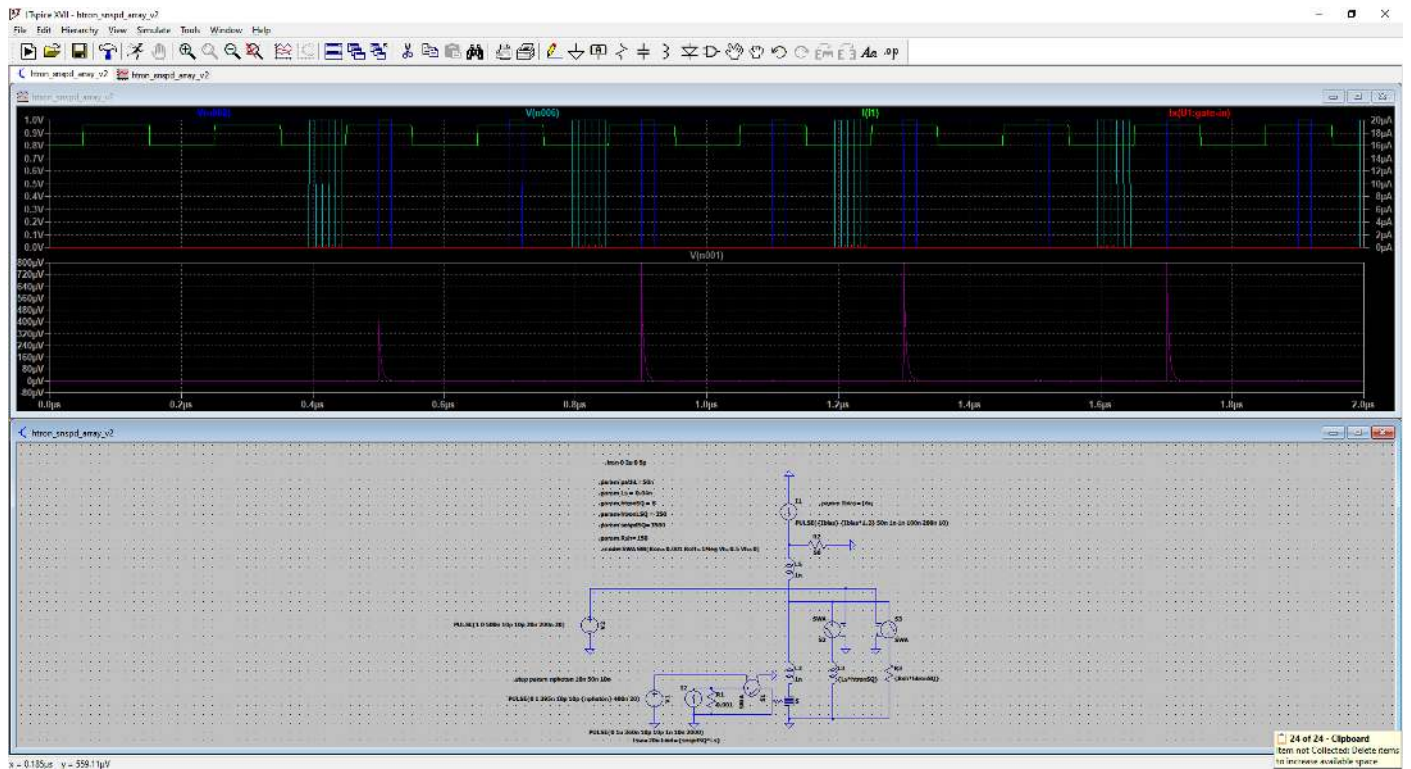
2022-01-22-Note-12-02.pdf

Simpler 1-bit SNSPD array:

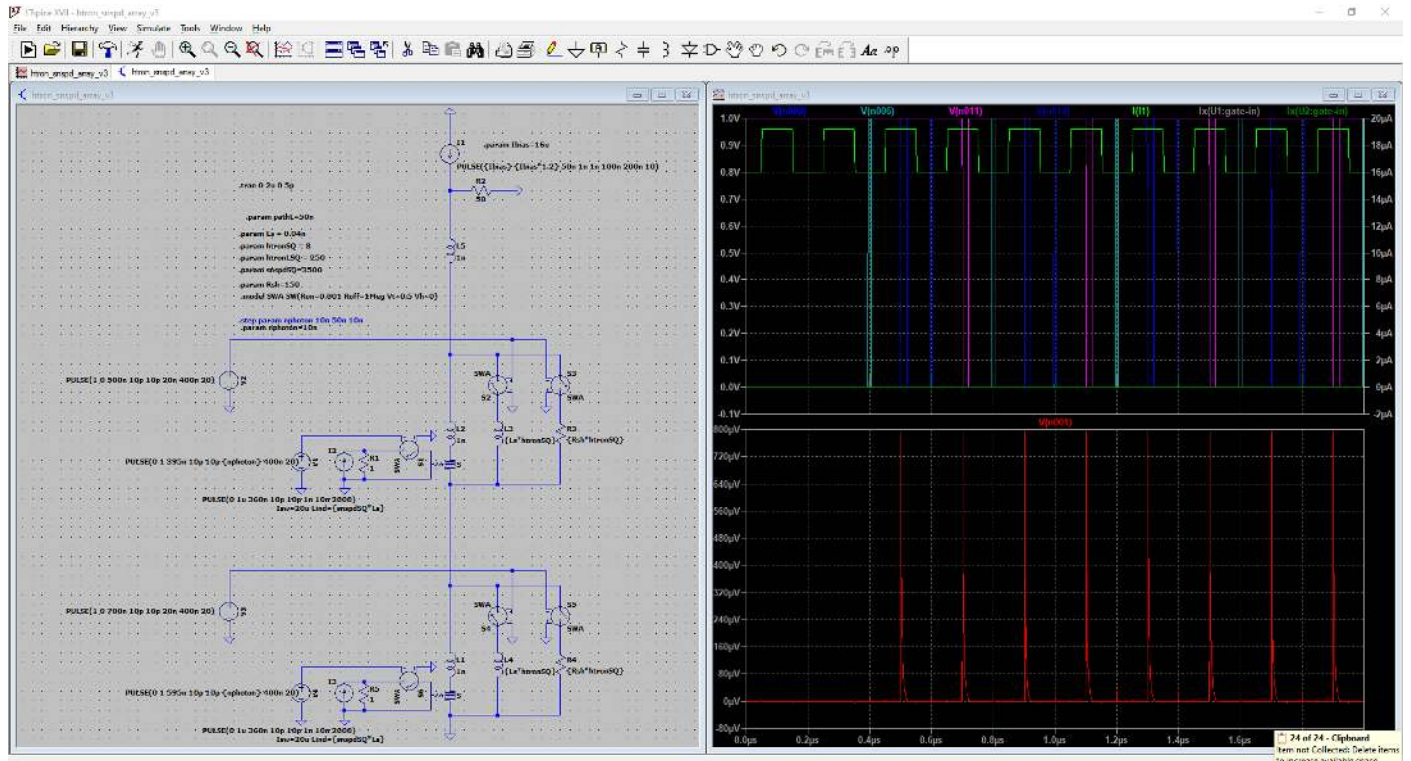


- ① turn on $C\phi \rightarrow C_N$ (BIAS)
- ② overbias $R_0 \dots R_N$ to clear loop currents. then turn off $R_0 \dots R_N$ (SET)
- ③ Allow photons to arrive & integrate (WRITE)
- ④ Apply read bias (a small increase) to $C\phi \rightarrow C_N$
- ⑤ Apply pulse to R_0 2 read voltages @ $C\phi \rightarrow C_N$
- ⑥ repeat ⑤ for ~~R0~~ $R_1, R_2 \dots R_N$ until entire array is read out.

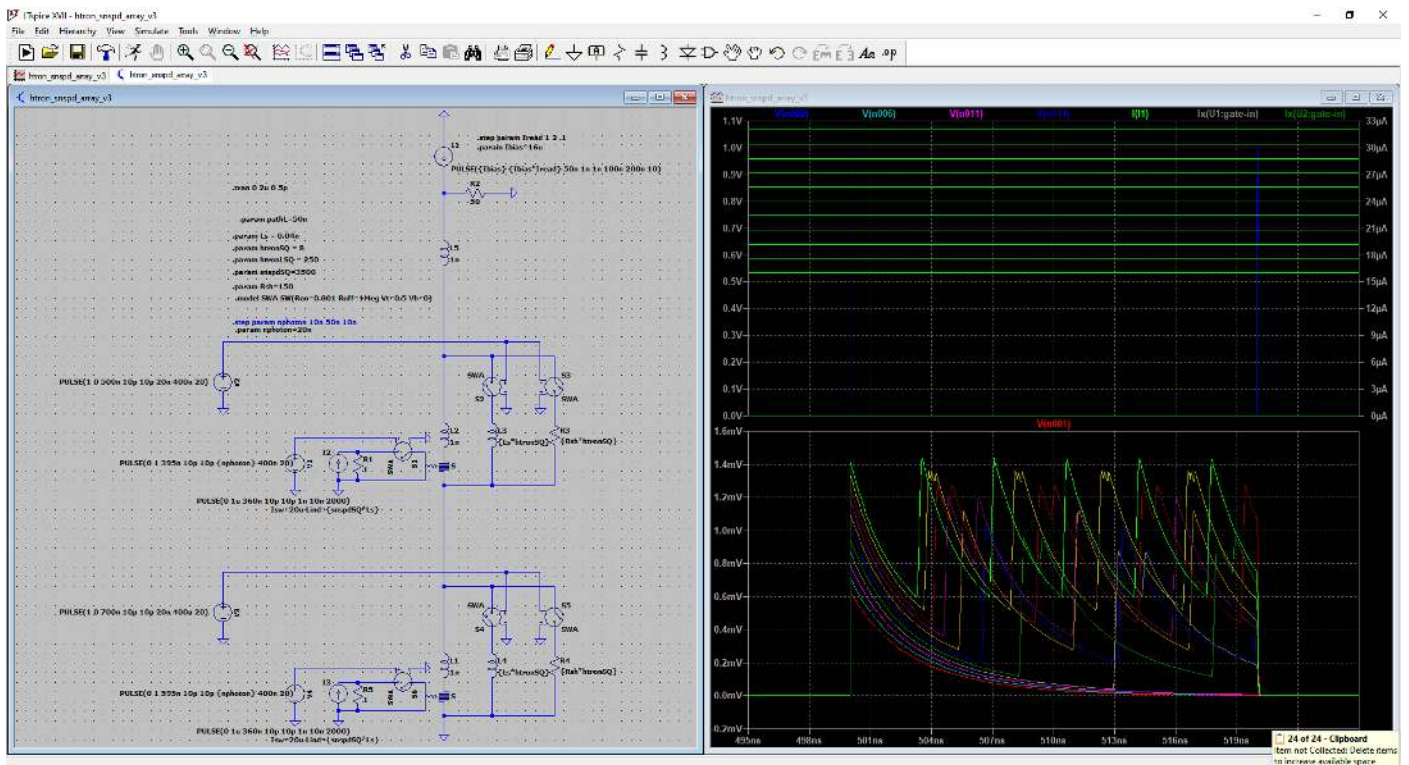
Thanks to Owen + Brenden for helpful ideas + discussion



Single Pixel. Step shows 1-5 photon pulses. No PNR on pulse height. Might have to change params/bias conditions.



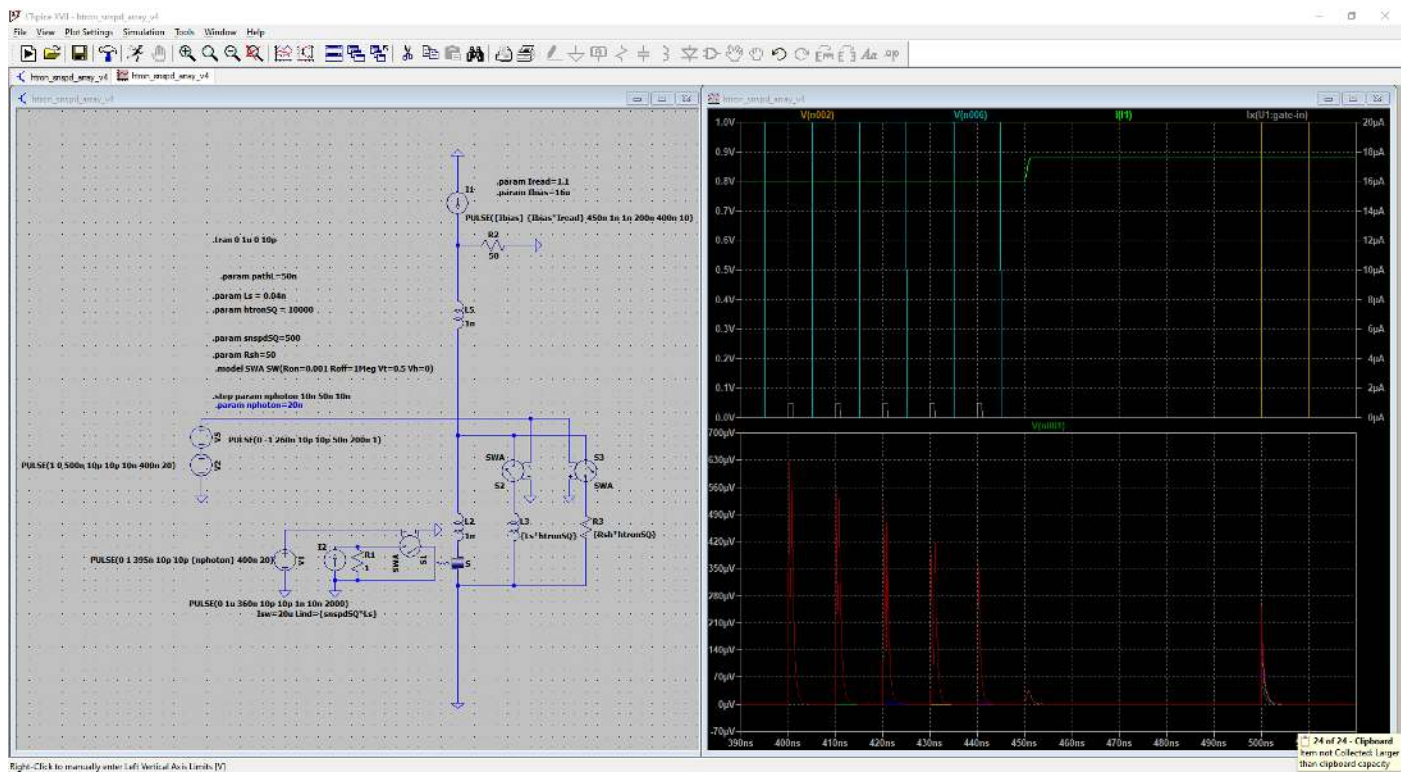
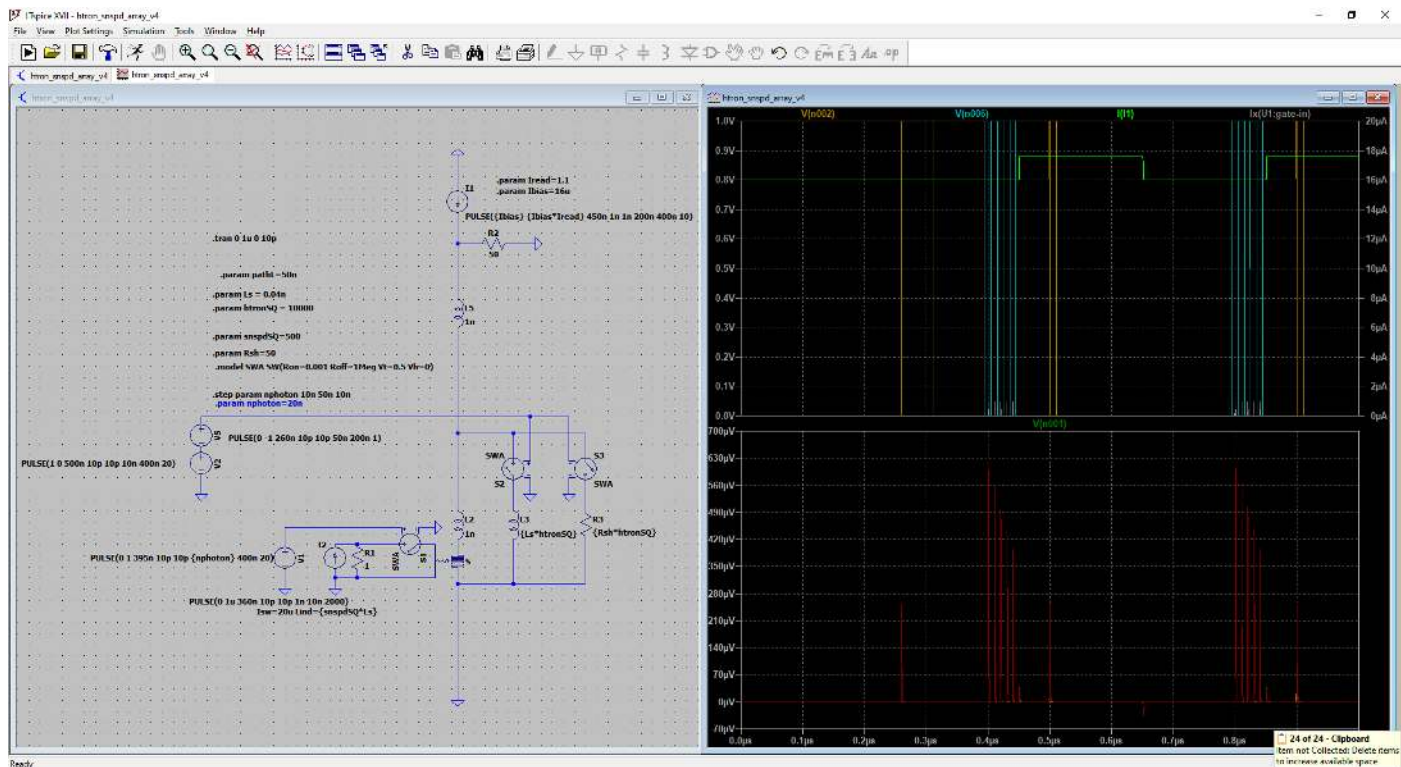
Two rows. Use nphoton to change number of incident photons. 10ns = 1photon. 20ns = 2photons

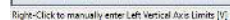


Two photon arrival on both rows. Sweeping the read bias. At $I_{read}=I_{bias}$ it still works. increasing I_{read} just produces ROs.
No PNR

In the plots above I was actually operating the SNSPD in a manner different from the sketch from Karl. I corrected the bias operation in the plot below. The top plot pane shows four traces. The green trace is the main column bias (C0 in Karl's drawing) which starts at 16uA and increases to 17.6uA at 450ns. 16uA is high enough for photodetection, switching current is 20uA. The tan trace is the row heater bias. When tan is high, the current flows through the inductor L3 (hTron superconducting), when tan is low the current flows through resistor R3 (hTron switched). Grey pulses are the snsdpd photon input and the cyan is a gating pulse used to create burst inputs.

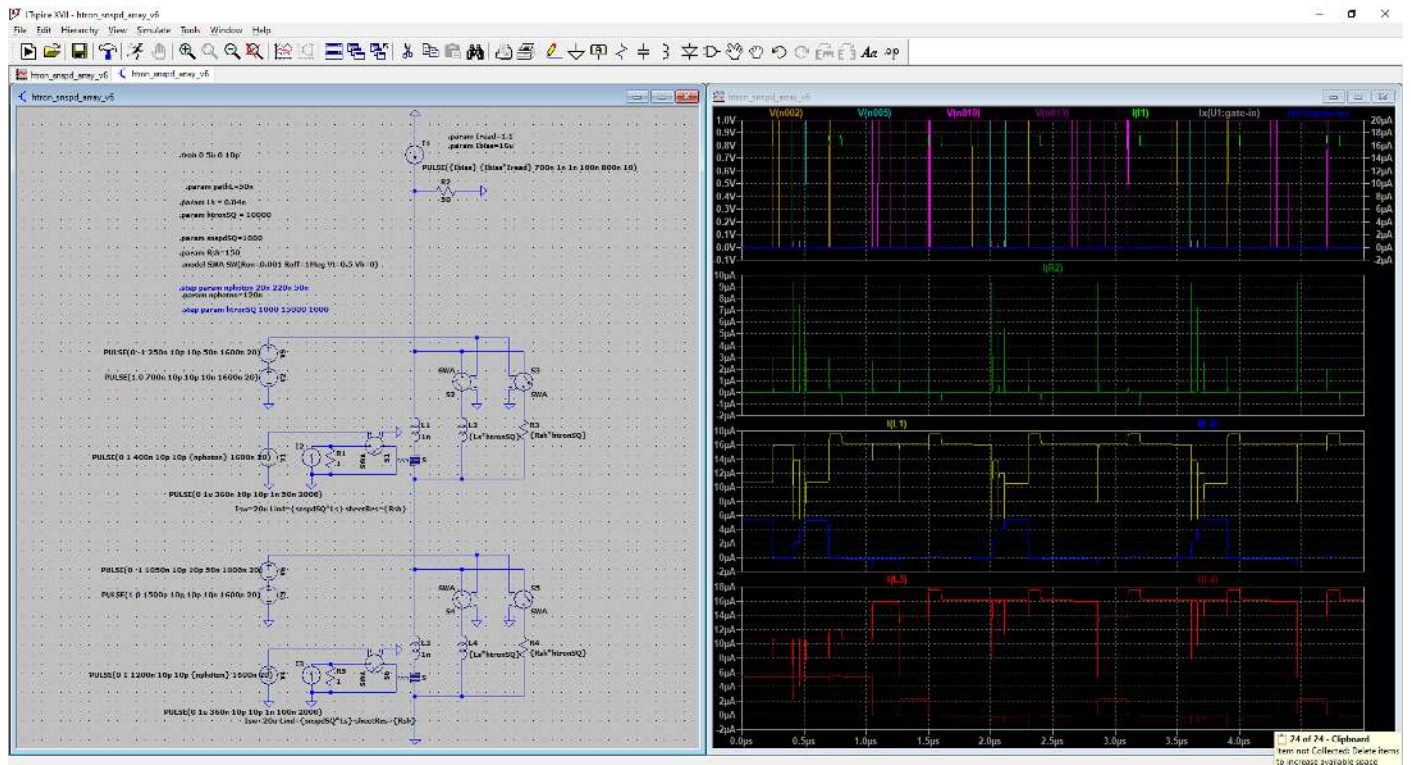
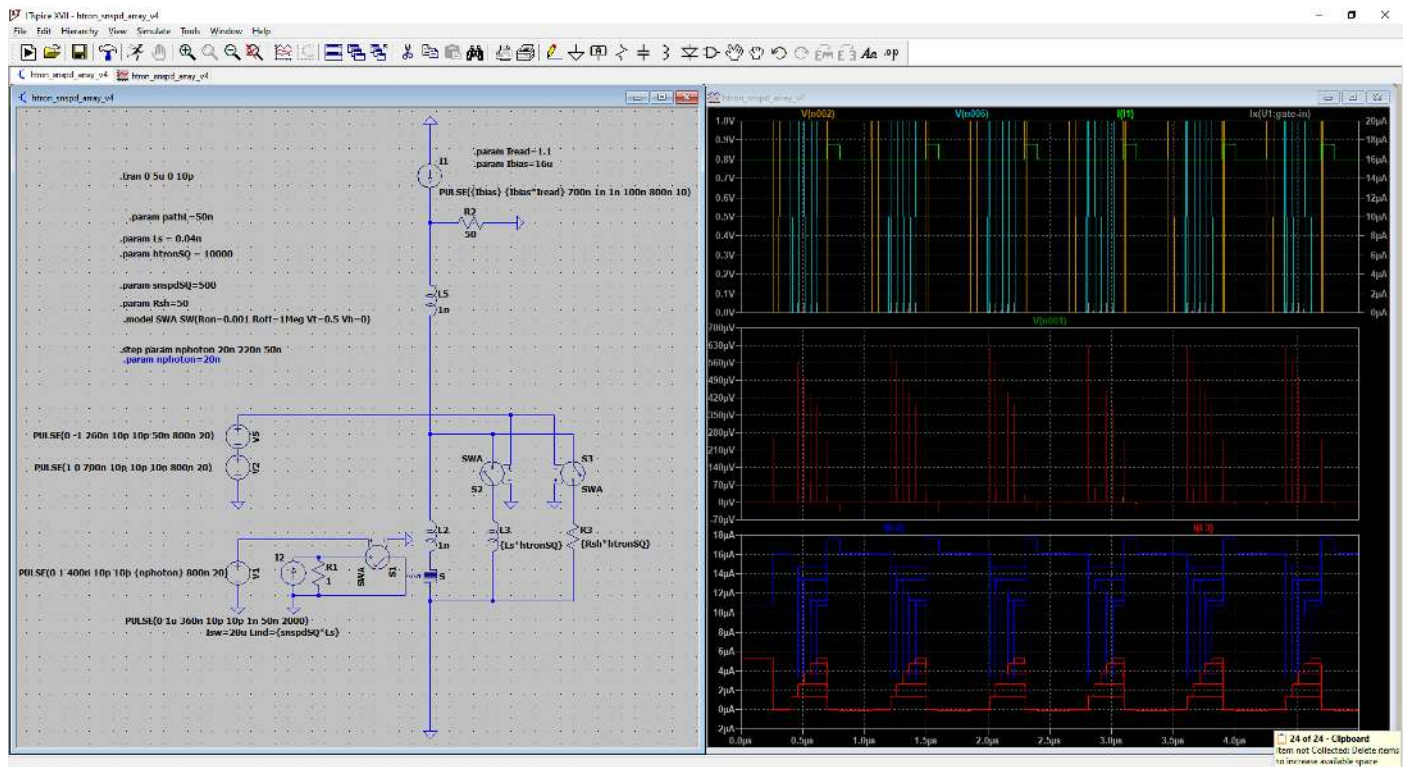
Operation recap: SNSPD is biased at $t=0$, current is split between the two inductors L2(snsdpd) and L3. Heater is turned on at 260ns and forces all current through the snsdpd. For the above parameters the current would remain in the hTron L3 after a photon arrival, preventing the snsdpd from detecting another pulse. Here the snsdpd is able to detect multiple pulses. The bias of the snsdpd is increased by 10% at 450ns and the heater is then turned on again as a read pulse. The amplitude of the output read pulse is dependent on the number of photon counts. See second figure.





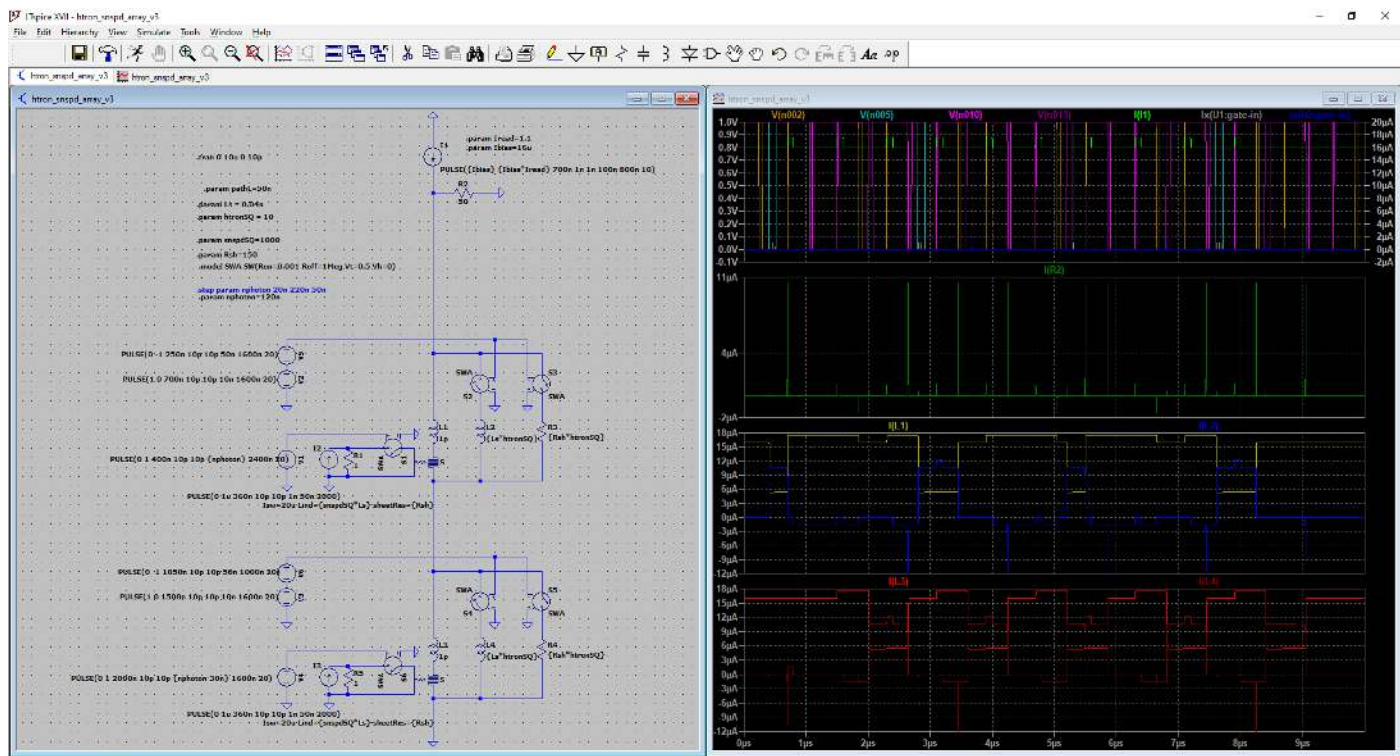
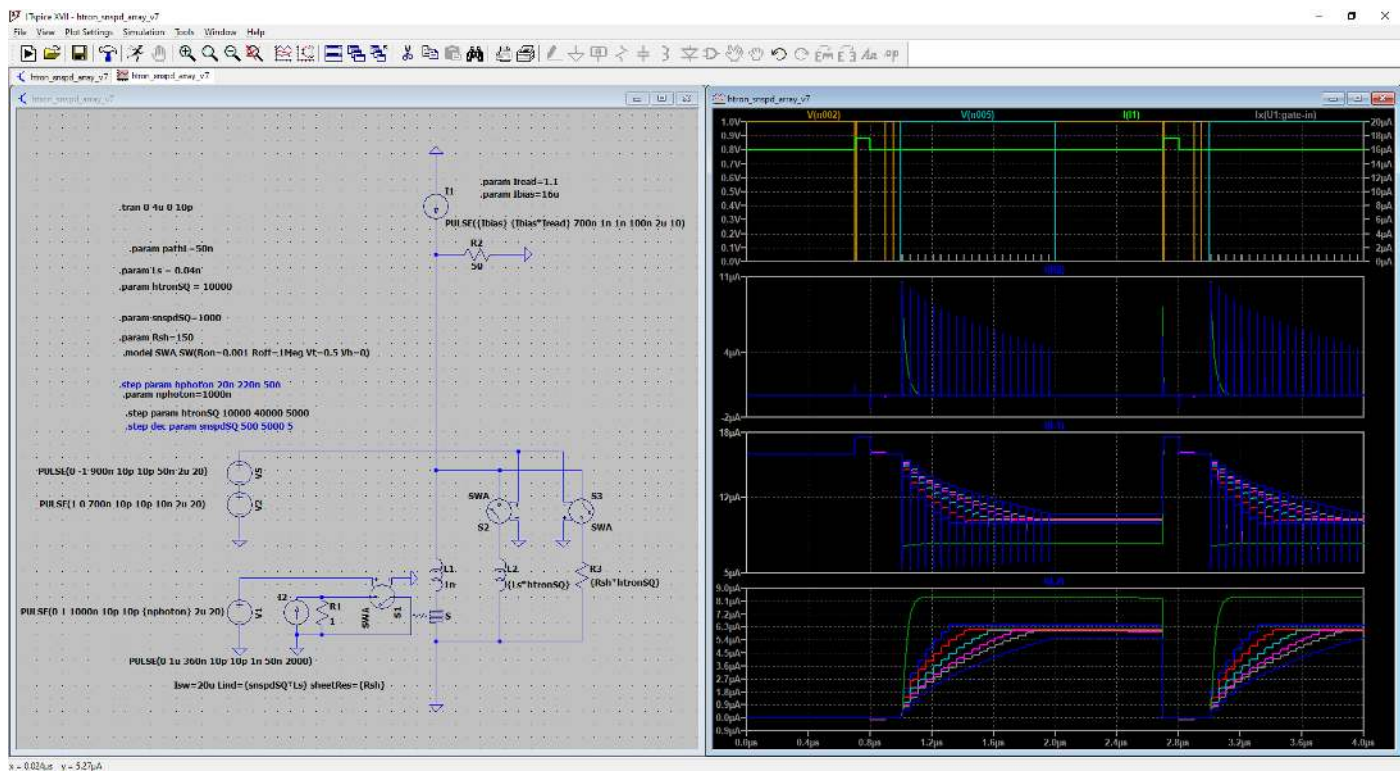
24 of 24 - Clipboard
Item not Collected: Delete items
to increase available space





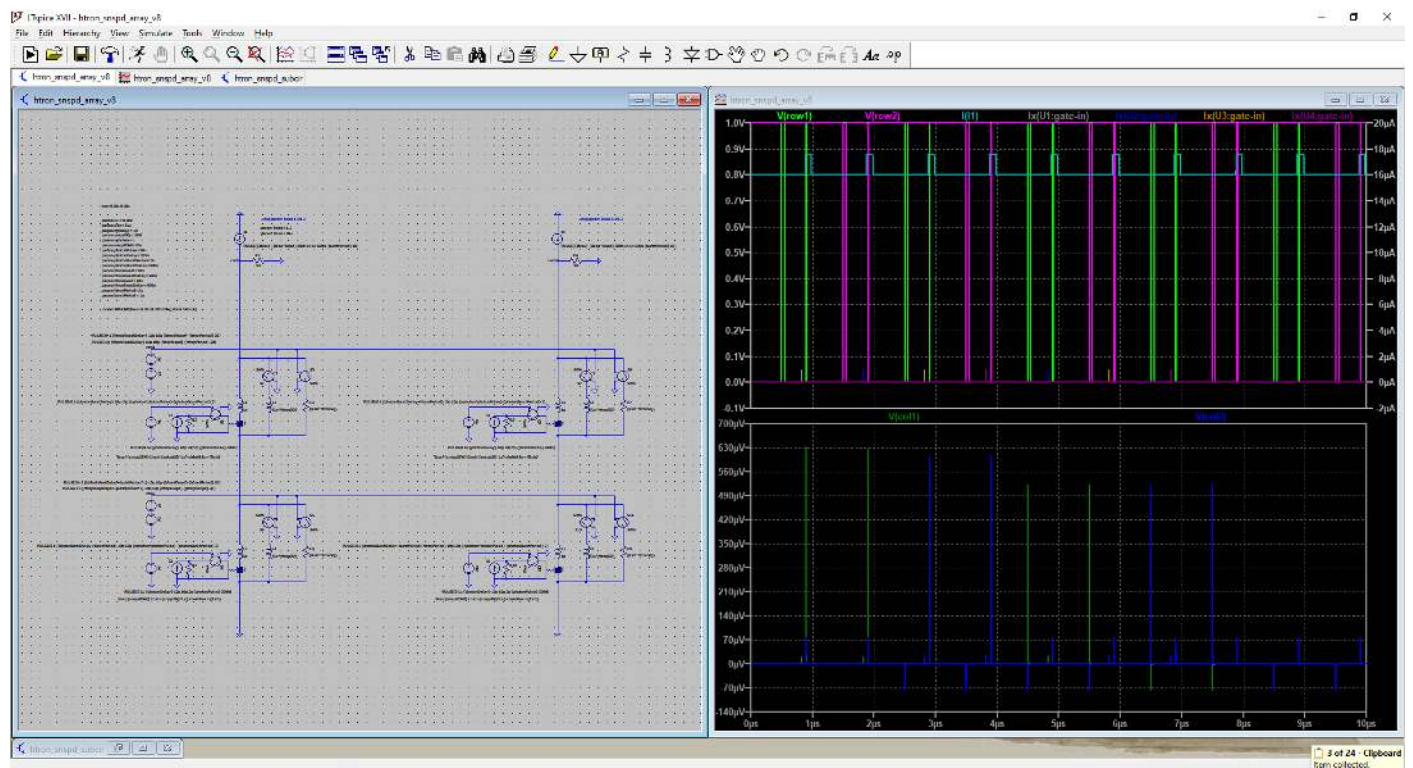
below shows two cells. The top cell received 3 photons, bottom received 2 photons, within the same time window. X shows the readout of the bottom, 2 photon cell, with a signal that is smaller than the O pulse for the 3 photon cell.







Files for the above plot: [htron_snsrd_array_v3.zip](#)

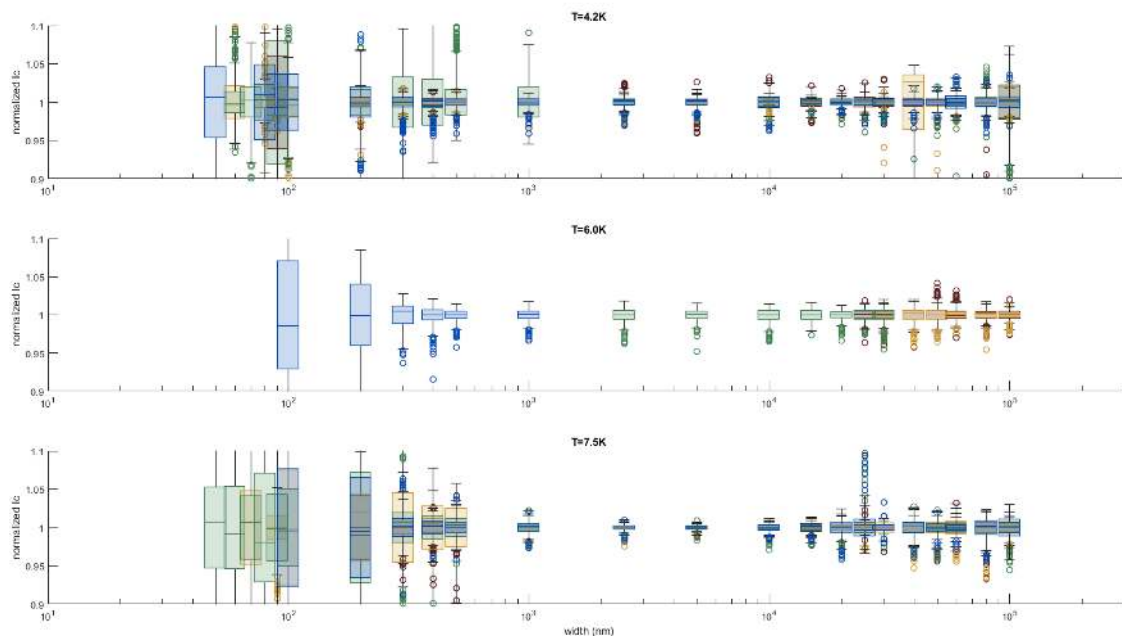
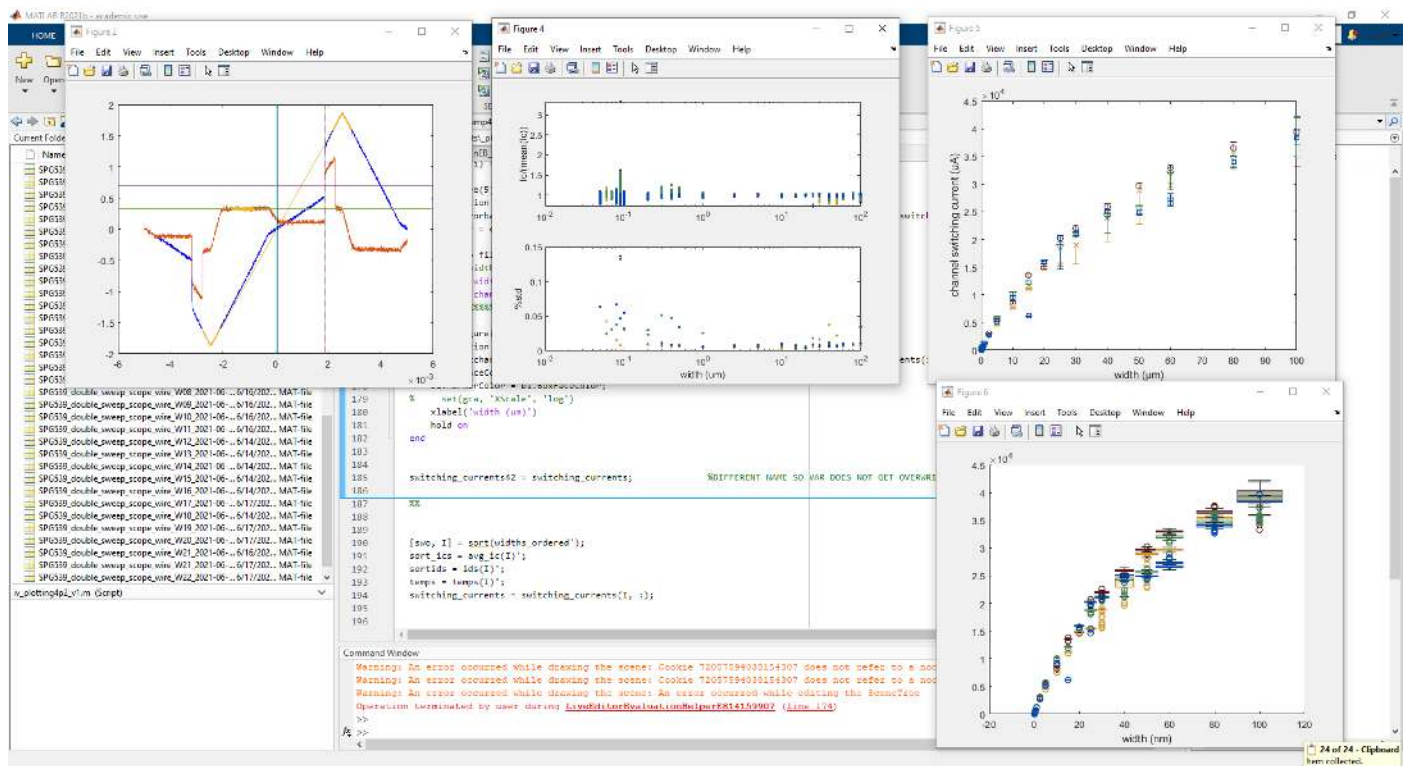


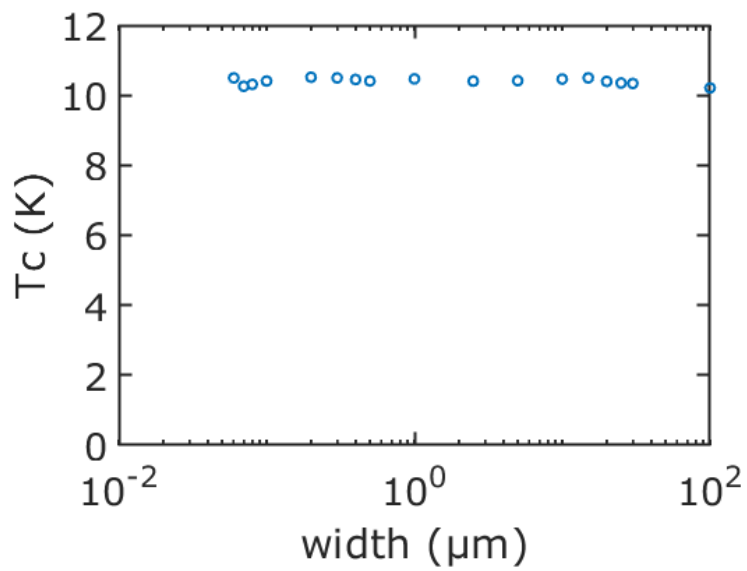
Pearl length 2022

February 8, 2022

Categories: Superconductivity

Revisiting the old data set. SPG539. Previous post <https://qnn.mit.edu/wordpress/archives/23134>





FPGA selection for nanowire electronics

March 2, 2022

Categories: FPGA, General

Current setup

Digitizer: WAVERUNNER 610ZI LeCroy Digital Oscilloscope – 1GHz bandwidth, 10GSPS

AWG: Keysight 33600a – 80 MHz models: 1 μ SPS to 660 MSPS, 1- μ SPS resolution 8

<https://docs.xilinx.com/v/u/en-US/ds890-ultrascale-overview>

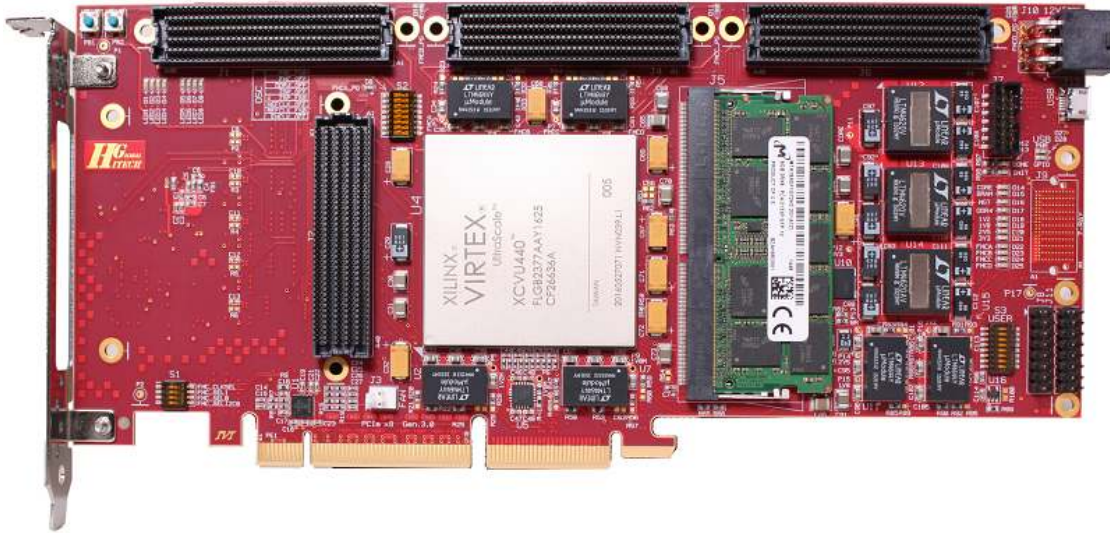
<https://www.spincore.com/products/PulseBlaster/>

Hitech Global

http://www.hitechglobal.com/Accessories/FMC_Modules.htm

<http://www.hitechglobal.com/Boards/Virtex-UltraScale-SOC.htm> — \$23k

4 FMC PORTS – limit on total number of ADC/DAC cards. MAX 8 in 8 out



http://www.hitechglobal.com/FMCMODULES/FMC_AD9082_AD9081.htm — \$7.5k (RF-ADC/DAC not what we want)

http://www.hitechglobal.com/FMCMODULES/16-bitDAC_14-bitADC.htm

<https://www.xilinx.com/products/boards-and-kits/fmc-cards.html>

VadaTech

AMC589 Quad ADC @ 3 GSPS with Quad DAC @ 12 GSPS, UltraScale+™, AMC

<https://www.vadatech.com/product.php?product=538>

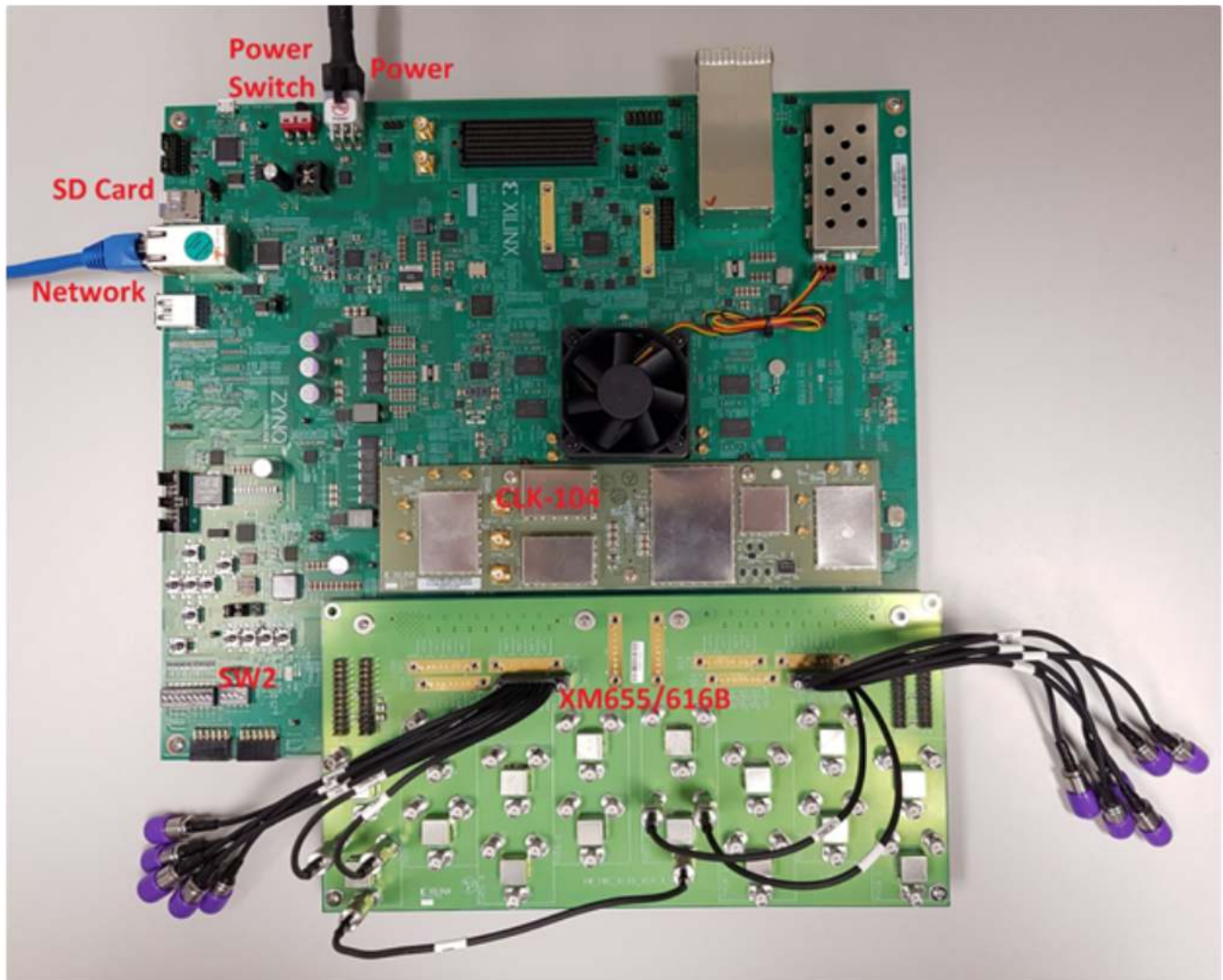
<https://www.vadatech.com/product.php?product=538>

Xilinx – \$14k (14-bit, 2.5GSPS RF-ADC (qty 16), 14-bit, 9.85GSPS RF-DAC (qty 16))

I thought this would be the best option until I saw they have RF-ADC/DAC

<https://www.xilinx.com/products/boards-and-kits/zcu216.html#whatsInside>

<https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/769228974/XM650+XM655+and+CLK104+Add-On+Cards+Hardware+Description>



Keysight – \$65k

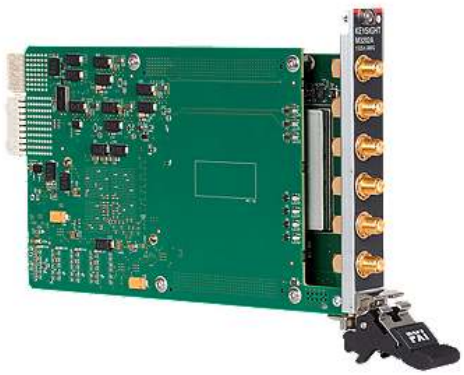
[2443910-1.pdf](#)

Max channels in 10U chassis 16/16.

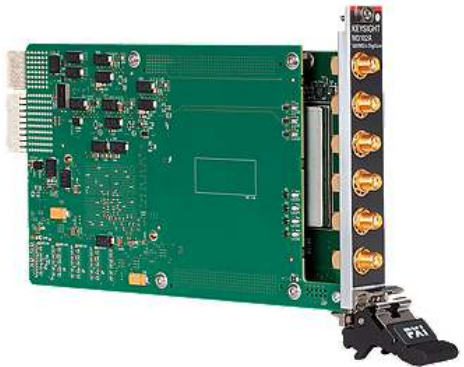
multiple chassis can be connected.

Average nMem waveform length 300ns and 1ns resolution. For onboard memory of 1GS we can store 3e6 waveforms.

AWG: (4ch) PXIe Arbitrary Waveform Generator: 1GSPS, 14 bits — \$22k



Digitizer: (4ch) PXIe Digitizer: 500 MSPS, 14 bits — \$21k



Chassis: PXIe Chassis: 10-slot, 3U, 24GB/s — \$6k



Controller: PXIe Embedded Controller: Intel i7, 4 GB RAM, 240 GB SSD — \$8.5k



Link to external PC: PXIe High Performance System Module: Dual Port (x16) Gen 3 + PCIe Host Adapter: Single Port (x8), Gen 3 — \$4k



FPGA Software: KF9000B PathWave FPGA — \$3k

National Instruments ~\$40k (much lower performance)

PXI Advisor – National Instruments.pdf

Annapolis Micro

<https://www.annapmicro.com/product-category/mezzanine-boards/>

<https://www.annapmicro.com/product-category/wild40-ecosystem-openvpx-6u/>

| *WILD FMC+ QM30 ADC & DAC – WWQM30*

FPGA Boards – 6U — *WILDSTAR UltrakVP 2PE for 6U OpenVPX – WB6XU2*



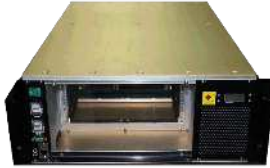
[annapolis_wsultrakvp_2pe_6u_marketdata_15501_rev1.9.pdf](#)

FMC CARD (8 ADC, 4 DAC) — *WILD FMC+ QM61 ADC & DAC – WWQM61*



[annapolis_WWQM61_marketdata_18329_rev1.1.pdf](#)

4 SLOT CHASSIS – [WILD40 4-Slot 6U OpenVPX Chassis](#)



[annapolis_Wild40OpenVPXEcoSystemChassis_marketdata_15250_rev1.8.pdf](#)

Some contact

Bob Kirk, Chief Sales Officer

T: 410-841-2514

C: 214-364-7723

bkirk@annapmicro.com

Sales Regions

US Capital Region

(Includes DC, MD & VA)

John Ludicke, Director of Business Development, Mid-Atlantic

T: 410-841-2514

F: 410-841-2518

john.ludicke@annapmicro.com

US Western Region & Western Canada

(Includes AZ, CA, CO, ID, MT, ND, NM, NV, OR, SD, UT, WA, WY & Western Canada)

Dale Stevenson, Director of Sales Development, Western

T: 831-630-9121

dale.stevenson@annapmicro.com

US Southeast Region

(Includes AL, FL, GA, MS, NC, SC & TN)

Cole Crosby, Account Manager, Southeast

T: 601-543-3239

cole.crosby@annapmicro.com

US Central Region & International

(Includes AK, AR, DE, HI, IL, IN, IA, KY, KS, LA, MI, MN, MO, NE, NJ, OH, OK, PA, PR, TX, WI, WV & International)

Bob Kirk, Chief Sales Officer

T: 410-841-2514

C: 410-507-1894

bkirk@annapmicro.com

US Northeast Region & Eastern Canada

(Includes CT, MA, ME, NH, NY, RI, VT & Eastern Canada)

David King, Director, Northeast

T: 978-660-8057

david.king@annapmicro.com

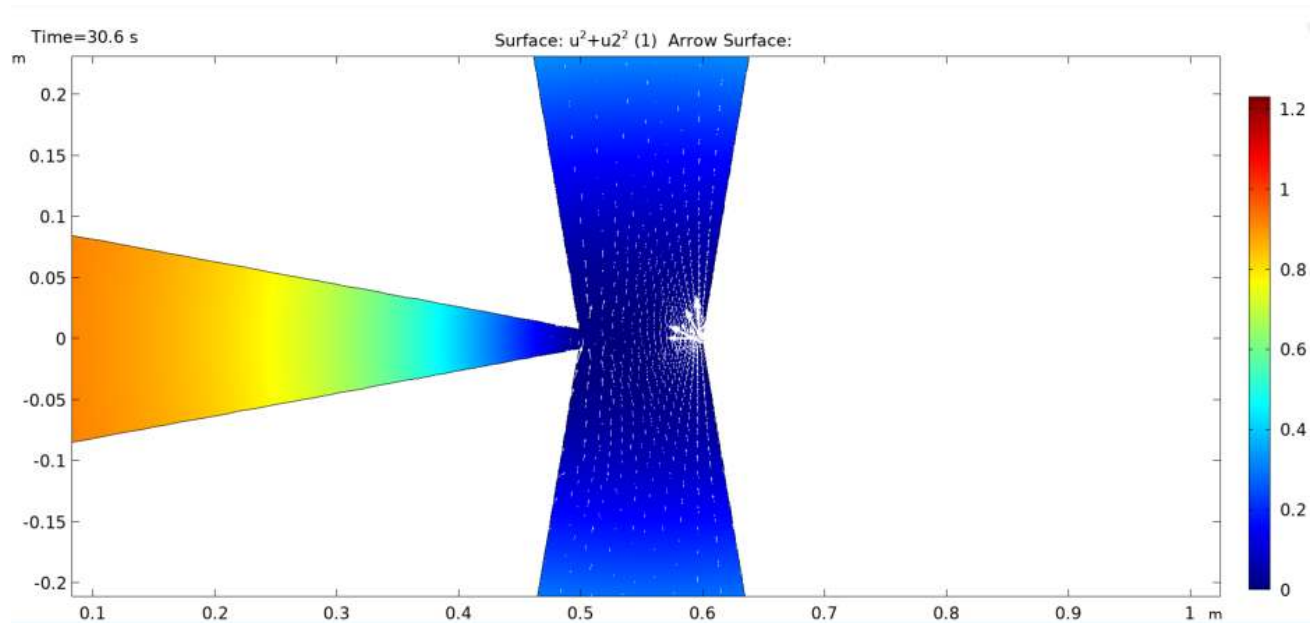
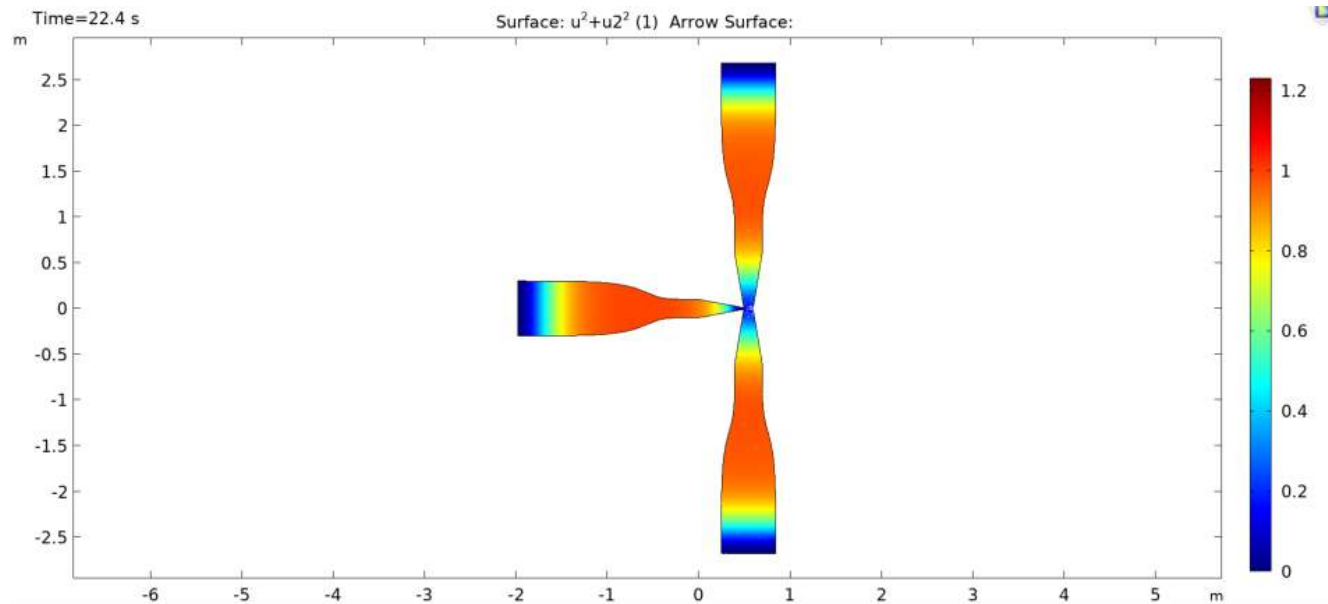
TDGL simulation in Comsol

May 7, 2022

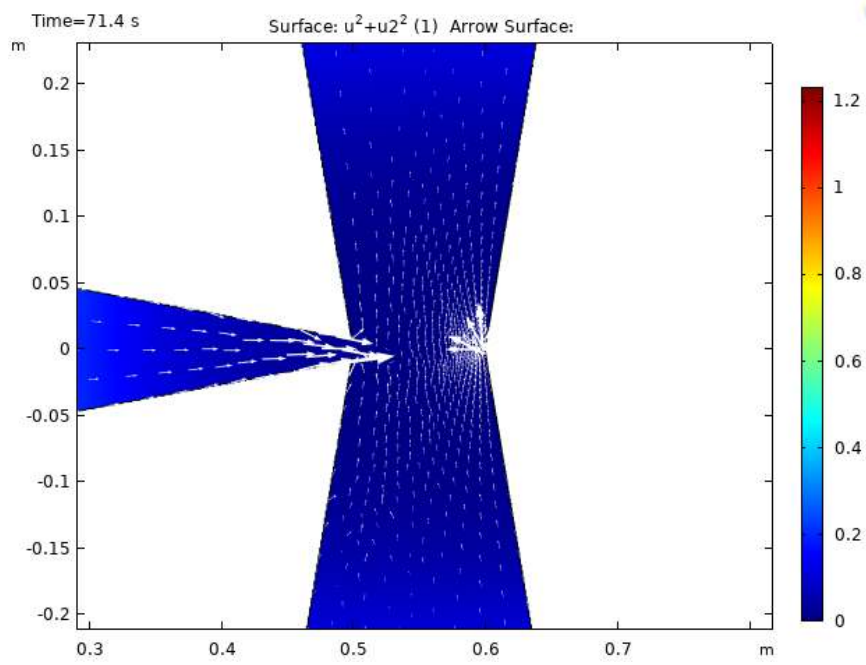
Categories: Comsol, Electronics, nTron, Simulation, Superconductivity, TDGL

Modeled using the general form PDE. 5 coupled PDEs: RealPsi, ImagPsi, VecPotX, VecPotY, GradA.normBoundary=0.

Cooper pair density is equal to $u^2 + u2^2$. Below is an nTron with normal metal leads, which makes Psi go to zero at the edges. In the center of the channel Psi is suppressed.



Here we apply a current to the gate.

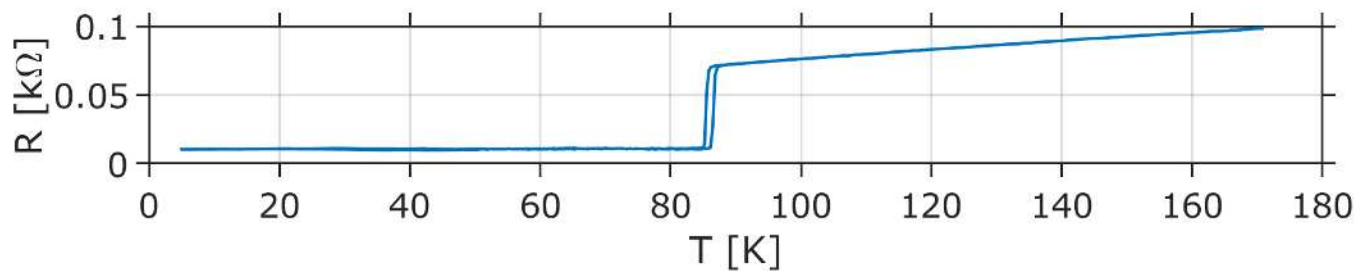
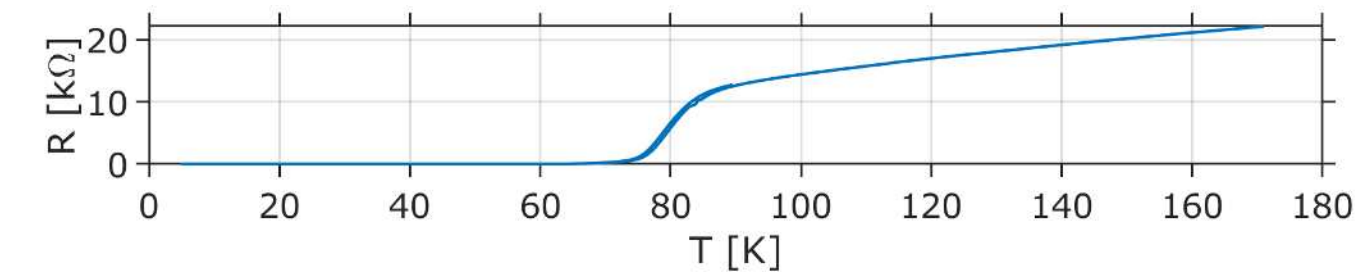


YBCO wires

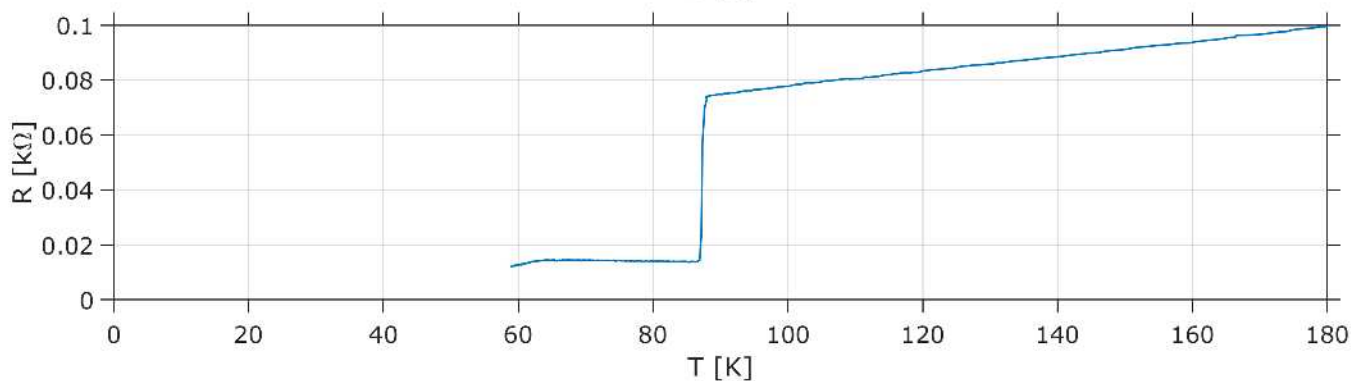
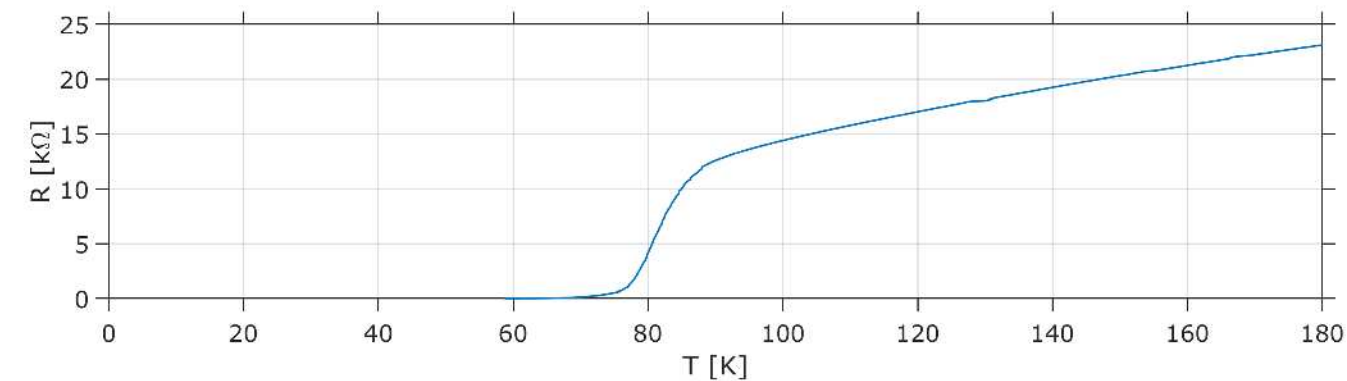
May 23, 2022

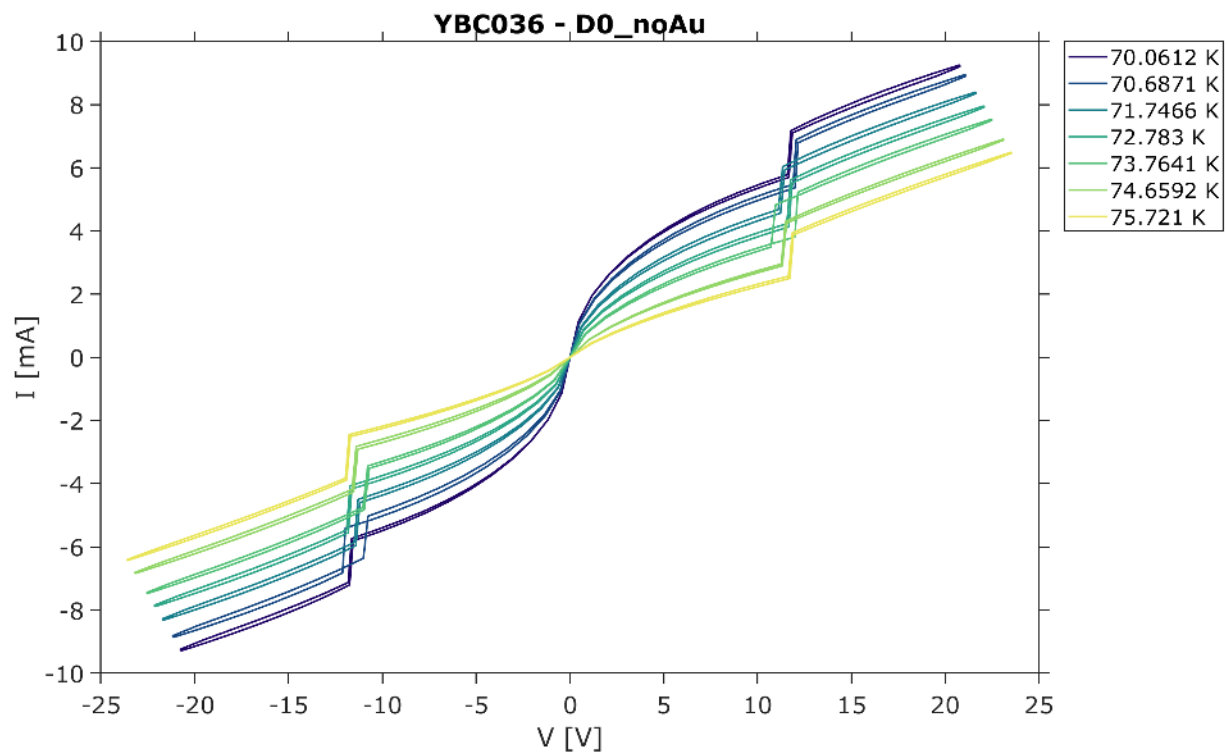
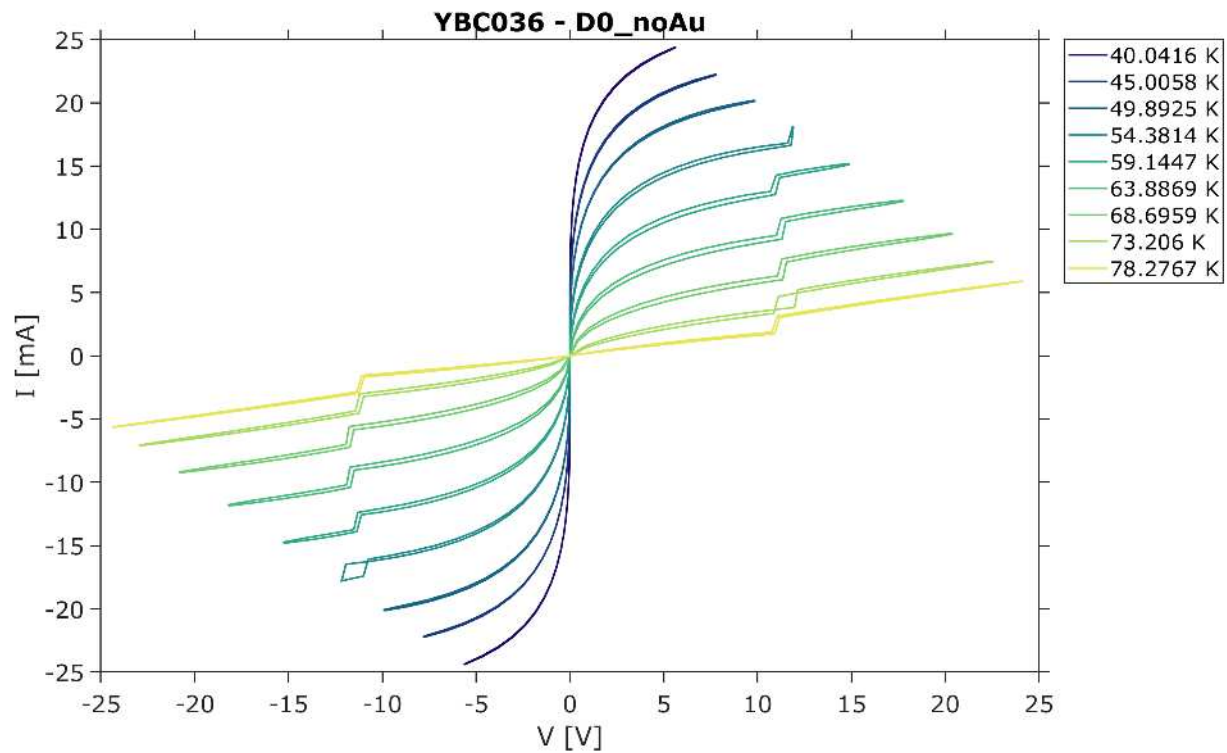
Categories: General

T_c of D0 devices. Top is unshunted, bottom is shunted



NEXT DAY



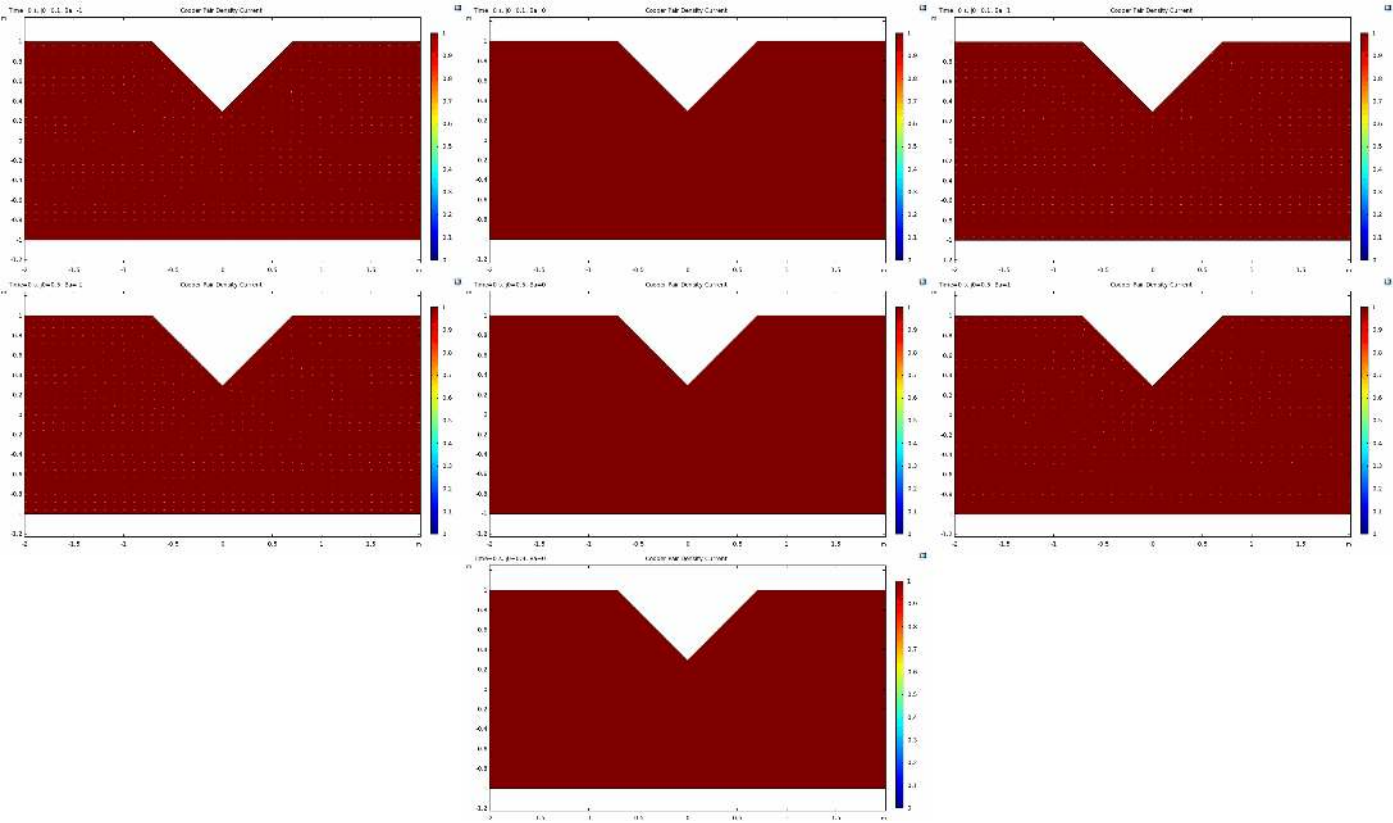


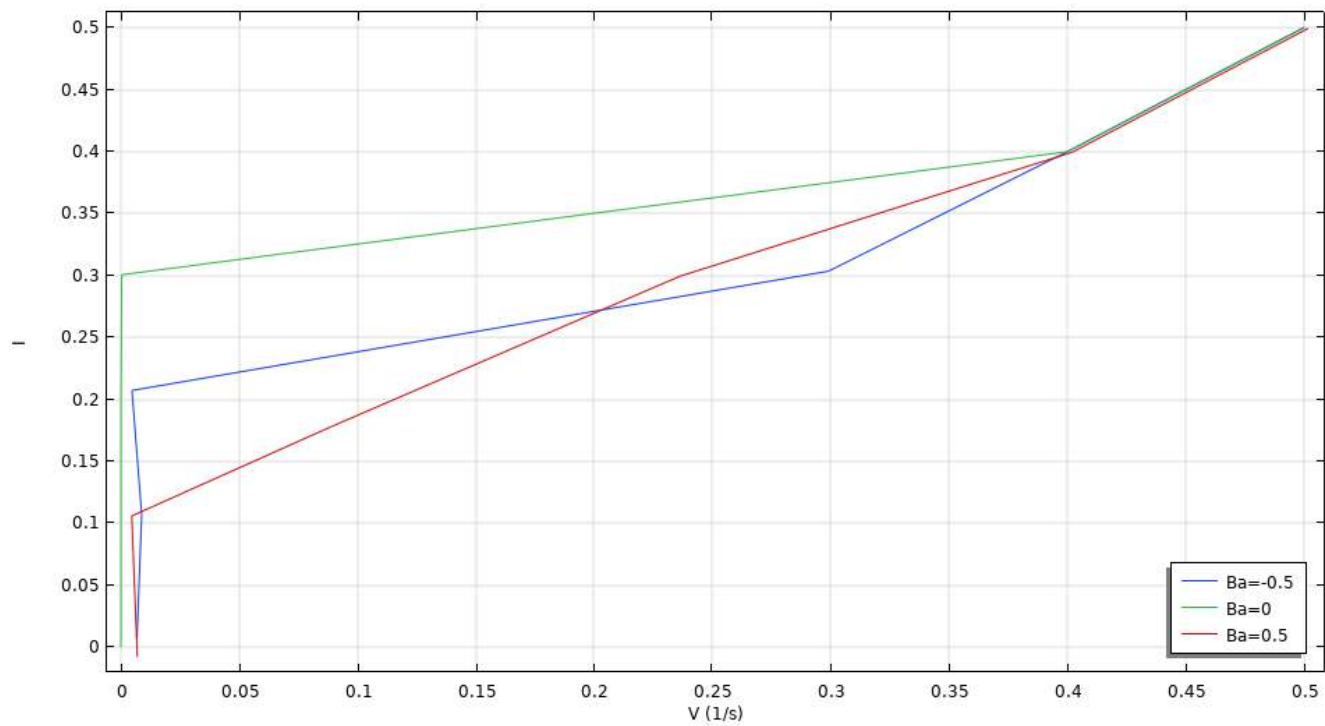
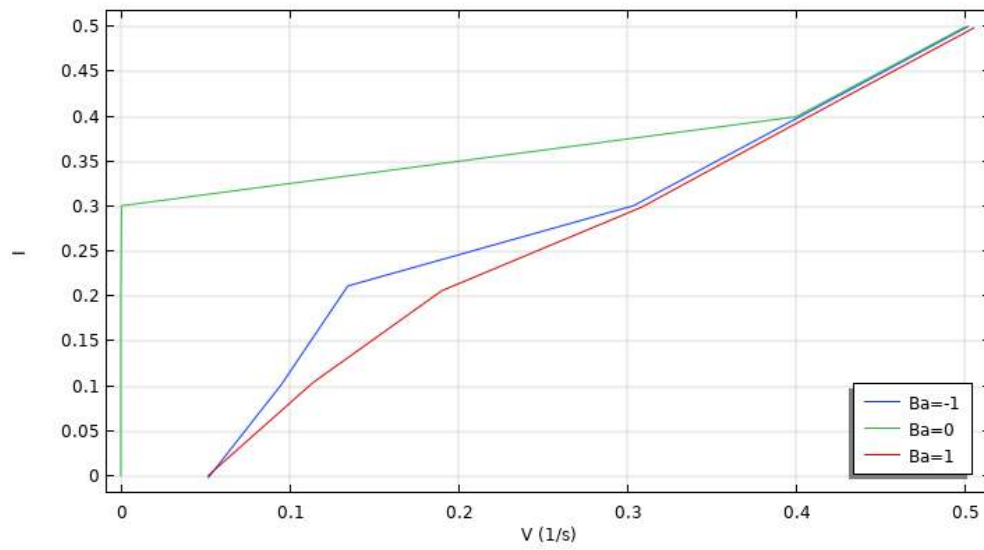
uwire2.gds

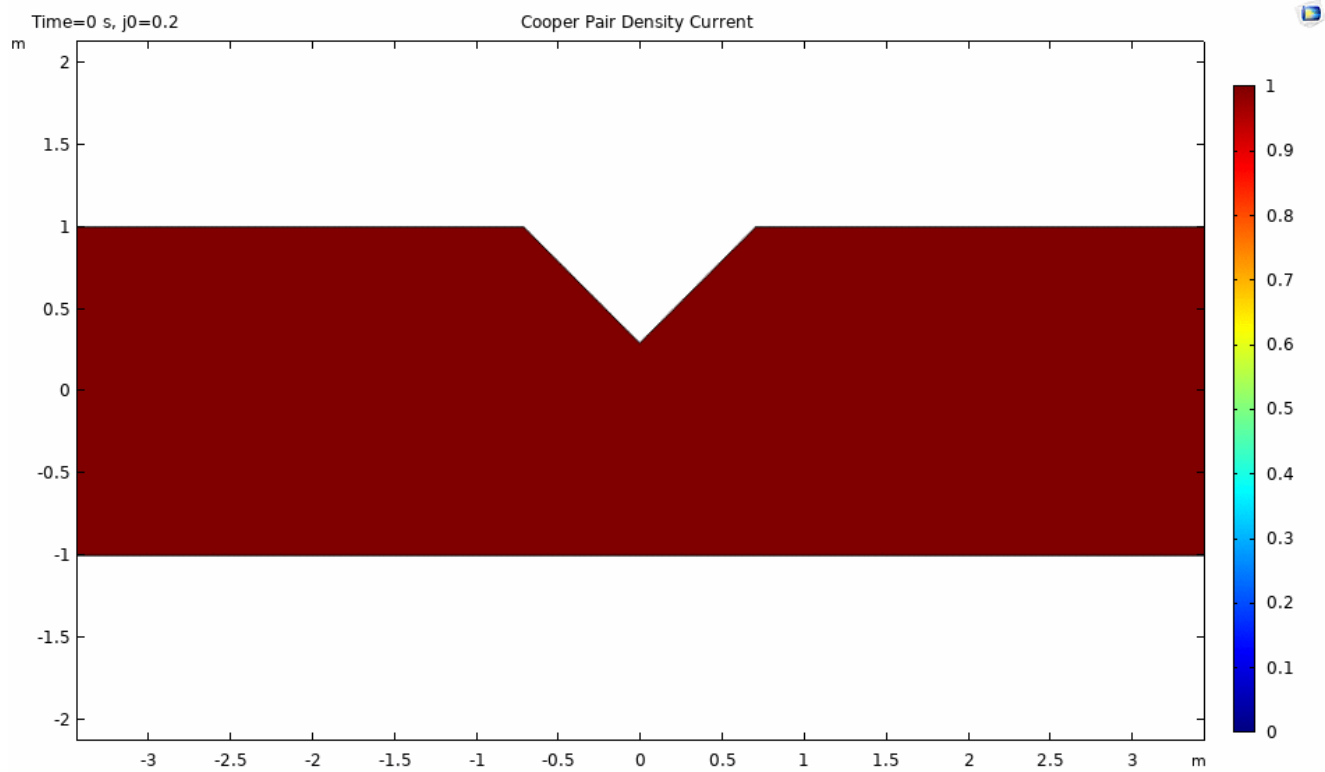
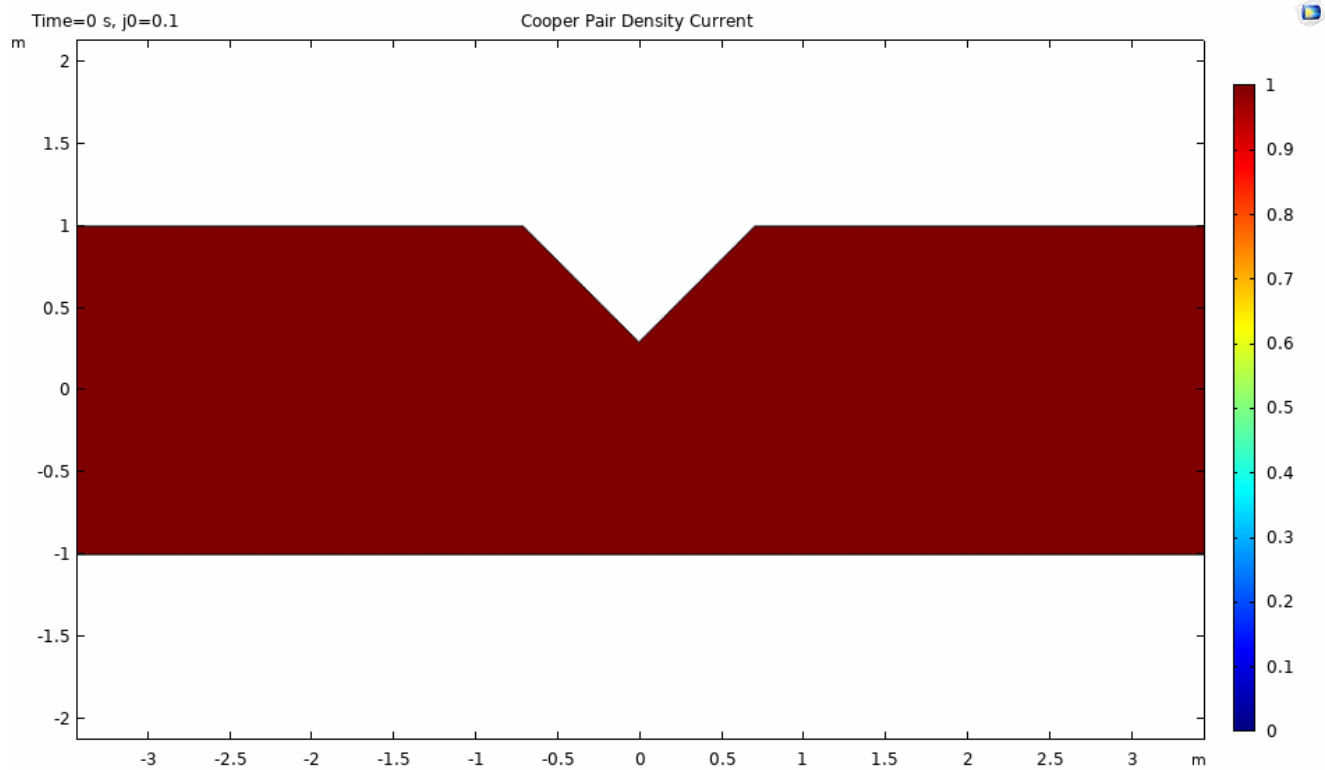
comsol diode TDGL

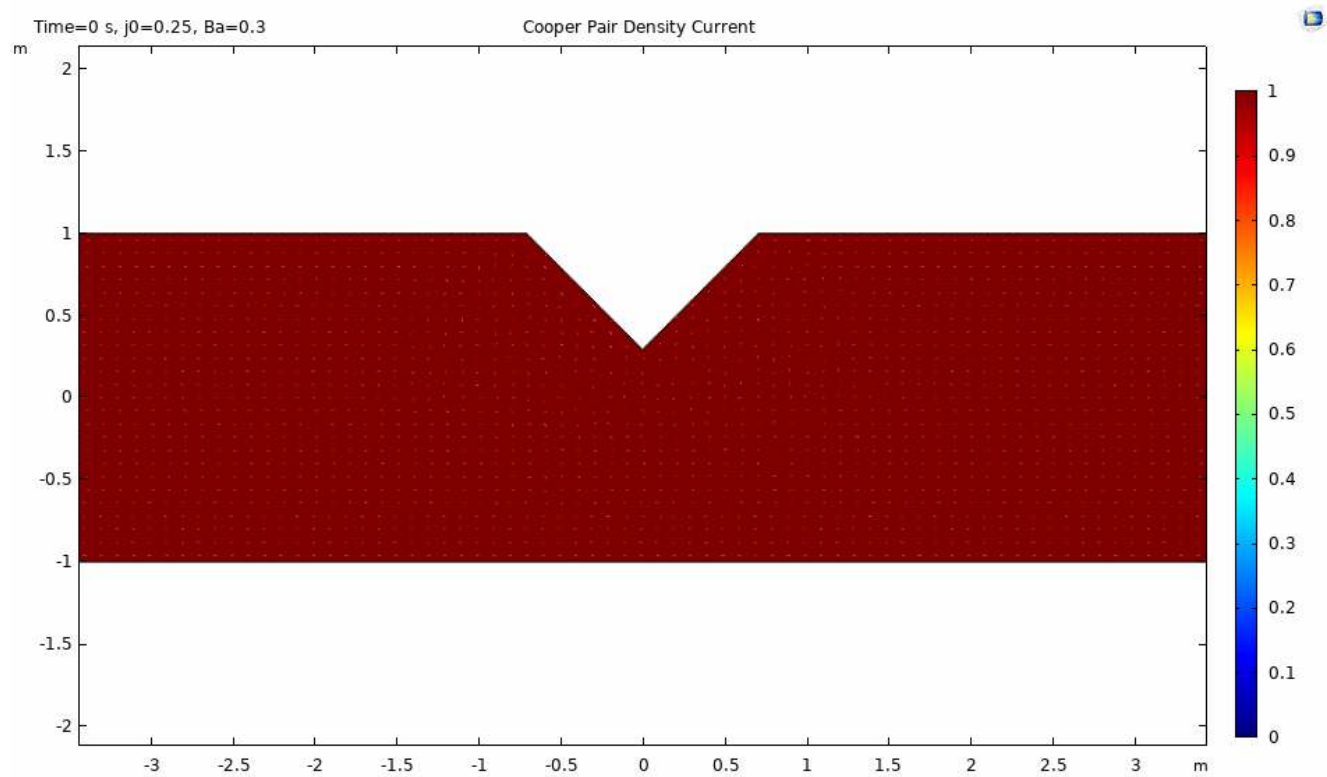
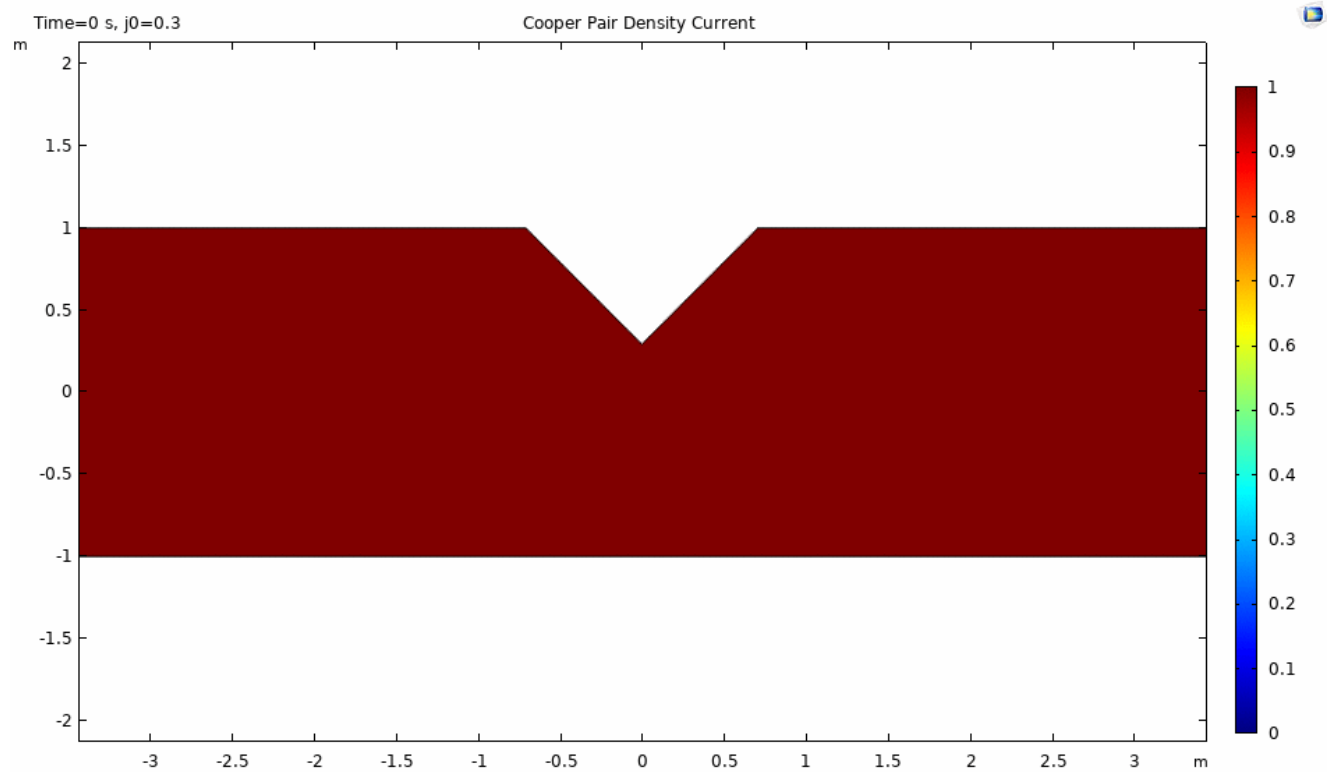
June 15, 2022

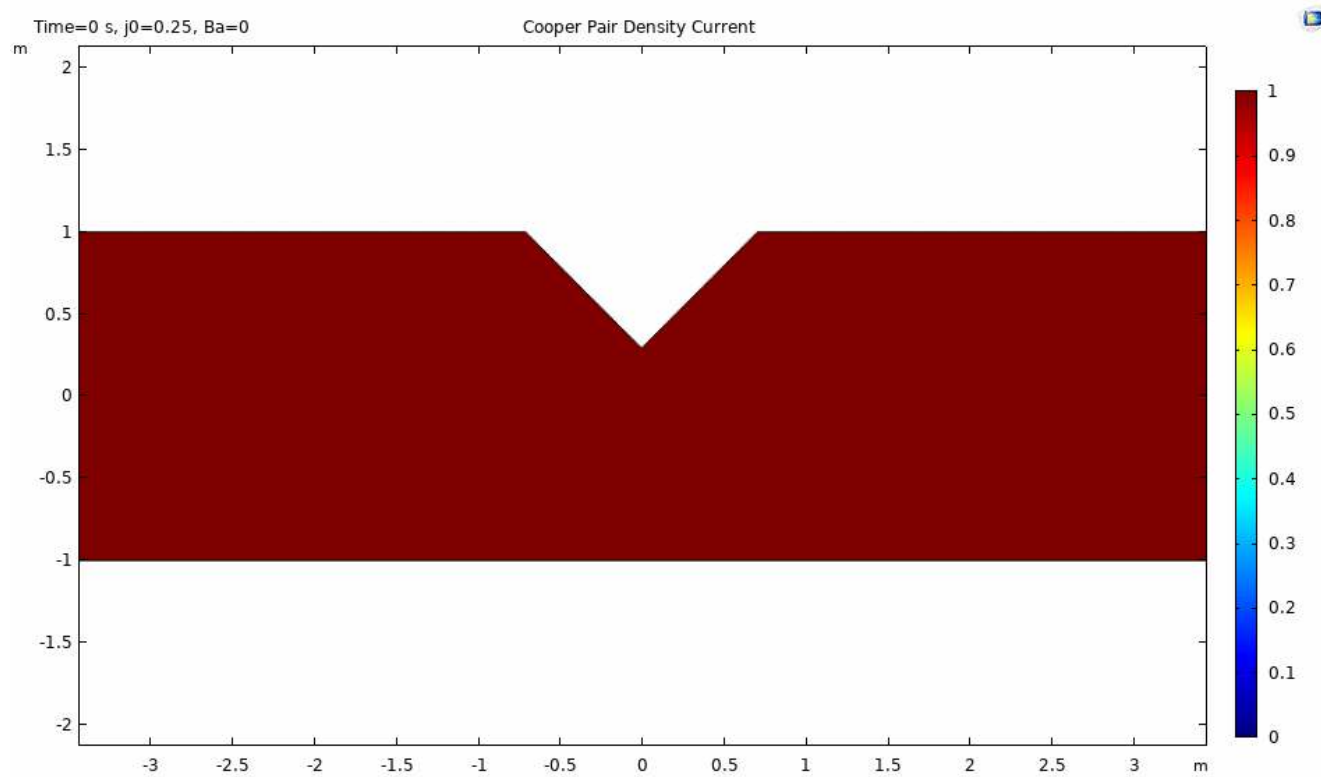
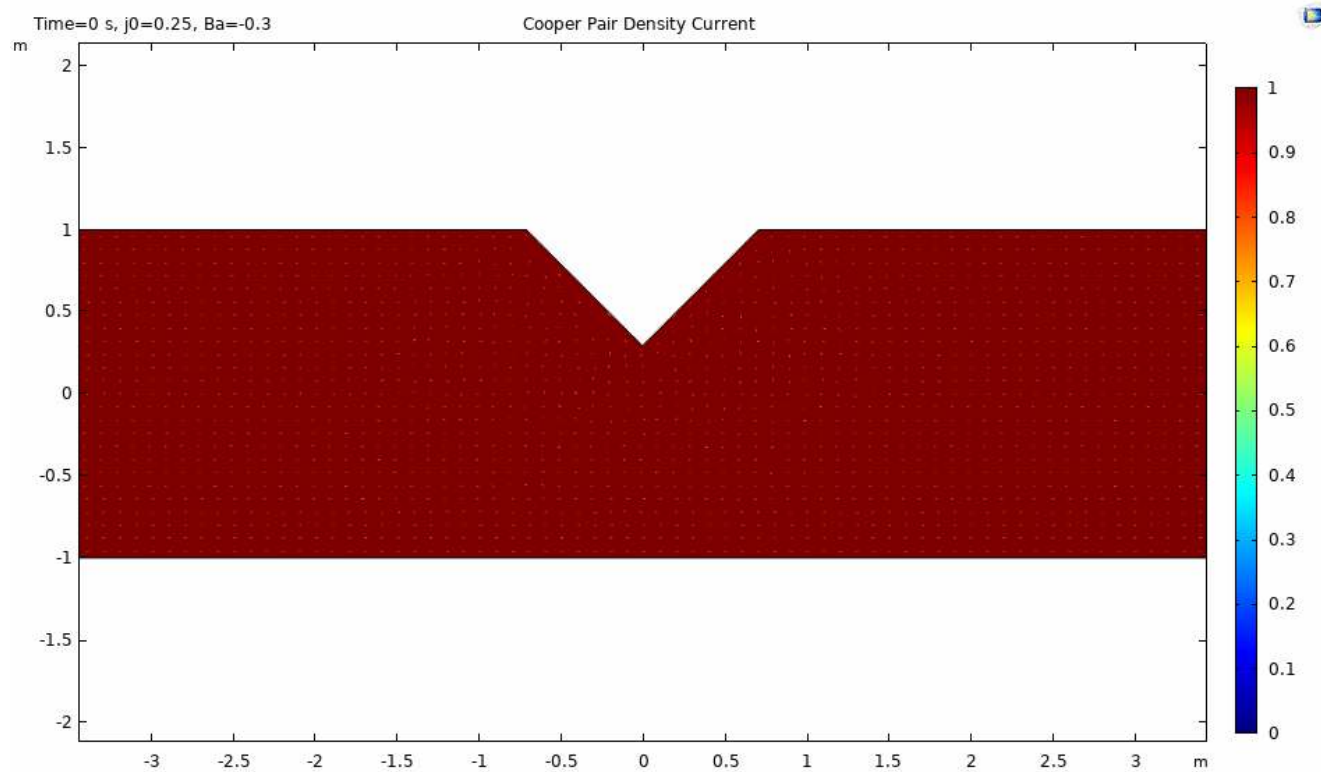
Categories: Comsol, Electronics, nTron, Simulation, TDGL

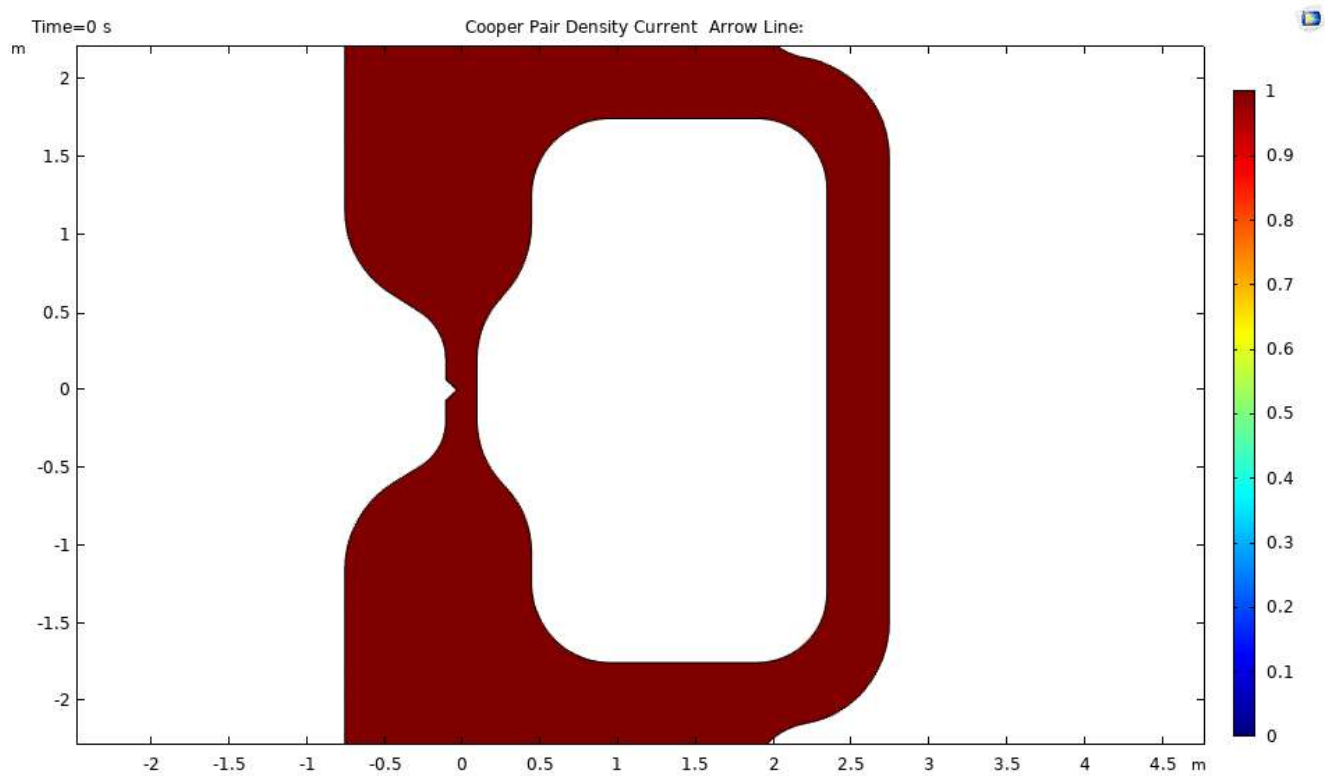
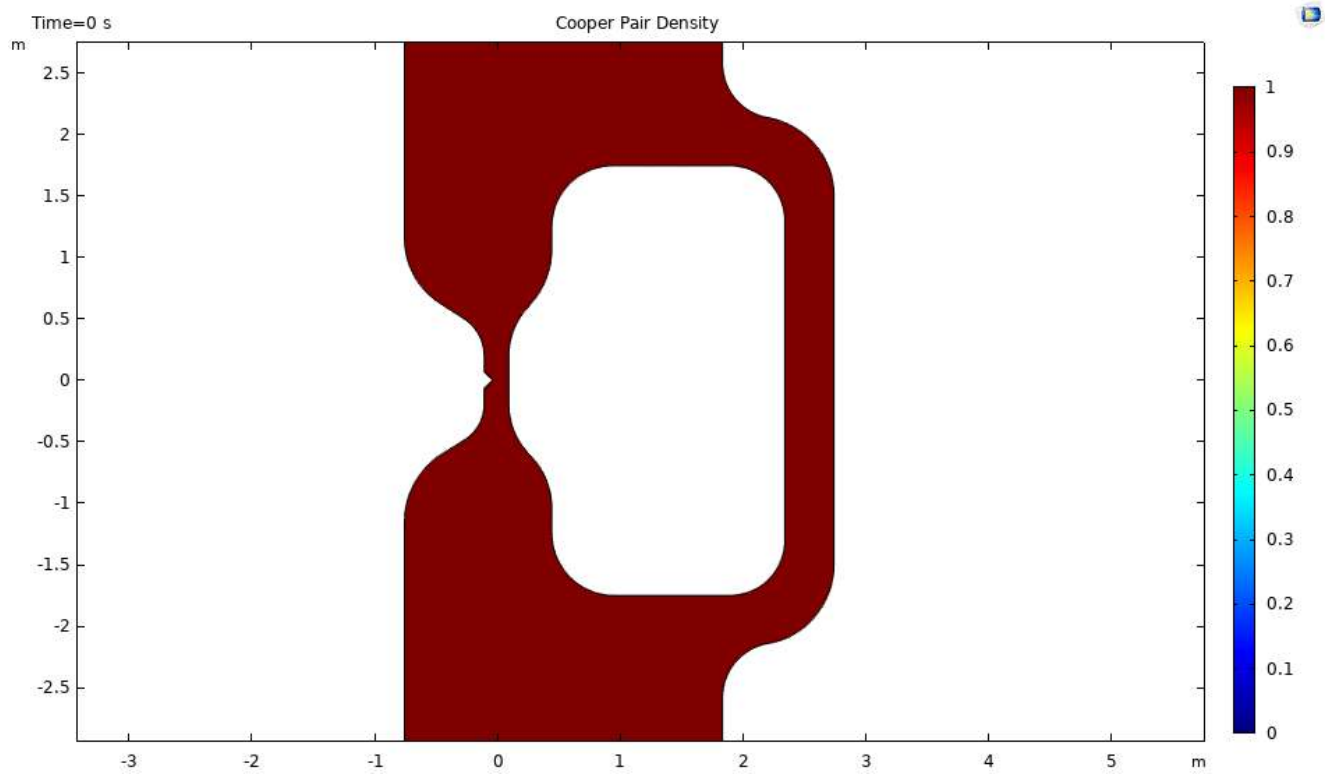


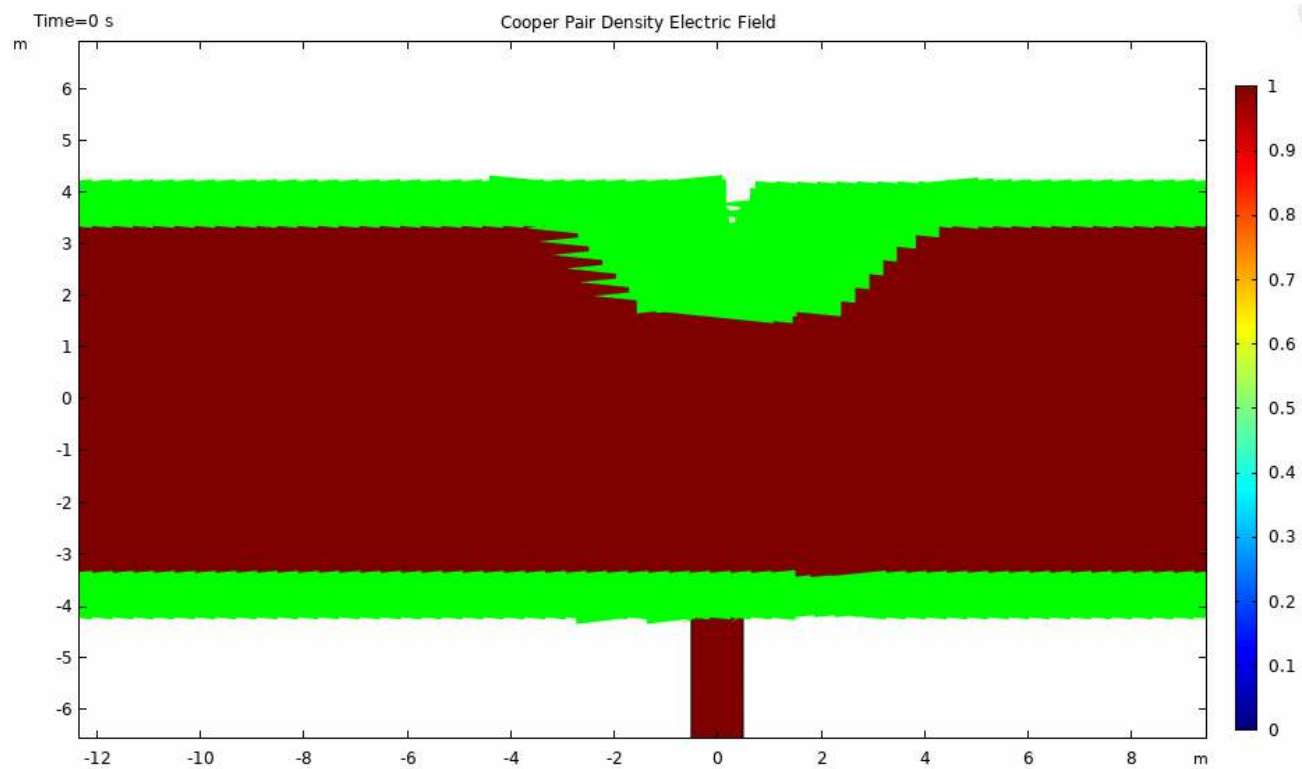
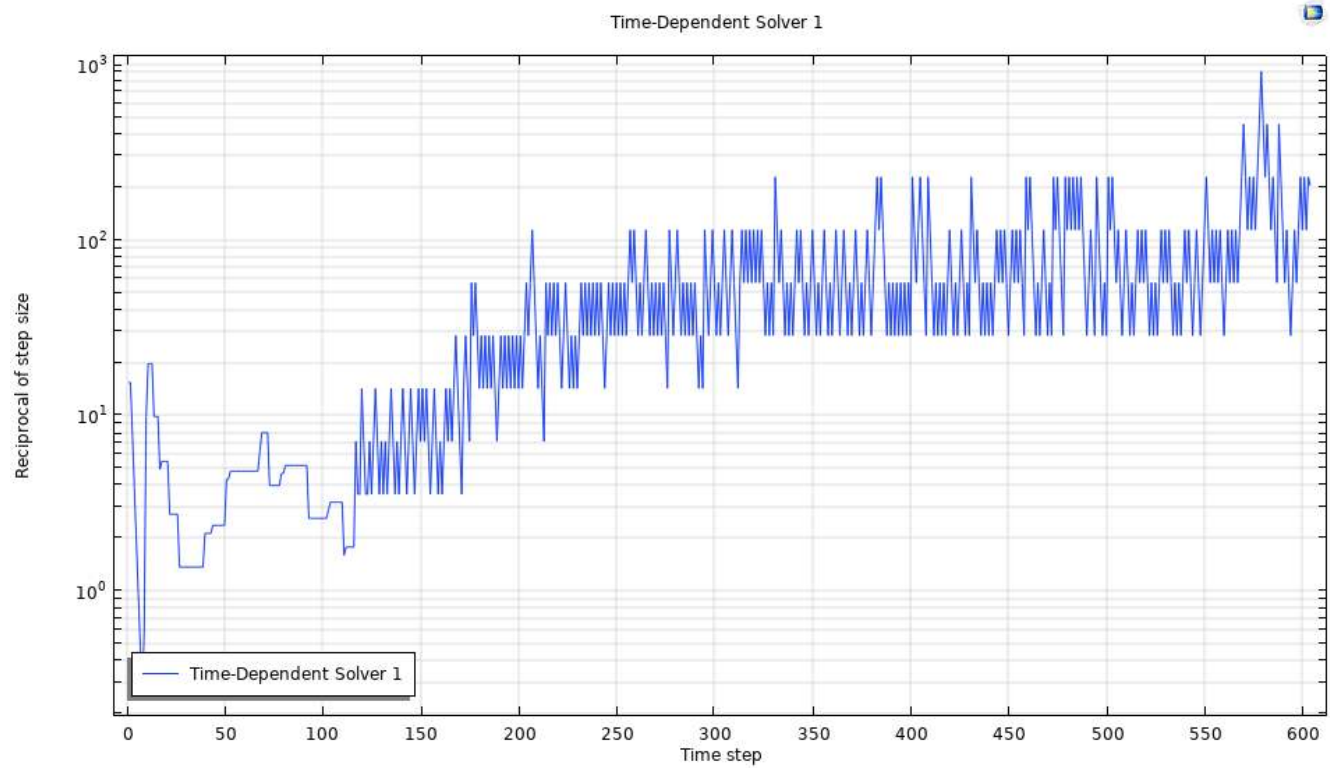












Free Space Cryo Upgrade cont

June 27, 2022

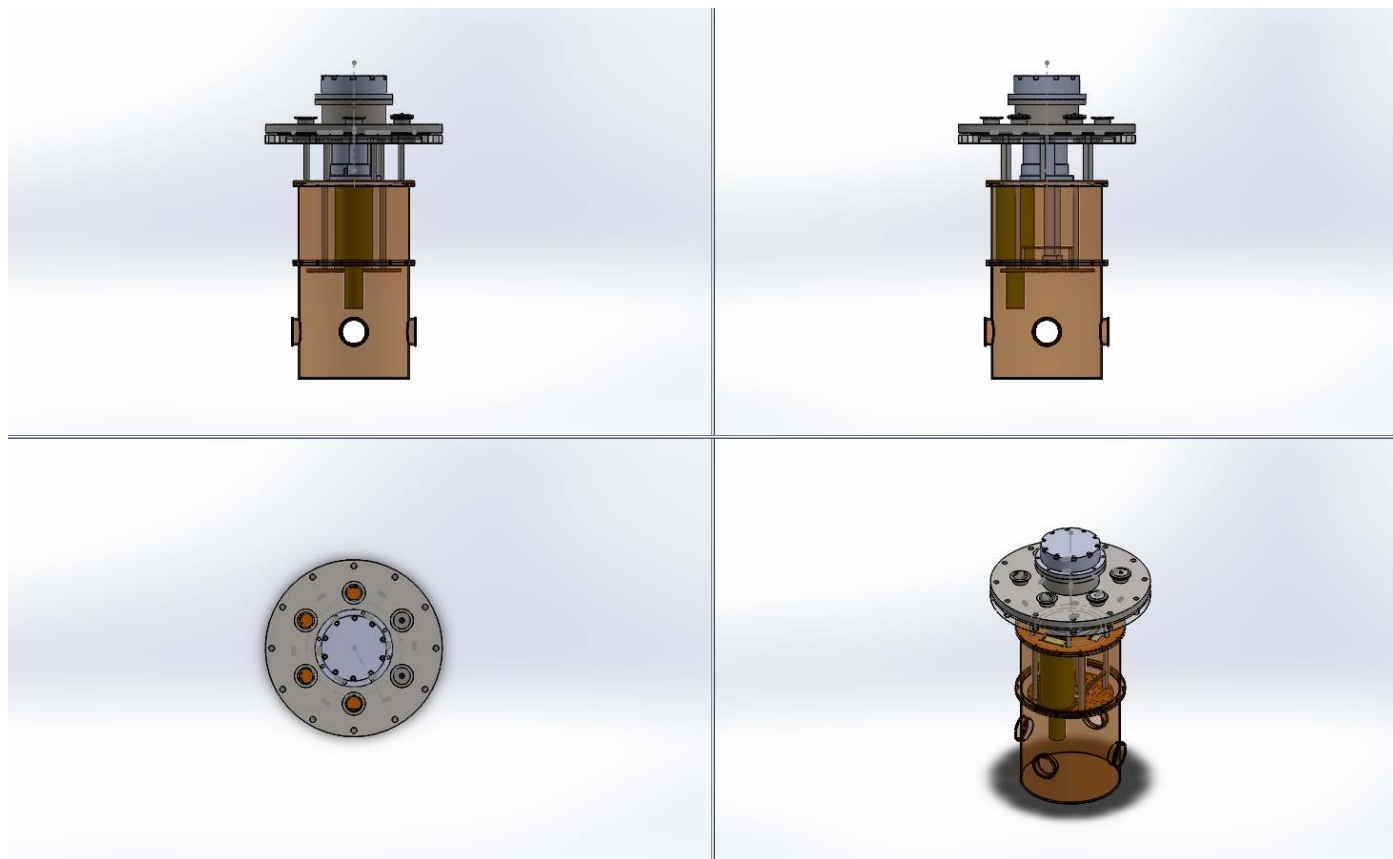
Categories: Cryostat

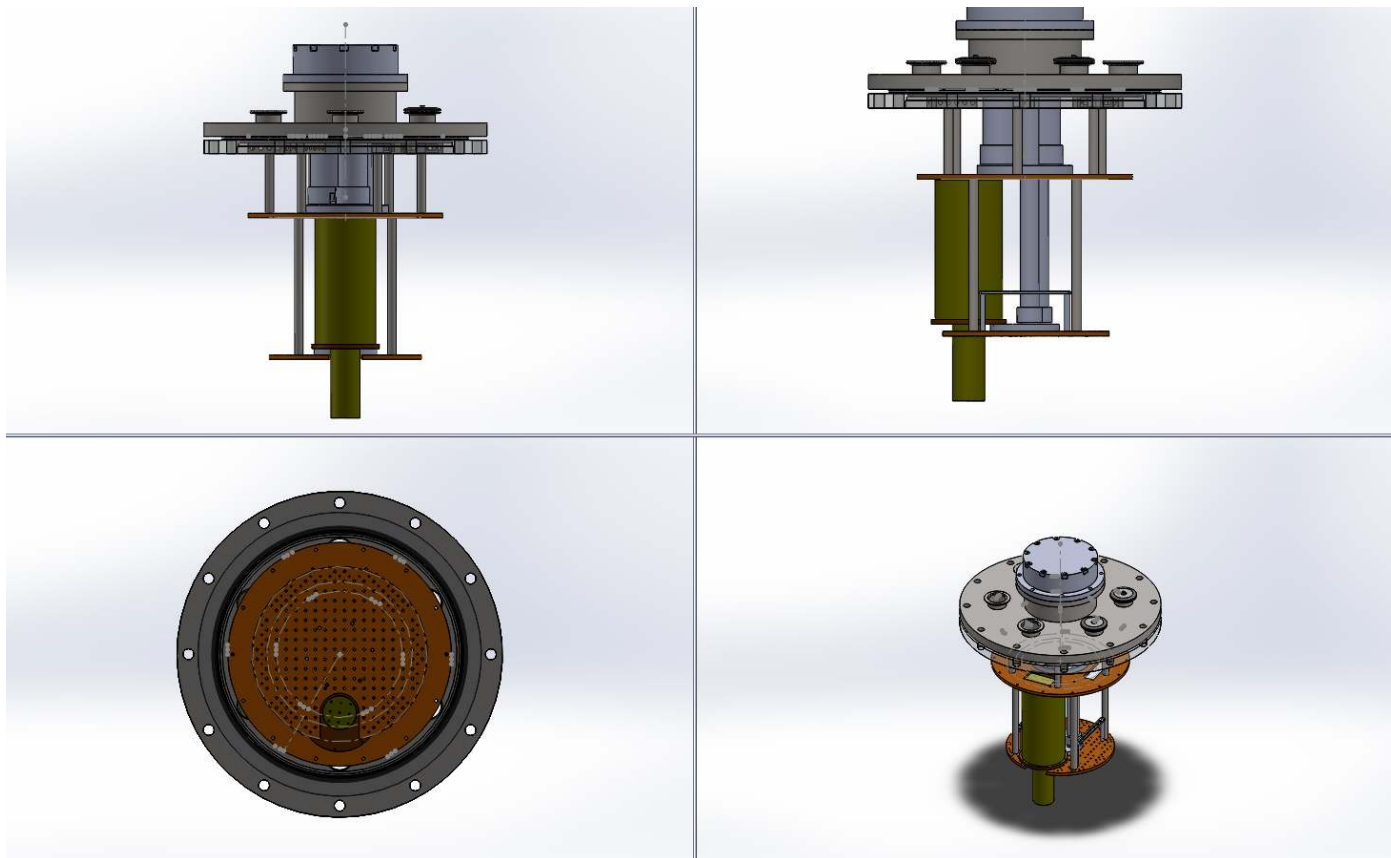
Things I would like to be able to do in the free space that are impossible due to the current design.

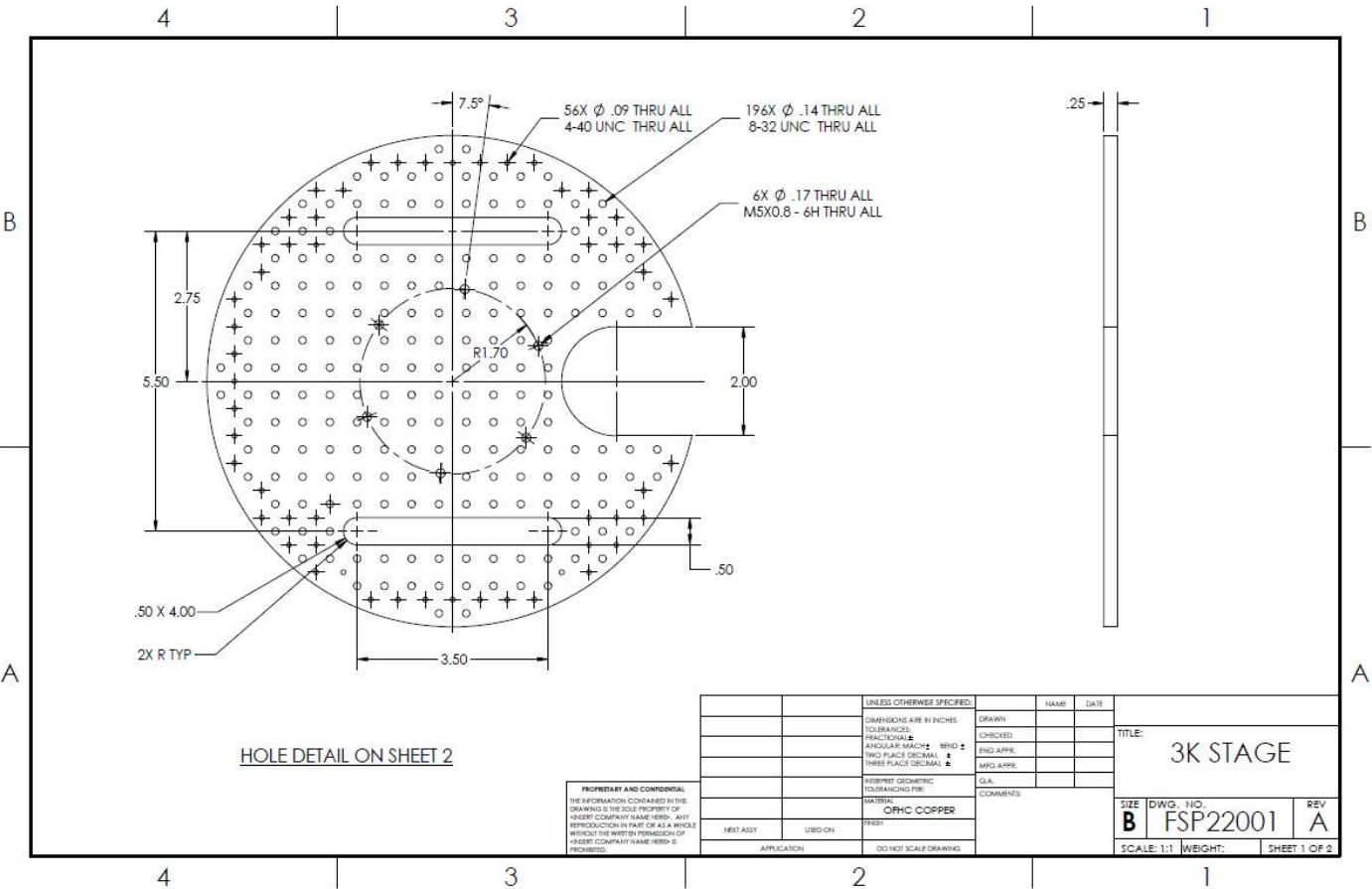
- Test more than one sample at a time.
- Install/Uninstall components easily.
 - Components like: cryo bias tee, midIR source, magnet, rf switch
- Reach the lowest possible temperature. With sorb ~ 1.7 , without ~ 2.7 , current = $3.7-4K$
- Install more RF and DC lines.

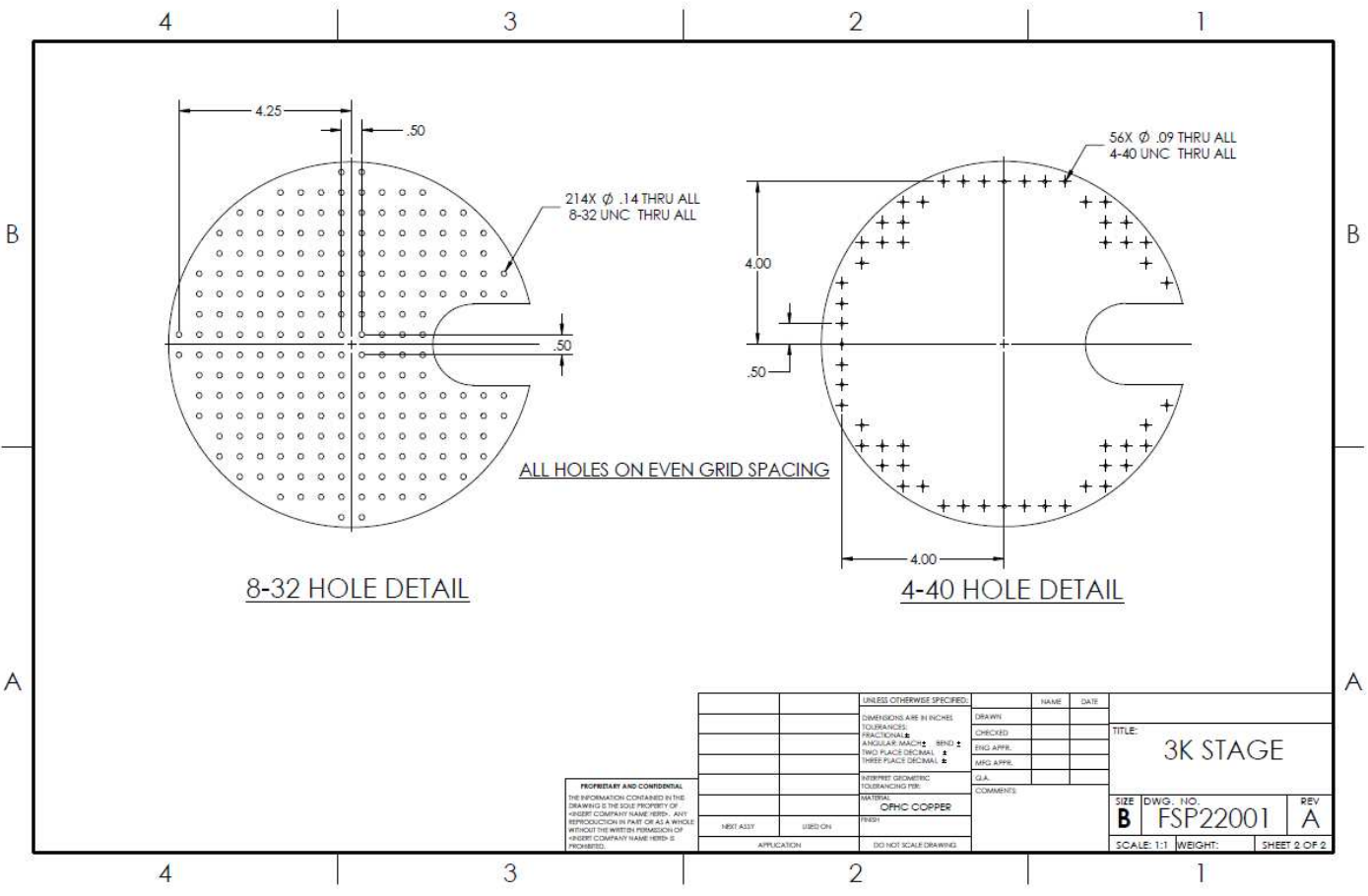
Questions to be answered:

- Should we keep G10 bars or swap out for SS?
- KF vacuum feedthrough currently 4SMA/KF40. Ideally we would have 8SMA/KF40





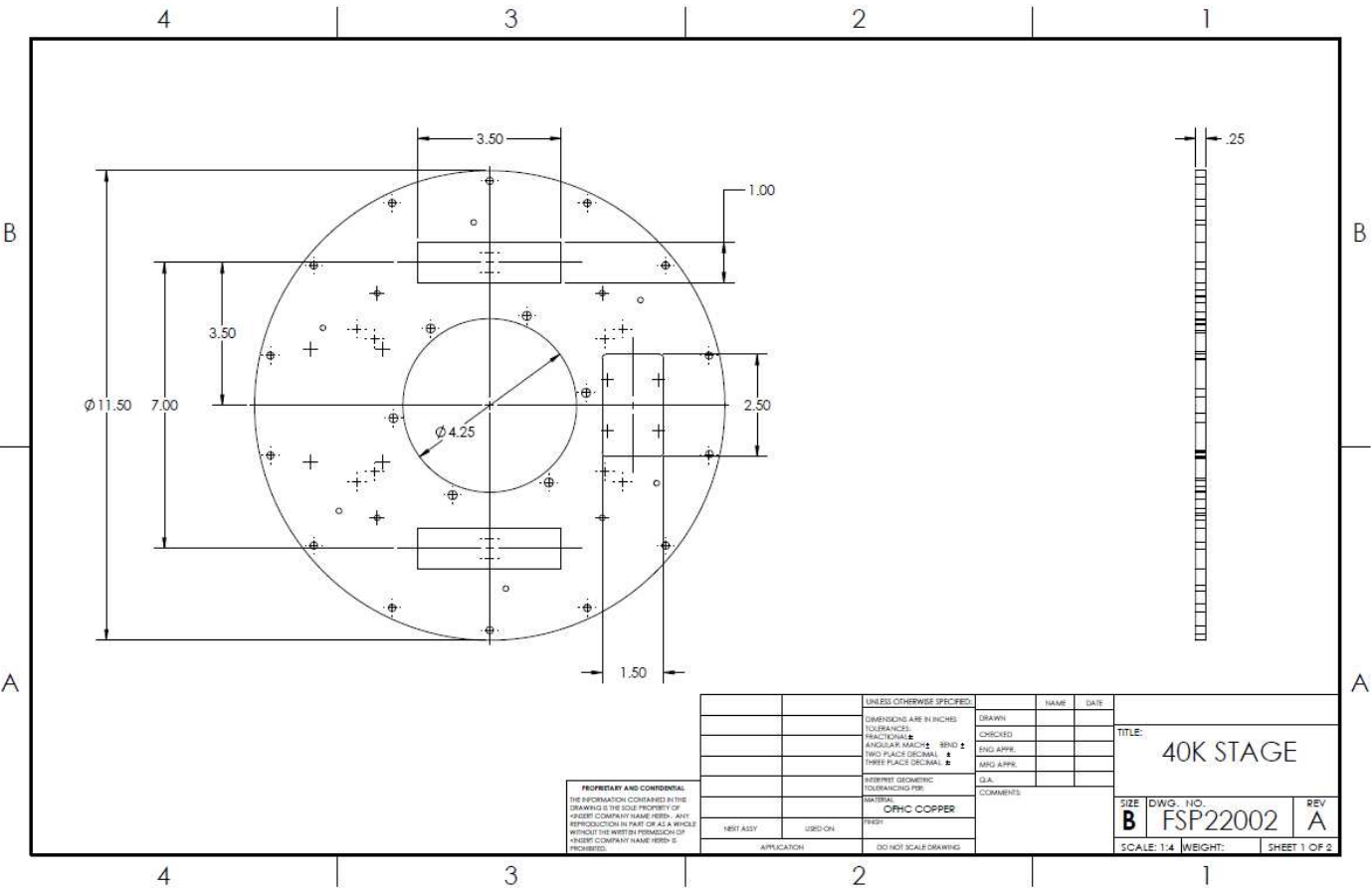




PROPRIETARY AND CONFIDENTIAL
THE INFORMATION CONTAINED IN THIS
DRAWING IS THE SOLE PROPERTY OF
HINERT COMPANY NAME HERE. ANY
REPRODUCTION IN PART OR AS A WHOLE
WITHOUT THE WRITTEN PERMISSION OF
HINERT COMPANY NAME HERE IS
PROHIBITED.

UNLESS OTHERWISE SPECIFIED:		NAME	DATE
DIMENSIONS ARE IN INCHES		DRAWN	
TOLERANCES		CHECKED	
FRACTIONAL $\pm$		ENG APPR.	
ANGULAR MATCH $\pm$.010		MRG APPR.	
TWO PLACE DECIMAL $\pm$		G.A.	
THREE PLACE DECIMAL $\pm$		COMMENTS	
INTERPRET GEOMETRIC			
TOLERANCING PER			
MATERIAL			
OFHC COPPER			
TEST			
TEST ASST	USED ON		
APPLICATION			
DO NOT SCALE DRAWING			

TITLE:		3K STAGE	
SIZE	DWG. NO.	REV	
B	FSP22001	A	
SCALE: 1:1	WEIGHT:	SHEET 2 OF 2	



PROPRIETARY AND CONFIDENTIAL
THE INFORMATION CONTAINED IN THIS
DRAWING IS THE SOLE PROPERTY OF
ANERT COMPANY NAME HERE. ANY
REPRODUCTION IN PART OR AS A WHOLE
WITHOUT THE WRITTEN PERMISSION OF
ANERT COMPANY NAME HERE IS
PROHIBITED.

UNLESS OTHERWISE SPECIFIED:		NAME	DATE
DIMENSIONS ARE IN INCHES		DRAWN	
TOLERANCES		CHECKED	
FRACTIONAL ± .005		ENG APPR.	
ANGULAR MATCH ± .010		MRG APPR.	
TWO PLACE DECIMAL ± .005		QA	
THREE PLACE DECIMAL ± .001		COMMENTS	
INTERPRET GEOMETRIC TOLERANCING PER			
MATERIAL			
COPPER			
FINISH			
NEXT ASSY			
USED ON			
APPLICATION			
		DO NOT SCALE DRAWING	

TITLE:		
40K STAGE		
SIZE	DWG. NO.	REV
B	FSP22002	A
SCALE: 1:4	WEIGHT:	SHEET 1 OF 2

